MC9S12XEP100
Reference Manual
Covers MC9S12XE Family

HCS12X
Microcontrollers

MC9S12XEP100RMV1

Rev. 1.25

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To provide the most up-to-date information, the document revision on the World Wide Web is the most current. A printed copy may be an earlier revision. To verif, refer to:

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This document contains information for the complete S12XE-Family and thus includes a set of separate FTM module sections to cover the whole family. A full list of family members and options is included in the appendices.

This document contains information for all constituent modules, with the exception of the S12X CPU. For S12X CPU information please refer to CPU12XV2 in the CPU12/CPU12X Reference Manual.

Revision History. Refer to module section revision history tables for more information.

Date	Revision	Description
Sep, 2008	1.18	Updated NVM timing parameter section for brownout case Specified time delay from RESET to start of CPU code execution Added NVM patch Part IDs Enhanced ECT GPIO / timer function transitioning description
Dec, 2008	1.19	Updated 208MAPBGA thermal parameters Revised TIM flag clearing procedure Corrected CRG register address Added maskset identifier suffix for ATMC fab Fixed typos
Aug, 2009	1.20	Added 208MAPBGA disclaimer Added VREAPI to PT5. Added LVR Note to electricals. Updates to TIM/ECT/XGATE/SCI/MSCAN (see embedded rev. history)
Apr, 2010	1.21	FTM section (see FTM revision history) PIM section (see PIM revision history)
May, 2010	1.22	ECT and TIM sections (see ECT, TIM revision history tables) BDM Alternate clock source defined in device overview
Sep, 2010	1.23	Added S12XEG256 option. Updated MSCAN section
Aug, 2012	1.24	Added bandgap voltage to electricals Added new maskset and Part ID numbers Minor updates to MSCAN,SCI and S12XINT sections Removed BGA disclaimer
Feb, 2013	1.25	Updated MSCAN section Formatting updates and minor corrections in PWM, CRG, BDM, DBG sections Updated Ordering Information

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Chapter 1
Device Overview MC9S12XE-Family

Chapter 2
Port Integration Module (S12XEPIMV1)

Chapter 3
Memory Mapping Control (S12XMMCV4)

Chapter 4
Memory Protection Unit (S12XMPUV1)

Chapter 5
External Bus Interface (S12XEBIV4)

Chapter 6
Interrupt (S12XINTV2)

Chapter 7
Background Debug Module (S12XBDMV2)

Chapter 8
S12X Debug (S12XDBGV3) Module

Chapter 9
Security (S12XE9SECV2)

Chapter 10
XGATE (S12XGATEV3)