

# **X2000/E IoT Application Processor**

Data Sheet

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北京君正集成电路股份有限公司  
Ingenic Semiconductor Co.,Ltd.

# **X2000/E IoT Application Processor**

## **Data Sheet**

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# 1 Overview

X2000/E is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

NAME	SIP LPDDR	RGMII
X2000	128MB, LPDDR3	x1
X2000E	256MB, LPDDR2	x2

## 1.1 Block Diagram

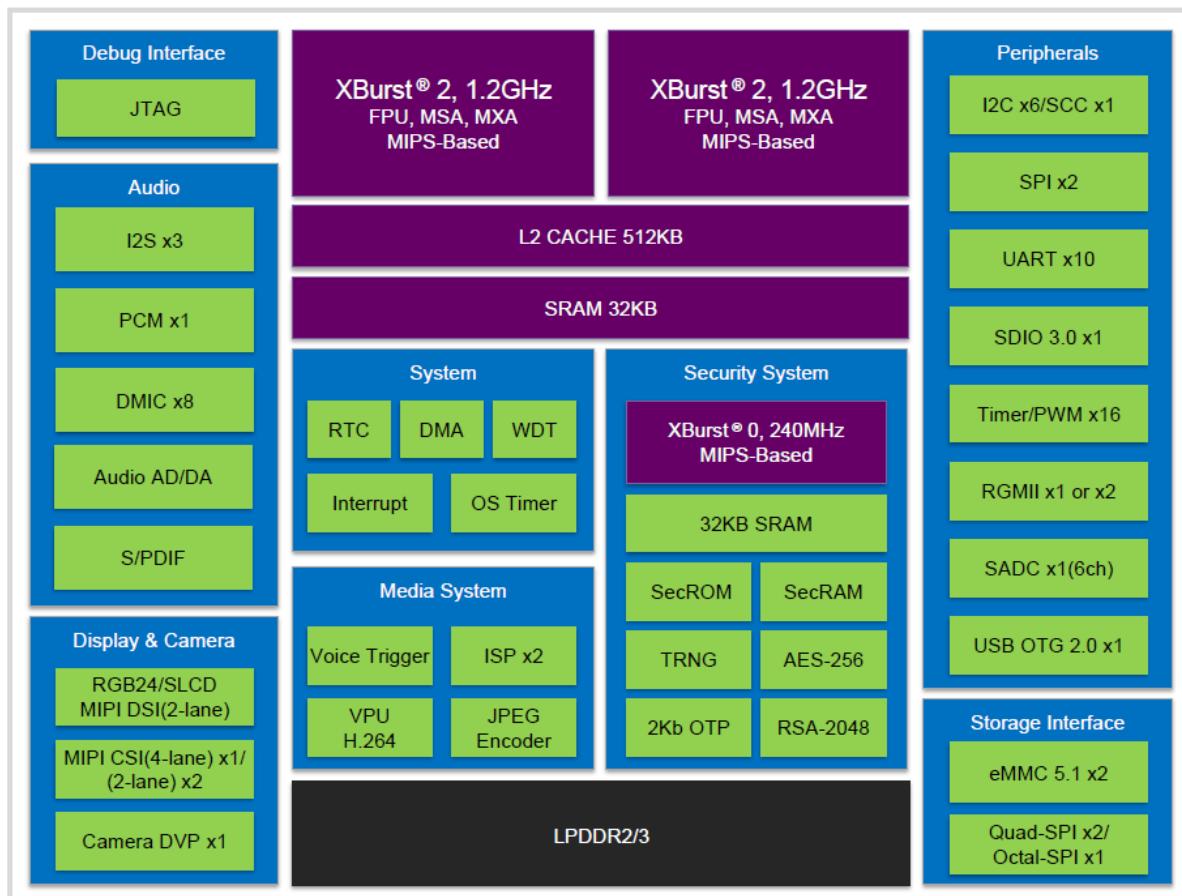


Figure 1-1 X2000/E Diagram

## 1.2 Features

### 1.2.1 CPU Core

- XBurst® 2, at 1.2GHz, Dual Core, Dual-issue, high performance and low power implementation of MIPS32 ISA R5
- MIPS32 ISA R5 plus MIPS SIMD instruction set architecture:128bit MSA
- Ingenic SIMD instruction set architecture: 128bit MXA
- Dual-issue, superscalar, super pipeline with Simultaneous Multi-Threading (SMT)
  - 2 hardware threads per physical core
  - Quad instruction fetch per cycle
  - Dual issue instructions per cycle per thread
- 32KB L1 D cache +32K L1 I cache , 512 KB L2 cache, 32KB SRAM
- High-performance Floating-point Unit and SIMD Engine: FSE
  - 32 x 128-bit register set, 128-bit loads/stores to/from SIMD unit
  - IEEE-754 2008 compliant
- Programmable Memory Management Unit (MMU)
  - 1st level mini-TLBs (MTLBs) – 8 x 2 entry instruction TLB, 16 x 2 entry data TLB
  - 2nd level TLBs: 32 × 2 entry VTLB, 256 × 2 entry 4-way set associative FTLB
- The XBurst® processor system supports little endian only

### 1.2.2 Video Process Unit(VPU)

- H.264 Encoder
  - Input data format NV12/NV21
  - Encoding resolution and frame rate up to 1920x1080@30fps
  - Support hardware RBSP bytes insertion
  - Support auto-read of slice header
  - Support reference frame lossless compression
- H.264 Decoder
  - Output data format NV12/NV21
  - Decoding resolution and frame rate up to 1920x1080@30fps
  - Support hardware RBSP bytes eliminate
- JPEG Codec
  - JPEG compressing/decompressing up to 70Mega-pixels per second
  - Baseline ISO/IEC 10918-1 JPEG compliant
  - 8-bit pixel depth support
  - Up to four programmable Quantization tables
  - Fully programmable Huffman tables

### 1.2.3 Image Signal Processor(ISPx2)

- Data stream feature
  - DVP: raw8 / 10 / 12 / YUV422 input
  - MIPI: up to 1080P@60fps
  - Support dual-camera sync

- Frame data check, make up for lost data and drop redundant data
- Advanced feature
  - 2A(Auto Exposure/Auto White Balance) supported
  - Advanced demosaic, color processing, lens shading, sharpen, static/dynamic defect pixel and other modules provide high image quality
  - 2-D noise reduction filter

#### 1.2.4 Memory Interface

- DDR Controller
  - Support LPDDR2, LPDDR3, 16Bit bus width, clock up to 800MHz
  - 128MB/256MB memory in package,
    - X2000: 128MB SIP LPDDR3
    - X2000E: 256MB SIP LPDDR2
- SFC Controller
  - 1 group clock and CE pad
  - Two Quad SPI, one Octal SPI ( SFC0/1 )
  - Support Standard, Dual, Quad SPI and Octal DDR protocol
  - Clock frequency up to 80MHz in SDR mode
  - Support multiple transfer modes, standard SPI, dual-output/dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI, and Octal-I/O

#### 1.2.5 Audio

- Digital Microphone Array Controller
  - Support 8 channels digital MIC
  - 24/16bit precision internal controller, sample rate support 8K, 16K, 32K, 48K and 96K
  - SNR: 90dB, THD: -90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
  - Low power voice trigger when waiting to start talking.
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.
  - Support low power voice trigger enable
- I2S(1~3) / I2S0
  - DMA transfer mode supported
  - Support share clock mode and split clock mode.
  - I2S0: Internal I2S CODEC supported
  - Support master mode and slave mode
  - Support number of data pin from 1 to 4
  - Support six modes of operation for TDM protocol
- PCM interface
  - Support master mode and slave mode
  - Support four modes of operation for PCM

- DSP NORMAL \ LEFT MODE
- PCM NORMAL \ LEFT MOD
- S/PDIF(IN and OUT)
  - Support IEC 60958-3 compliant, up to 2 channels
  - Sample bit support 20-bit and 24-bit two mode
  - Sample rate support, all of IEC60958-3 sample rate(44.1k up to 192k)
- Internal Audio Codec (**DAC and ADC working together**)
  - 24 bits DAC / ADC
  - Sample rate supported: 8k, 12k, 16k, 24k, 32k, 44.1k, 48k, 96k
  - **Mono Differential input/output**
  - DAC : SNR: 90dB A-Weighted, THD: -80dB @FS, -1dB ; ADC: SNR 90dB

### 1.2.6 MIPI-CSI

- MIPI-CSI2(v1.0) interface, resolution up to 1080P@120fps
  - Support dual 2-lane mode and single 4-lane mode
  - Support 1-lane, 2-lane and 4-lane mode

### 1.2.7 Camera

- Camera interface module(CIM)
  - Support DVP 8bit / MIPI input ,resolution up to 1280x720@30fps
  - Support snapshot control
  - Supported data format: RGB888, RGB565, YCbCr 4:2:2
  - Supports ITU656 (YCbCr 4:2:2) input
  - Support histogram output and global binarization

### 1.2.8 Display

- MIPI-DSI2(v1.0) interface
  - Display size up to 1920x1080@40Hz
- SLCD controller
  - Display size up to 640x480@60Hz, 24BPP
  - Supports different size of display panel
- RGB controller
  - Display size up to 1280x720@60Hz, 24BPP
  - Support input format, ARGB8888, ARGB1555, RGB888, RGB565, RGB555, YUV422, YUV420
  - Support 4 modes parallel interface, 24-bit, 18-bit, 16-bit and 8-bit(third times)
  - Support frame buffer crop and dither

### 1.2.9 System Functions

- Clock generation and power management
  - On-chip oscillator circuit (support 24MHz)
  - Two phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR\_CLK frequency can be changed

- separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down
- TCU
  - 8 channels each channel has two pins
  - Support posedge / negedge / dualedge clock counting
  - Support gate counting(only count for gating signal)
  - Support quadrature counting
  - Support direction counting(add / sub because of input signal)
  - Support counting after posedge / negedge signal
  - Support capture counting, output signal high-level time and total cycle time
  - Support exclk / pclk two clock source
- PWM
  - 16 channels, output signal ~50MHz, signal precision ~500MHz
  - Cpu / dma mode to update config
- OS timer
  - One event timer for one logic core
  - One global timer for system time
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
- Watchdog timer
  - A 16-bit Data register and a 16-bit counter
  - Programmable interrupt generation prior to timeout
  - Counter clock uses the input clock selected by software
    - EXTAL / RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- PDMA Controller
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit:  $1 \sim 2^{24} - 1$
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
- SAR A/D Controller
  - 6 Channels
  - Resolution: 10-bit

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32KHz clock generation.
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
  - Power Detect to Shut down PMU (find Core without voltage then shut PMU other voltage)

### 1.2.10 Peripherals

- General-Purpose I/O ports
  - Input / output / function port configurable
  - Low/high, rising/falling edge triggering. Every interrupt source can be masked independent
- Six I2C Controller (I2C0~5)
  - Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Three speeds mode
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
    - High speed mode (3.4Mb/s)
  - Programmable SCL generator
  - Master or slave I2C operation
  - 7-bit addressing/10-bit addressing
  - The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF
- One Smart Card Controller (SCC)
  - Supports normal card and UIM card.
  - Supports asynchronous character (T=0) communication modes.
  - Supports asynchronous block (T=1) communication modes.
  - Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.).
  - Supports extra guard time waiting.
  - Auto-error detection in T=0 receive mode.
  - Auto-character repeat in T=0 transmit mode.
  - Transforms inverted format to regular format and vice versa.
  - Support stop clock function in some power consuming sensitive applications.

- Two Synchronous serial interfaces (SSI0~1)
    - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
    - Full-duplex or transmit-only or receive-only operation
    - Programmable transfer order: MSB first or LSB first
    - Configurable normal transfer mode or Interval transfer mode
    - Programmable clock phase and polarity for Motorola's SSI format
    - Two slave select signal (SSI0\_CE0\_ / SSI1\_CE0\_) supporting up to 2 slave devices
    - Back-to-back character transmission/reception mode
    - Loop back mode for testing
    - Data transfer up to 30Mbits/s
  - Ten UARTs (UART0~9)
    - Full-duplex operation
    - Baud rate supports 4800, 9600, 19200, 38400, 43000, 56000, 57600, 115200, 230400, 460800, 576000, 921600, 1000000, 1152000, 1500000, 2000000, 2500000, 3000000, 3500000, 4000000, 6000000, 8000000, 12000000
    - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
    - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
    - Separate DMA requests for transmit and receive data services in FIFO mode
    - Supports modem flow control by software or hardware
  - Three MMC/SD/SDIO controllers (MSC0, MSC1, SDIO)
    - All support eMMC 5.1 (command queueing)
    - Support SD Specification 3.0
    - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
    - Maximum clock speed is 104MHz
    - Both support MMC data width 1bit, 4bit, only MSC0 support 8bit
    - Single or multi block access to the card including erase operation
    - The maximum block length is 4096bytes
  - USB 2.0 OTG interface
    - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
    - Support operating as USB peripheral, as USB host
    - Support split transmission
    - Support hub
    - Support remote-wakeup
  - GMAC controller
    - 10/100 Mbps and 1000Mbps operation
-

- Supports RMII and RGMII PHY interfaces
- Support IEEE 1588-2002
- Security System
  - XBurst®, 240MHz
  - Secret ROM and RAM
  - Up to 32KB SRAM
  - True Random Number Generator
  - Encryption Engine
    - MD5, SHA, SHA2
    - AES, support 256-bit, 192-bit, 128-bit key size Algorithm
    - RSA, support 1024/2048-bit key size
  - Support secure boot
- OTP Slave Interface
  - Total 2Kb.

### 1.2.11 Bootrom

16KB Boot ROM memory and 16KB Security Boot ROM

## 2 PAD Information

### 2.1 Pin Map

X2000 Ball Assignment Ver1.0 BGA270, 12mm X 12mm X 1.2mm, 0.65pitch, TOP view																		
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A MS01_D6_SF1_C DQ2_WP_UART Q.CTS_PD25	SD0_CMD_SS0 _DT_PD09	SD0_I2C1_S CK_PD11	SD0_I2C1_S DA_PD12		UART3_TXD_PCO M_D0_TCK_PDO 3	I2C_SCK_PCM DI_TMS_PDO4	VSS	VDDMEM	VREF	DDR_VDD1	DDRPLL_VCCA	VSS	UART3_RTS_I2 C5_SDA_P25	SD15_SS10_CLK UART9_RXD_P83 1	SD9_LCD_VSYN C_SLCDC_DC_PB 25	SD3_LCD_D19_R GMAC1_MDC_PB 19		
B MS01_CMD_SF0 I2C_SSH1_D1 PD18	SD0_CLK_SS0 CLK_PD08	SD0_I2C1_S R_PD10	UART2_RXD_PCO 3_SCK_PWM1_T CU0_IN0_PD30	UART3_CTS_I2 C4_SCK_PDO0	UART3_RXD_PCO 2	I2C_SDA_PCM SYNC_PD05	VDDMEM	VDDMEM	VSS	DDR_VDD1	DDR_VSSA	VSS	UART3_RXD_I2C 4_SCK_P25	SD10_LCD_HSY NC_SLCDC_WR_P 4	SD2_LCD_D18_R GMAC1_RXD_VD PB18	B		
C MS01_D1_SF0 DQ1_B2C2_SCK PD20	MS01_D0_SF0 DQ0_SSH1_DR_P D19	MS01_D7_SF1_C DQ3_HOLD_UA RT0_RTS_P26	SD0_I2C1_S E0_PD13	UART2_RXD_PCO 3_SDA_PWM1_T CU0_IN1_PD31	UART3_RTS_I2 C4_SDA_TDO_P D01	VSS	VDDMEM	VDDMEM	ZQ	VSS	VDDMEM	VDDMEM	UART3_CTS_I2 C5_SDA_P27	SD14_SS0_DT UART8_RXD_PB B16	SD7_LCD_D23_I2 C2_SDA_RGMAC 3	SD4_LCD_D20_R GMAC1_MDD_P C20		
D MS01_CLK_SF0 I2C_SSH1_CLK PD17	MS01_D2_SF0 DQ2_WP_DC2 SDA_PD21	MS01_D4_SF0 DQ0_UART0_RX D0_P22	ADEVFUSE	TRST	VSS	VSS	VSS	VSS	VDDMEM	VDDMEM	VDDMEM	VDDMEM	SD12_SS0_CEO UART8_RXD_P B29	SD11_LCD_DE 9	WE_LCD_D14 SLCD_D14_RGM AC1_RXD2_PB27	SD2_LCD_D12_R SLCD_D12_RGM AC1_RXD0_PB12		
E RTC32K_PE23	EXCLK_CIM_VC MCILK_P24	MS01_D5_SF1_C DQ1_UART0_RX D_P24												WAIT_LCD_D15 SLCD_D15_R6 MAC1_RXD3_PB 15	S06_LCD_D22_I2 C2_SCK_RGMAC 1_RXCLK_PB22	S11_LCD_D15_S C1_RXD1_PB13	E	
F VDDIO_RTC	WKUP__PE31	PWRON	DRV_VBUS_P2		VSS	VSS	VDD	VDD	VSS	VDD	VDD	VSS		SD1_LCD_D17_R S041_LCD_D11 SLCD_D11_RGM AC1_RXD3_PB11	S09_LCD_D8_S GMAC1_TX_EN PB17	S04_LCD_D8_S CD_D9_RGMAC AC1_RXD2_PB10	F	
G OSC32_X0	OSC32_X0	PPRST_	TEST_TE		VDDIO	VSS	VDD	VDD	VSS	VDD	VDD	VSS		SA6_LCD_D6_SL CD_D6_P206	SA3_LCD_D3_SL CD_D3_P203	SD5_LCD_D21_I2 GMAC1_TX_CLK PB21	SA6_LCD_D8_S CD_D8_RGMAC TXD0_P208	G
H PLL_AVDD	VDD_RTC	VSS_RTC		VDDIO	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDDIO33		SA5_LCD_D5_P205	SA1_LCD_D1_SL CD_D1_P201	SA2_LCD_D2_SL CD_D2_P202	H	
J EXCLK_X0	EXCLK_X0	PLL_VDD	PLL_AVSS		VSS	VSS	VSS			VSS	VSS	VDDIO18		SA7_LCD_D7_SL CD_D7_P207	SA4_LCD_D4_SL CD_D4_P204	TX_DATAP1	TX_DATAP1	J
K I2C3_SCK_I2S3 TX_BCLK_PA16	BOOT_SEL2_PE 27	PLL_VSS	BOOT_SEL1_PE 25		VSS	VDD	VDD			VDD	VDD	VSS		SA0_LCD_D0_SL CD_D0_P200	TX_DATAP0	TX_CLKP	TX_CLKN	K
L CIM_EXPOSURE _PA15	I2C3_SDA_I2S2 RX_BCLK_PA17			VSS	VDD	VDD	VSS	VSS	VDD	VDD	VDD	VSS		DSI_AVSS	DSI_AVD09	TX_DATAN0		L
M CIM_VIC_VSYNC _PA13	CIM_VIC_HSYNC _PA15	CIM_VIC_PCLK_P A14	CIM_D10_I2S2_R X_DA10_PA10	VDDIO33_CIM	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VSS		CSI_AVSS	CSI_AVD18	RX_DATAP0	RX_DATAN0	M
N VIC_D11_I2S2_R X_DATA1_PA11	VIC_D9_UART7 TXD_I2S2_RX_LR CK_PA09	VIC_D8_UART7 RXD_PA08	CIM_VIC_D7_UAR T5_RXD_I2S3_TX _DATA1_PA05	VDDIO18_CIM	VSS	VDDIO18_SD	VDDIO33_SD	VSS	VSS	VDDIO18	VDDIO33			CSI_AVD09	RX_CLKP0	RX_DATAP1	RX_DATAN1	N
P CIM_VIC_D4_UAR T5_RXD_I2S3_TX _DATA1_PA04	CIM_VIC_D5_UAR T5_RXD_I2S3_TX _DATA2_PA05	CIM_VIC_D6_UAR T5_RXD_I2S3_TX _DATA2_PA06	USB_AVSS	USB_ID	USB_BIAS	CODEC_AVSS	MSC1_D3_PWM _TCU3_IN1_P205	MSC1_CLK_PWM 2_TCU1_IN1_P200	PWM4_TC12_IN0 ROMAC0_TCX0 0_ROMAC0_TC 1_ROMAC0_TCX0 1_ROMAC0_TC 2_ROMAC0_TCX0 2_ROMAC0_TC 3_ROMAC0_TCX0 3_ROMAC0_TC 4_ROMAC0_TC 5_ROMAC0_TCX0 5_ROMAC0_TC 6_ROMAC0_TC 7_ROMAC0_TCX0 7_ROMAC0_TC 8_ROMAC0_TC 9_ROMAC0_TC 10_ROMAC0_TC 11_ROMAC0_TC 12_ROMAC0_TC 13_ROMAC0_TC 14_ROMAC0_TC 15_ROMAC0_TC 16_ROMAC0_TC 17_ROMAC0_TC 18_ROMAC0_TC 19_ROMAC0_TC 20_ROMAC0_TC 21_ROMAC0_TC 22_ROMAC0_TC 23_ROMAC0_TC 24_ROMAC0_TC 25_ROMAC0_TC 26_ROMAC0_TC 27_ROMAC0_TC 28_ROMAC0_TC 29_ROMAC0_TC 30_ROMAC0_TC 31_ROMAC0_TC 32_ROMAC0_TC 33_ROMAC0_TC 34_ROMAC0_TC 35_ROMAC0_TC 36_ROMAC0_TC 37_ROMAC0_TC 38_ROMAC0_TC 39_ROMAC0_TC 40_ROMAC0_TC 41_ROMAC0_TC 42_ROMAC0_TC 43_ROMAC0_TC 44_ROMAC0_TC 45_ROMAC0_TC 46_ROMAC0_TC 47_ROMAC0_TC 48_ROMAC0_TC 49_ROMAC0_TC 50_ROMAC0_TC 51_ROMAC0_TC 52_ROMAC0_TC 53_ROMAC0_TC 54_ROMAC0_TC 55_ROMAC0_TC 56_ROMAC0_TC 57_ROMAC0_TC 58_ROMAC0_TC 59_ROMAC0_TC 60_ROMAC0_TC 61_ROMAC0_TC 62_ROMAC0_TC 63_ROMAC0_TC 64_ROMAC0_TC 65_ROMAC0_TC 66_ROMAC0_TC 67_ROMAC0_TC 68_ROMAC0_TC 69_ROMAC0_TC 70_ROMAC0_TC 71_ROMAC0_TC 72_ROMAC0_TC 73_ROMAC0_TC 74_ROMAC0_TC 75_ROMAC0_TC 76_ROMAC0_TC 77_ROMAC0_TC 78_ROMAC0_TC 79_ROMAC0_TC 80_ROMAC0_TC 81_ROMAC0_TC 82_ROMAC0_TC 83_ROMAC0_TC 84_ROMAC0_TC 85_ROMAC0_TC 86_ROMAC0_TC 87_ROMAC0_TC 88_ROMAC0_TC 89_ROMAC0_TC 90_ROMAC0_TC 91_ROMAC0_TC 92_ROMAC0_TC 93_ROMAC0_TC 94_ROMAC0_TC 95_ROMAC0_TC 96_ROMAC0_TC 97_ROMAC0_TC 98_ROMAC0_TC 99_ROMAC0_TC 100_ROMAC0_TC 101_ROMAC0_TC 102_ROMAC0_TC 103_ROMAC0_TC 104_ROMAC0_TC 105_ROMAC0_TC 106_ROMAC0_TC 107_ROMAC0_TC 108_ROMAC0_TC 109_ROMAC0_TC 110_ROMAC0_TC 111_ROMAC0_TC 112_ROMAC0_TC 113_ROMAC0_TC 114_ROMAC0_TC 115_ROMAC0_TC 116_ROMAC0_TC 117_ROMAC0_TC 118_ROMAC0_TC 119_ROMAC0_TC 120_ROMAC0_TC 121_ROMAC0_TC 122_ROMAC0_TC 123_ROMAC0_TC 124_ROMAC0_TC 125_ROMAC0_TC 126_ROMAC0_TC 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## 2.2 Pin Description

### 2.2.1 GPIO Group A

Ball No.	Ball Name	In/O ut	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Power
R4	CIM_VIC_D0_UART4_CTS_I2S3_TX_MCLK_PA00	IO	PU	Yes	Yes	GPA[0]	CIM/VIC_D0	UART4_CTS_	I2S3_TX_MCLK	VDDIO33_CIM
R3	CIM_VIC_D1_UART4_RTS_PA01	IO	PU	Yes	Yes	GPA[1]	CIM/VIC_D1	UART4_RTS_		VDDIO33_CIM
R2	CIM_VIC_D2_UART4_RXD_I2S3_TX_LRCK_PA02	IO	PU	Yes	Yes	GPA[2]	CIM/VIC_D2	UART4_RXD	I2S3_TX_LRCK	VDDIO33_CIM
R1	CIM_VIC_D3_UART4_TXD_I2S3_TX_DATA0_PA03	IO	PU	Yes	Yes	GPA[3]	CIM/VIC_D3	UART4_TXD	I2S3_TX_DATA0	VDDIO33_CIM
P2	CIM_VIC_D4_UART5_RXD_I2S3_TX_DATA1_PA04	IO	PU	Yes	Yes	GPA[4]	CIM/VIC_D4	UART5_RXD	I2S3_TX_DATA1	VDDIO33_CIM
P3	CIM_VIC_D5_UART5_TXD_I2S3_TX_DATA2_PA05	IO	PU	Yes	Yes	GPA[5]	CIM/VIC_D5	UART5_TXD	I2S3_TX_DATA2	VDDIO33_CIM
P4	CIM_VIC_D6_UART6_RXD_I2S3_TX_DATA3_PA06	IO	PU	Yes	Yes	GPA[6]	CIM/VIC_D6	UART6_RXD	I2S3_TX_DATA3	VDDIO33_CIM
N4	CIM_VIC_D7_UART6_TXD_I2S2_RX_MCLK_PA07	IO	PU	Yes	Yes	GPA[7]	CIM/VIC_D7	UART6_TXD	I2S2_RX_MCLK	VDDIO33_CIM
N3	VIC_D8_UART7_RXD_PA08	IO	PU	Yes	Yes	GPA[8]	VIC_D8	UART7_RXD		VDDIO33_CIM
N2	VIC_D9_UART7_TXD_I2S2_RX_LRCK_PA09	IO	PU	Yes	Yes	GPA[9]	VIC_D9	UART7_TXD	I2S2_RX_LRCK	VDDIO33_CIM
M4	VIC_D10_I2S2_RX_DATA0_PA10	IO	PU	Yes	Yes	GPA[10]	VIC_D10		I2S2_RX_DATA0	VDDIO33_CIM
N1	VIC_D11_I2S2_RX_DATA1_PA11	IO	PU	Yes	Yes	GPA[11]	VIC_D11		I2S2_RX_DATA1	VDDIO33_CIM
M2	CIM_VIC_HSYNC_I2S2_RX_DATA2_PA12	IO	PD	Yes	Yes	GPA[12]	CIM_VIC_HSYNC		I2S2_RX_DATA2	VDDIO33_CIM
M1	CIM_VIC_VSYNC_I2S2_RX_DATA3_PA13	IO	PD	Yes	Yes	GPA[13]	CIM_VIC_VSYNC		I2S2_RX_DATA3	VDDIO33_CIM
M3	CIM_VIC_PCLK_PA14	IO	PD	Yes	Yes	GPA[14]	CIM/VIC_PCLK			VDDIO33_CIM
L2	CIM_EXPOSURE_PA15	IO	PD	Yes	Yes	GPA[15]	CIM_EXPOSURE			VDDIO33_CIM
K1	I2C3_SCK_I2S3_TX_BCLK_PA16	IO	PU	Yes	Yes	GPA[16]	I2C3_SCK		I2S3_TX_BCLK	VDDIO33_CIM
L3	I2C3_SDA_I2S2_RX_BCLK_PA17	IO	PU	Yes	Yes	GPA[17]	I2C3_SDA		I2S2_RX_BCLK	VDDIO33_CIM

### 2.2.2 GPIO Group B

Ball No.	Ball Name	In/Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
K15	SA0_LCD_D0_SLCD_D0_PB00	IO	PD	No	Yes	GPB[0]	SA0	LCD_D0	SLCD_D0		VDDIO33
H16	SA1_LCD_D1_SLCD_D1_PB01	IO	PD	No	Yes	GPB[1]	SA1	LCD_D1	SLCD_D1		VDDIO33
H17	SA2_LCD_D2_SLCD_D2_PB02	IO	PD	No	Yes	GPB[2]	SA2	LCD_D2	SLCD_D2		VDDIO33
G16	SA3_LCD_D3_SLCD_D3_PB03	IO	PD	No	Yes	GPB[3]	SA3	LCD_D3	SLCD_D3		VDDIO33
J16	SA4_LCD_D4_SLCD_D4_PB04	IO	PD	No	Yes	GPB[4]	SA4	LCD_D4	SLCD_D4		VDDIO33
H15	SA5_LCD_D5_SLCD_D5_PB05	IO	PD	No	Yes	GPB[5]	SA5	LCD_D5	SLCD_D5		VDDIO33
G15	SA6_LCD_D6_SLCD_D6_PB06	IO	PD	No	Yes	GPB[6]	SA6	LCD_D6	SLCD_D6		VDDIO33
J15	SA7_LCD_D7_SLCD_D7_PB07	IO	PD	No	Yes	GPB[7]	SA7	LCD_D7	SLCD_D7		VDDIO33
G18	SA8_LCD_D8_SLCD_D8_RGMAC1_TXD0_PB08	IO	PD	No	Yes	GPB[8]	SA8	LCD_D8	SLCD_D8	RGMAC1_RXD0	VDDIO33
F18	SA9_LCD_D9_SLCD_D9_RGMAC1_TXD1_PB09	IO	PD	No	Yes	GPB[9]	SA9	LCD_D9	SLCD_D9	RGMAC1_RXD1	VDDIO33
F17	SA10_LCD_D10_SLCD_D10_RGMAC1_TXD2_PB10	IO	PD	No	Yes	GPB[10]	SA10	LCD_D10	SLCD_D10	RGMAC1_RXD2	VDDIO33
F16	SA11_LCD_D11_SLCD_D11_RGMAC1_TXD3_PB11	IO	PD	No	Yes	GPB[11]	SA11	LCD_D11	SLCD_D11	RGMAC1_RXD3	VDDIO33
D18	SA12_LCD_D12_SLCD_D12_RGMAC1_RXD0_PB12	IO	PD	No	Yes	GPB[12]	SA12	LCD_D12	SLCD_D12	RGMAC1_RXD0	VDDIO33
E17	RD_LCD_D13_SLCD_D13_RG MAC1_RXD1_PB13	IO	PU	No	Yes	GPB[13]	RD_	LCD_D13	SLCD_D13	RGMAC1_RXD1	VDDIO33
D17	WE_LCD_D14_SLCD_D14_RGMAC1_RXD2_PB14	IO	PU	No	Yes	GPB[14]	WE_	LCD_D14	SLCD_D14	RGMAC1_RXD2	VDDIO33
E15	WAIT_LCD_D15_SLCD_D15_RGMAC1_RXD3_PB15	IO	PU	No	Yes	GPB[15]	WAIT_	LCD_D15	SLCD_D15	RGMAC1_RXD3	VDDIO33
C16	SD0_LCD_D16_PB16	IO	PU	No	Yes	GPB[16]	SD0	LCD_D16	SLCDRD		VDDIO33
F15	SD1_LCD_D17_RGMAC1_TXEN_PB17	IO	PU	No	Yes	GPB[17]	SD1	LCD_D17		RGMAC1_TX_EN	VDDIO33
B18	SD2_LCD_D18_RGMAC1_RXDV_PB18	IO	PU	No	Yes	GPB[18]	SD2	LCD_D18		RGMAC1_RX_DV	VDDIO33
A18	SD3_LCD_D19_RGMAC1_MDC	IO	PU	No	Yes	GPB[19]	SD3	LCD_D19		RGMAC1_MDC	VDDIO33

	_PB19										
C18	SD4_LCD_D20_RGMAC1_MDI_O_PB20	IO	PU	No	Yes	GPB[20]	SD4	LCD_D20		RGMAC1_MDIO	VDDIO33
G17	SD5_LCD_D21_RGMAC1_TX_CLK_PB21	IO	PU	No	Yes	GPB[21]	SD5	LCD_D21		RGMAC1_TX_CLK_O	VDDIO33
E16	SD6_LCD_D22_I2C2_SCK_RG_MAC1_RX_CLK_PB22	IO	PU	No	Yes	GPB[22]	SD6	LCD_D22	I2C2_SCK	RGMAC1_RX_CLK_I	VDDIO33
C17	SD7_LCD_D23_I2C2_SDA_RG_MAC1_PHY_CLK_PB23	IO	PU	No	Yes	GPB[23]	SD7	LCD_D23	I2C2_SDA	RGMAC1_PHY_CLK_O	VDDIO33
B17	SD8_LCD_PCLK_SLCD_CE_P_B24	IO	PU	No	Yes	GPB[24]	SD8	LCD_PCLK	SLCD_CE_		VDDIO33
A17	SD9_LCD_VSYNC_SLCD_DC_PB25	IO	PU	No	Yes	GPB[25]	SD9	LCD_VSYNC	SLCD_DC		VDDIO33
B16	SD10_LCD_HSYNC_SLCD_WR_PB26	IO	PU	No	Yes	GPB[26]	SD10	LCD_HSYNC	SLCD_WR		VDDIO33
D16	SD11_LCD_DE_SLCD_TE_PB27	IO	PU	No	Yes	GPB[27]	SD11	LCD_DE	SLCD_TE		VDDIO33
D14	SD12_SSI0_CE0_UART8_RX_D_PB28	IO	PU	No	Yes	GPB[28]	SD12	SSI0_CE0_	UART8_RX_D		VDDIO33
D15	SD13_SSI0_DR_UART8_TXD_PB29	IO	PU	No	Yes	GPB[29]	SD13	SSI0_DR	UART8_TX_D		VDDIO33
C15	SD14_SSI0_DT_UART9_RXD_PB30	IO	PU	No	Yes	GPB[30]	SD14	SSI0_DT	UART9_RX_D		VDDIO33
A16	SD15_SSI0_CLK_UART9_TXD_PB31	IO	PU	No	Yes	GPB[31]	SD15	SSI0_CLK	UART9_TX_D		VDDIO33

## 2.2.3 GPIO Group C

Ball No.	Ball Name	In/Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
P15	PWM0_TCU0_IN0_PC00	IO	PD	No	Yes	GPC[0]	PWM0_TCU0_IN0				VDDIO33
V16	PWM1_TCU0_IN1_RGMAC0_P HY_CLK_I2S1_RX_MCLK_UAR T7_RXD_PC01	IO	PU	No	Yes	GPC[1]	PWM1_TCU0_IN1	RGMAC0_PHY_CLK	I2S1_RX_MCLK	UART7_RXD	VDDIO33
V13	PWM2_TCU1_IN0_RGMAC0_T XD0_I2S1_RX_BCLK_UART7_TXD_PC02	IO	PU	No	Yes	GPC[2]	PWM2_TCU1_IN0	RGMAC0_TXD0	I2S1_RX_B_CLK	UART7_TXD	VDDIO33
U13	PWM3_TCU1_IN1_RGMAC0_T XD1_I2S1_RX_LRCK_SCC_SC_K_PC03	IO	PU	No	Yes	GPC[3]	PWM3_TCU1_IN1	RGMAC0_TXD1	I2S1_RX_L_RCK	SCC_SCK	VDDIO33
R11	PWM4_TCU2_IN0_RGMAC0_T XD2_I2S1_RX_DATA_SCC_SD_A_PC04	IO	PU	No	Yes	GPC[4]	PWM4_TCU2_IN0	RGMAC0_TXD2	I2S1_RX_DATA	SCC_SDA	VDDIO33
U14	PWM5_TCU2_IN1_RGMAC0_T XD3_I2S1_TX_BCLK_UART5_RXD_PC05	IO	PU	No	Yes	GPC[5]	PWM5_TCU2_IN1	RGMAC0_TXD3	I2S1_TX_B_CLK	UART5_RXD	VDDIO33
T14	PWM6_TCU3_IN0_RGMAC0_R XD0_I2S1_TX_LRCK_UART5_TXD_PC06	IO	PU	No	Yes	GPC[6]	PWM6_TCU3_IN0	RGMAC0_RXD0	I2S1_TX_L_RCK	UART6_RXD	VDDIO33
T13	PWM7_TCU3_IN1_RGMAC0_R XD1_I2S1_TX_DATA_UART6_RXD_PC07	IO	PU	No	Yes	GPC[7]	PWM7_TCU3_IN1	RGMAC0_RXD1	I2S1_TX_DATA	UART6_RXD	VDDIO33
U15	PWM8_TCU4_IN0_RGMAC0_R XD2_I2S1_TX_MCLK_UART6_TXD_PC08	IO	PU	No	Yes	GPC[8]	PWM8_TCU4_IN0	RGMAC0_RXD2	I2S1_TX_MCLK	UART6_TXD	VDDIO33
R14	PWM9_TCU4_IN1_RGMAC0_R XD3_SSI1_CE0_UART4_CTS_PC09	IO	PU	No	Yes	GPC[9]	PWM9_TCU4_IN1	RGMAC0_RXD3	SSI1_CE0_-	UART4_CTS	VDDIO33
R12	PWM10_TCU5_IN0_RGMAC0_TX_EN_SSI1_DR_UART4_RTS	IO	PU	No	Yes	GPC[10]	PWM10_TCU5_IN0	RGMAC0_TX_E_N	SSI1_DR_-	UART4_RTS	VDDIO33

	PC10										
R13	PWM11_TCU5_IN1_RGMAC0_RX_DV_SSI1_DT_UART4_RXD_PC11	IO	PU	No	Yes	GPC[11]	PWM11_TCU5_IN1	RGMAC0_RX_DV	SSI1_DT	UART4_RXD	VDDIO33
R15	PWM12_TCU6_IN0_RGMAC0_MDC_SSI1_CLK_UART4_TXD_PC12	IO	PU	No	Yes	GPC[12]	PWM12_TCU6_IN0	RGMAC0_MDC	SSI1_CLK	UART4_TXD	VDDIO33
T15	PWM13_TCU6_IN1_RGMAC0_MDIO_SPDIF_IN_I2C0_SCK_PC13	IO	PU	No	Yes	GPC[13]	PWM13_TCU6_IN1	RGMAC0_MDIO	SPDIF_IN	I2C0_SCK	VDDIO33
T12	PWM14_TCU7_IN0_RGMAC0_TX_CLK_SPDIF_OUT_I2C0_SDA_PC14	IO	PU	No	Yes	GPC[14]	PWM14_TCU7_IN0	RGMAC0_TX_CLK	SPDIF_OUT	I2C0_SDA	VDDIO33
V15	PWM15_TCU7_IN1_RGMAC0_RX_CLK_CIM_VIC_MCLK_PC15	IO	PU	No	Yes	GPC[15]	PWM15_TCU7_IN1	RGMAC0_RX_CLK	CIM/VIC_M_CLK		VDDIO33
V17	DMIC_CLK_PC20	IO	PD	No	Yes	GPC[20]	DMIC_CLK				VDDIO33
U16	DMIC_IN0_UART1_CTS_PC21	IO	PU	No	Yes	GPC[21]	DMIC_IN0	UART1_CTS_			VDDIO33
V18	DMIC_IN1_UART1_RTS_PC22	IO	PU	No	Yes	GPC[22]	DMIC_IN1	UART1_RTS_			VDDIO33
T16	DMIC_IN2_UART1_RXD_I2C1_SCK_NEMC_CS1_PC23	IO	PU	No	Yes	GPC[23]	DMIC_IN2	UART1_RXD	I2C1_SCK	NEMC_CS1_	VDDIO33
R16	DMIC_IN3_UART1_TXD_I2C1_SDA_NEMC_CS2_PC24	IO	PU	No	Yes	GPC[24]	DMIC_IN3	UART1_TXD	I2C1_SDA	NEMC_CS2_	VDDIO33
B14	UART3_RXD_I2C4_SCK_PC25	IO	PU	No	Yes	GPC[25]	UART3_RXD	I2C4_SCK			VDDIO33
B15	UART3_TXD_I2C4_SDA_PC26	IO	PU	No	Yes	GPC[26]	UART3_TXD	I2C4_SDA			VDDIO33
C14	UART3_CTS_I2C5_SCK_PC27	IO	PU	No	Yes	GPC[27]	UART3_CTS_	I2C5_SCK			VDDIO33
A15	UART3_RTS_I2C5_SDA_PC28	IO	PU	No	Yes	GPC[28]	UART3_RTS_	I2C5_SDA			VDDIO33

## 2.2.4 GPIO Group D

Ball No.	Ball Name	In/Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Func2	Func3	Power
B5	UART3_CTS_I2C4_SCK_PD00	IO	PU	No	No	GPD[0]	GPIO0	UART3_CTS_	I2C4_SCK		VDDIO
C6	UART3_RTS_I2C4_SDA_TDO_PD01	IO	PU	No	No	GPD[1]	GPIO1	UART3_RTS_	I2C4_SDA	TDO	VDDIO
B6	UART3_RXD_PCM_CLK_TDI_PD02	IO	PU	No	No	GPD[2]	GPIO2	UART3_RXD	PCM_CLK	TDI	VDDIO
A6	UART3_TXD_PCM_DO_TCK_PD03	IO	PU	No	No	GPD[3]	GPIO3	UART3_TXD	PCM_DO	TCK	VDDIO
A7	I2C5_SCK_PCM_DI_TMS_PD04	IO	PU	No	No	GPD[4]	GPIO4	I2C5_SCK	PCM_DI	TMS	VDDIO
B7	I2C5_SDA_PCM_SYNC_PD05	IO	PU	No	No	GPD[5]	GPIO5	I2C5_SDA	PCM_SYNC		VDDIO
B2	SDIO_CLK_SSI0_CLK_PD08	IO	PU	No	No	GPD[8]	SDIO_CLK	SSI0_CLK			VDDIO
A2	SDIO_CMD_SSI0_DT_PD09	IO	PU	No	No	GPD[9]	SDIO_CMD	SSI0_DT			VDDIO
B3	SDIO_D0_SSI0_DR_PD10	IO	PU	No	No	GPD[10]	SDIO_D0	SSI0_DR			VDDIO
A3	SDIO_D1_I2C1_SCK_PD11	IO	PU	No	No	GPD[11]	SDIO_D1	I2C1_SCK			VDDIO
A4	SDIO_D2_I2C1_SDA_PD12	IO	PU	No	No	GPD[12]	SDIO_D2	I2C1_SDA			VDDIO
C4	SDIO_D3_SSI0_CE0_PD13	IO	PU	No	No	GPD[13]	SDIO_D3	SSI0_CE0_			VDDIO
D1	MSC0_CLK_SFC0_CLK_SSI1_CLK_PD17	IO	PU	No	No	GPD[17]	MSC0_CLK	SFC0_CLK	SSI1_CLK		VDDIO
B1	MSC0_CMD_SFC0_CE_SSI1_DT_PD18	IO	PU	No	No	GPD[18]	MSC0_CMD	SFC0_CE_	SSI1_DT		VDDIO
C2	MSC0_D0_SFC0_DQ0_SSI1_DR_PD19	IO	PU	No	No	GPD[19]	MSC0_D0	SFC0_DQ0	SSI1_DR		VDDIO
C1	MSC0_D1_SFC0_DQ1_I2C2_SCK_PD20	IO	PU	No	No	GPD[20]	MSC0_D1	SFC0_DQ1	I2C2_SCK		VDDIO
D2	MSC0_D2_SFC0_DQ2_WP_I2C2_SDA_PD21	IO	PU	No	No	GPD[21]	MSC0_D2	SFC0_DQ2_WP_	I2C2_SDA		VDDIO
D4	MSC0_D3_SFC0_DQ3_HOLD_SSI1_CE0_PD22	IO	PU	No	No	GPD[22]	MSC0_D3	SFC0_DQ3_HOLD_	SSI1_CE0_		VDDIO
D3	MSC0_D4_SFC1_DQ0_UART0_RXD_PD23	IO	PU	No	No	GPD[23]	MSC0_D4	SFC1_DQ0	UART0_RXD		VDDIO
E4	MSC0_D5_SFC1_DQ1_UART0_TXD_PD24	IO	PU	No	No	GPD[24]	MSC0_D5	SFC1_DQ1	UART0_TXD		VDDIO
A1	MSC0_D6_SFC1_DQ2_WP_UART0_CTS_PD25	IO	PU	No	No	GPD[25]	MSC0_D6	SFC1_DQ2_WP_	UART0_CTS_		VDDIO
C3	MSC0_D7_SFC1_DQ3_HOLD_UART0_RTS_PD26	IO	PU	No	No	GPD[26]	MSC0_D7	SFC1_DQ3_HOLD_	UART0_RTS_		VDDIO
B4	UART2_RXD_I2C3_SCK_PWM0_TCU0_IN0_PD30	IO	PU	No	No	GPD[30]	UART2_RXD	I2C3_SCK	PWM0_TCU0_IN0		VDDIO
C5	UART2_TXD_I2C3_SDA_PWM1_TCU0_IN1_PD31	IO	PU	No	No	GPD[31]	UART2_TXD	I2C3_SDA	PWM1_TCU0_IN1		VDDIO

## 2.2.5 GPIO Group E

Ball No.	Ball Name	In/Out	Pull	Slew Rate	Schmitt	GPIO	Func0	Func1	Power
R10	MSC1_CLK_PWM2_TCU1_IN0_PE00	IO	PU	Yes	Yes	GPE[0]	MSC1_CLK	PWM2/TCU1_IN0	VDDIO33_SD
V10	MSC1_CMD_PWM3_TCU1_IN1_PE01	IO	PU	Yes	Yes	GPE[1]	MSC1_CMD	PWM3/TCU1_IN1	VDDIO33_SD
V9	MSC1_D0_PWM4_TCU2_IN0_PE02	IO	PU	Yes	Yes	GPE[2]	MSC1_D0	PWM4/TCU2_IN0	VDDIO33_SD
U9	MSC1_D1_PWM5_TCU2_IN1_PE03	IO	PU	Yes	Yes	GPE[3]	MSC1_D1	PWM5/TCU2_IN1	VDDIO33_SD
T9	MSC1_D2_PWM6_TCU3_IN0_PE04	IO	PU	Yes	Yes	GPE[4]	MSC1_D2	PWM6/TCU3_IN0	VDDIO33_SD
R9	MSC1_D3_PWM7_TCU3_IN1_PE05	IO	PU	Yes	Yes	GPE[5]	MSC1_D3	PWM7/TCU3_IN1	VDDIO33_SD
T10	SFC0_CLK_SSI1_CLK_PE16	IO	PU	No	Yes	GPE[16]	SFC0_CLK	SSI1_CLK	VDDIO33
U10	SFC0_CE_SSI1_DT_PE17	IO	PU	No	Yes	GPE[17]	SFC0_CE_	SSI1_DT	VDDIO33
T11	SFC0_DQ0_SSI1_DR_PE18	IO	PU	No	Yes	GPE[18]	SFC0_DQ0	SSI1_DR	VDDIO33
U11	SFC0_DQ1_I2C2_SCK_PE19	IO	PU	No	Yes	GPE[19]	SFC0_DQ1	I2C2_SCK	VDDIO33
V12	SFC0_DQ2_WP_I2C2_SDA_PE20	IO	PU	No	Yes	GPE[20]	SFC0_DQ2_WP_	I2C2_SDA	VDDIO33
U12	SFC0_DQ3_HOLD_SSI1_CE0_PE21	IO	PU	No	Yes	GPE[21]	SFC0_DQ3_HOLD_	SSI1_CE0_	VDDIO33
F4	DRV_VBUS_PE22	IO	PD	No	No	GPE[22]	DRV_VBUS		VDDIO
E2	RTC32K_PE23	IO	PD	No	No	GPE[23]	RTC32K		VDDIO
E3	EXCLK_CIM_VIC_MCLK_PE24	IO	PD	No	No	GPE[24]	EXCLK	CIM/VIC_MCLK	VDDIO
L4	BOOT_SEL0_PE25	IO	PD	No	No	GPE[25]	BOOT_SEL0		VDDIO
K4	BOOT_SEL1_PE26	IO	PD	No	No	GPE[26]	BOOT_SEL1		VDDIO
K2	BOOT_SEL2_PE27	IO	PD	No	No	GPE[27]	BOOT_SEL2		VDDIO

## 2.3 X2000/E Analog PAD DESCRIPTION

Table 2-1 X2000/E function pin description

Ball No.	Pin Names	IO	Power	Pin Description
<b>Debug</b>				
D6	TRST	I	VDDIO	JTAG reset
<b>Memory</b>				
A11	DDR_VDD1	P	DDR_VDD1	For sdram supply
B11	DDR_VDD1	P	-	For sdram supply
A12	DDRPLL_VCCA	P	-	DDR PHY PLL supply 1.8v
B12	DDR_VSSA	P	-	ground
A10	VREF	P		for sdram, reference voltage
C10	ZQ	I		for sdram, external reference resistor for output calibrating
<b>Power and Ground</b>				
A9	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
B8	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
B9	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
C8	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
C9	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
C12	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
C13	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
D12	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
D13	VDDMEM	P	-	DDR PHY LPDDR2/3 IO 1.2v supply
G6	VDDIO	P	-	GPIO 1.8v supply
H6	VDDIO	P	-	GPIO 1.8v supply
J13	VDDIO18	P	-	GPIO 1.8V supply for 3.3v PAD
N6	VDDIO18_CIM	P	-	CIM Type PAD1.8V supply
N8	VDDIO18_SD	P	-	Connect to 1uf capacity for SD type PAD

H13	VDDIO33	P	-	GPIO 3.3V supply for 3.3v PAD
N13	VDDIO33	P	-	GPIO 3.3V supply for 3.3v PAD
M6	VDDIO33_CIM	P	-	CIM GPIO 3.3V /1.8Vsupply
N9	VDDIO33_SD	P	-	SD GPIO 3.3V/1.8V supply
A8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
A13	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
B10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
B13	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
C7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
C11	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
D7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
D11	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F13	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
G7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
G10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
G13	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H9	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J7	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J11	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J12	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
K6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
K13	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
L6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V

L9	VSS	P	-	Core digital ground for none DRAM and CORE digital ground, 0V
L10	VSS	P	-	Core digital ground for none DRAM and CORE digital ground, 0V
L13	VSS	P	-	Core digital ground for none DRAM and CORE digital ground, 0V
F8	VDD	P	-	CORE digital power, 0.9V
F9	VDD	P	-	CORE digital power, 0.9V
F11	VDD	P	-	CORE digital power, 0.9V
F12	VDD	P	-	CORE digital power, 0.9V
G8	VDD	P	-	CORE digital power, 0.9V
G9	VDD	P	-	CORE digital power, 0.9V
G11	VDD	P	-	CORE digital power, 0.9V
G12	VDD	P	-	CORE digital power, 0.9V
H11	VDD	P	-	CORE digital power, 0.9V
H12	VDD	P	-	CORE digital power, 0.9V
K7	VDD	P	-	CORE digital power, 0.9V
K8	VDD	P	-	CORE digital power, 0.9V
K11	VDD	P	-	CORE digital power, 0.9V
K12	VDD	P	-	CORE digital power, 0.9V
L7	VDD	P	-	CORE digital power, 0.9V
L8	VDD	P	-	CORE digital power, 0.9V
L11	VDD	P	-	CORE digital power, 0.9V
L12	VDD	P	-	CORE digital power, 0.9V
M11	VDD	P	-	CORE digital power, 0.9V
M12	VDD	P	-	CORE digital power, 0.9V
<b>Audio Codec</b>				
U7	CODEC_AVDD	P	CODEC_AVDD	1.8v supply
R8	CODEC_AVSS	P		Ground
T7	CODEC_MICBIAS	AO	CODEC_AVDD	Electric microphone biasing voltage
T8	CODEC_HPOUTN	AO	CODEC_AVDD	DAC Differential output N
U8	CODEC_HPOUTP	AO	CODEC_AVDD	DAC Differential output P
U6	CODEC_MICLN	AI	CODEC_AVDD	ADC Differential input N end
V6	CODEC_MICLP	AI	CODEC_AVDD	ADC Differential input P end

V7	CODEC_VCM	AO	CODEC_AVDD	Referebce voltage output
<b>SADC</b>				
T3	AUX0	AI	SADC_AVDD	Analog input 0
V1	AUX1	AI	SADC_AVDD	Analog input 1
T2	AUX2	AI	SADC_AVDD	Analog input 2
U2	AUX3	AI	SADC_AVDD	Analog input 3
T1	AUX4	AI	SADC_AVDD	Analog input 4
U3	AUX5	AI	SADC_AVDD	Analog input 5
U1	SADC_VREFP	AI	SADC_AVDD	Positive reference voltage input
T4	SADC_AVSS	P		ground
V2	SADC_AVDD	P	SADC_AVDD	1.8v supply
<b>DSI</b>				
L17	TX_DATAN0	AO	DSI_AVD18	Lane0 negative end
K16	TX_DATAP0	AO	DSI_AVD18	Lane0 positive end
J18	TX_DATAN1	AO	DSI_AVD18	Lane1 negative end
J17	TX_DATAP1	AO	DSI_AVD18	Lane1 positive end
K18	TX_CLKN	AO	DSI_AVD18	CLK negative end
K17	TX_CLKP	AO	DSI_AVD18	CLK positive end
L15	DSI_AVSS	P		ground
L16	DSI_AVD09	P	DSI_AVD09	0.9V Analog supply
M16	DSI_AVD18	P	DSI_AVD18	1.8V Analog supply
<b>CSI</b>				
M18	RX_DATAN0	AI	CSI_AVD18	Lane0 negative end
M17	RX_DATAP0	AI	CSI_AVD18	Lane0 positive end
N18	RX_DATAN1	AI	CSI_AVD18	Lane1 negative end
N17	RX_DATAP1	AI	CSI_AVD18	Lane1 positive end
R17	RX_DATAN2	AI	CSI_AVD18	Lane2 negative end
R18	RX_DATAP2	AI	CSI_AVD18	Lane2 positive end
T18	RX_DATAN3	AI	CSI_AVD18	Lane3 negative end
T17	RX_DATAP3	AI	CSI_AVD18	Lane3 positive end
P17	RX_CLKN0	AI	CSI_AVD18	CLK lane0 negative end

N16	RX_CLKP0	AI	CSI_AVD18	CLK lane0 positive end
U17	RX_CLKN1	AI	CSI_AVD18	CLK lane1 negative end
U18	RX_CLKP1	AI	CSI_AVD18	CLK lane0 positive end
M15	CSI_AVSS	P		ground
N15	CSI_AVD09	P	CSI_AVD09	0.9V Analog supply
P16	CSI_AVD18	P	CSI_AVD18	1.8V Analog supply
<b>USB OTG</b>				
V3	USB_DP0(OTG_DP)	AIO	USB_AVD33	USB OTG data plus
U4	USB_DM0(OTG_DM)	AIO	USB_AVD33	USB OTG data minus
T5	USB_VBUS(OTG_VBUS)	AI	USB_AVD18	USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin
R6	USB_ID(OTG_ID)	AI	USB_AVD33	Used to identify the device attached to the PHY. The state of the pin is one of: high impedance ( $>1M\ \Omega$ ), or low impedance ( $<10\Omega$ to ground).
R7	USB_BIAS	AIO	USB_AVD09	Connect to 135 ohm +/- 1% resistor, all internal bias base on it
R5	USB_AVSS	P	-	USB analog ground
V4	USB_AVD09	P	USB_AVD09	USB analog power.0.9V
U5	USB_AVD18	P	USB_AVD18	USB analog power.1.8V
T6	USB_AVD33	P	USB_AVD33	USB analog power.3.3V
<b>EFUSE</b>				
D5	AVDEFUSE	P	AVEFUSE	EFUSE programming power, 0V/1.8V
<b>CPM</b>				
G2	OSC32_XI	AI	VDDRTC	RTC OSC input.
G1	OSC32_XO	AO	VDDRTC	RTC OSC output.
J1	EXCLK_XI	AI	VDDIO	EXCLK OSC Input
J2	EXCLK_XO	AO	VDDIO	EXCLK OSC Output
J3	PLL_VDD	P		PLL digital power
K3	PLL_VSS	P		PLL digital ground
H2	PLL_AVDD	P		PLL analog power
J4	PLL_AVSS	P		PLL analog ground
<b>RTC</b>				

F3	PWRON	O	VDDRTCIO	Power on/off control of main power
G3	PPRST_	I	VDDRTCIO	RTC power on reset and RESET-KY reset input
G4	TEST_TE	I	VDDRTCIO	Manufacture test enable, program readable
F1	VDDIO_RTC	P	VDDRTCIO	1.8v supply to RTC IO
H3	VDDR	P		0.9v supply to RTC
H4	VSSRTC	P		

## 2.4 X2000/E Digital PAD DESCRIPTION

Table 2-2 X2000/E Function Description

Signal Name	In/Out	Description
<b>SLCD(Smart LCD)</b>		
SLCD_D0	Output	Smart LCD data output bit 0
SLCD_D1	Output	Smart LCD data output bit 1
SLCD_D2	Output	Smart LCD data output bit 2
SLCD_D3	Output	Smart LCD data output bit 3
SLCD_D4	Output	Smart LCD data output bit 4
SLCD_D5	Output	Smart LCD data output bit 5
SLCD_D6	Output	Smart LCD data output bit 6
SLCD_D7	Output	Smart LCD data output bit 7
SLCD_D8	Output	Smart LCD data output bit 8
SLCD_D9	Output	Smart LCD data output bit 9
SLCD_D10	Output	Smart LCD data output bit 10
SLCD_D11	Output	Smart LCD data output bit 11
SLCD_D12	Output	Smart LCD data output bit 12
SLCD_D13	Output	Smart LCD data output bit 13
SLCD_D14	Output	Smart LCD data output bit 14
SLCD_D15	Output	Smart LCD data output bit 15

SLCD_RD	Output	Smart LCD read signal
SLCD_WR	Output	Smart LCD write signal
SLCD_CE_	Output	Smart LCD chip select signal
SLCD_TE	Input	Smart LCD tearing effect signal
SLCD_DC	Output	Smart LCD data/command select signal
<b>LCD</b>		
LCD_Dn	Output	LCD data output bit n
LCD_PCLK	Output	LCD pixel clock
LCD_VSYNC	Output	LCD frame sync
LCD_HSYNC	Output	LCD line sync
LCD_DE	Output	LCD data enable
<b>CIM(Camera Interface)</b>		
CIM_EXPOSURE	Output	CIM exposure signal to sensor to generate snapshot
CIM_VIC_PCLK	Input	CIM pixel clock input
CIM_VIC_HSYNC	Input	CIM line horizontal sync input
CIM_VIC_VSYNC	Input	CIM vertical sync input
CIM_VIC_MCLK	Output	CIM master clock output
VIC_D11	Input	CIM data input bit 11
VIC_D10	Input	CIM data input bit 10
VIC_D9	Input	CIM data input bit 9
VIC_D8	Input	CIM data input bit 8
CIM_VIC_D7	Input	CIM/VIC data input bit 7
CIM_VIC_D6	Input	CIM/VIC data input bit 6
CIM_VIC_D5	Input	CIM/VIC data input bit 5
CIM_VIC_D4	Input	CIM/VIC data input bit 4
CIM_VIC_D3	Input	CIM/VIC data input bit 3
CIM_VIC_D2	Input	CIM/VIC data input bit 2
CIM_VIC_D1	Input	CIM/VIC data input bit 1
CIM_VIC_D0	Input	CIM/VIC data input bit 0
<b>I2S</b>		
I2Sn_MCLK	Output	I2S n master clock out

I2Sn_BCLK	Bidirection	I2S n bit clock
I2Sn_LRCLK	Bidirection	I2S n LR clock
I2Sn_DI	Input	I2S n data input
I2Sn_DO	Output	I2S n data output
<b>PCM</b>		
PCM_CLK	Bidirection	PCM clock
PCM_DO	Output	PCM data out
PCM_DI	Input	PCM data in
PCM_SYN	Bidirection	PCM sync
<b>DMIC</b>		
DMIC_IN0	Input	Dmic data in for dmic 0/1
DMIC_IN1	Input	Dmic data in for dmic 2/3
DMIC_IN2	Input	Dmic data in for dmic 4/5
DMIC_IN3	Input	Dmic data in for dmic 6/7
DMIC_CLK	Output	Digital MIC clock output
<b>SFC</b>		
SFC0_CLK	Output	Serial Flash clock output
SFC0_CE_	Output	Serial Flash chip enable
SFCn_DQ0	Bidirection	Serial Flash data (n=0,1)
SFCn_DQ1	Bidirection	Serial Flash data
SFCn_DQ2_WP_	Bidirection	Serial Flash n write protect signal
SRCn_DQ3_HOLD_	Bidirection	Serial Flash n hold signal
<b>PWM</b>		
PWM0/TCU0_IN0	Bidirection	Pwm/tcu data output/input
PWM1/TCU0_IN1	Bidirection	Pwm/tcu data output/input
PWM2/TCU1_IN0	Bidirection	Pwm/tcu data output/input
PWM3/TCU1_IN1	Bidirection	Pwm/tcu data output/input
PWM4/TCU2_IN0	Bidirection	Pwm/tcu data output/input
PWM5/TCU2_IN1	Bidirection	Pwm/tcu data output/input
PWM6/TCU3_IN0	Bidirection	Pwm/tcu data output/input
PWM7/TCU3_IN1	Bidirection	Pwm/tcu data output/input

PWM8/TCU4_IN0	Bidirection	Pwm/tcu data output/input
PWM9/TCU4_IN1	Bidirection	Pwm/tcu data output/input
PWM10/TCU5_IN0	Bidirection	Pwm/tcu data output/input
PWM11/TCU5_IN1	Bidirection	Pwm/tcu data output/input
PWM12/TCU6_IN0	Bidirection	Pwm/tcu data output/input
PWM13/TCU6_IN1	Bidirection	Pwm/tcu data output/input
PWM14/TCU7_IN0	Bidirection	Pwm/tcu data output/input
PWM15/TCU7_IN1	Bidirection	Pwm/tcu data output/input
<b>RTC</b>		
RTC32K	Output	32768Hz clock output
<b>I2C</b>		
I2Cn_SCK	Bidirection	I2C n serial clock
I2Cn_SDA	Bidirection	I2C n serial data
<b>SCC</b>		
SCC_SCK	Bidirection	Smart Card clock
SCC_SDA	Bidirection	Smart Card data
<b>SSI</b>		
SSI <sub>n</sub> _CLK	Output	SSI n clock output
SSI <sub>n</sub> _CE0_	Output	SSI n chip enable 0
SSI <sub>n</sub> _DT	Output	SSI n data output
SSI <sub>n</sub> _DR	Input	SSI n data input
<b>UART</b>		
UART <sub>n</sub> _RXD	Input	UART n receiving data
UART <sub>n</sub> _TXD	Output	UART n transmitting data
UART <sub>n</sub> _CTS_	Input	UART Clear to send control
UART <sub>n</sub> _RTS_	Output	UART Request to send control
<b>MSC</b>		
MSC <sub>n</sub> _D7	Bidirection	MSC(MMC/SD) n data bit 7
MSC <sub>n</sub> _D6	Bidirection	MSC(MMC/SD) n data bit 6
MSC <sub>n</sub> _D5	Bidirection	MSC(MMC/SD) n data bit 5

MSCn_D4	Bidirection	MSC(MMC/SD) n data bit 4
MSCn_D3	Bidirection	MSC(MMC/SD) n data bit 3
MSCn_D2	Bidirection	MSC(MMC/SD) n data bit 2
MSCn_D1	Bidirection	MSC(MMC/SD) n data bit 1
MSCn_D0	Bidirection	MSC(MMC/SD) n data bit 0
MSCn_CLK	Output	MSC(MMC/SD) n clock output
MSCn_CMD	Bidirection	MSC(MMC/SD) n command
<b>USB 2.0 OTG</b>		
DRV_VBUS	Output	USB OTG VBUS driver control signal
<b>RGMAC</b>		
RGMACn_PHY_CLK	Output	Ethernet n PHY clock (50MHz) (n=0, 1)
RGMACn_RX_DV	Input	Rx data valid
RGMACn_RX_CLK	Input	Rx clk
RGMACn_RXD3	Input	receive data bit 3
RGMACn_RXD2	Input	receive data bit 2
RGMACn_RXD1	Input	receive data bit 1
RGMACn_RXD0	Input	receive data bit 0
RGMACn_TX_CLK	Output	Tx clk
RGMACn_TX_EN	Output	Ethernet n transmit enable
RGMACn_TXD3	Output	tx data bit 3
RGMACn_TXD2	Output	tx data bit 2
RGMACn_TXD1	Output	tx data bit 1
RGMACn_TXD0	Output	tx data bit 0
RGMACn_MDC	Output	Ethernet n management clock
RGMACn_MDIO	Bidirection	Ethernet n management data
<b>NEMC</b>		
SAn	Output	Nemc Address (n=12)
SDn	Bidirection	Nemc Data (n=16)
RD_	Output	Nemc read enable, low active
WE_	Output	Nemc write enable, low active
NEMC_CS1_	Output	Nemc chip select1

NEMC_CS2	Output	Nemc chip select2
WAIT_	Input	Nemc wait for external memory
<b>DEBUG</b>		
TDO	Output	JTAG serial data output
TDI	Input	JTAG serial data input
TCK	Input	JTAG clock
TMS	Input	JTAG mode select

**NOTES:**

- 1 The meaning of phases in IO cell characteristics are:
  - a PU: The IO cell contains a pull-up resistor.
  - b PD: The IO cell contains a pull-down resistor.
  - c Schmitt: The IO cell is Schmitt trig input.
- 2 All GPIO shared pins are reset to GPIO input.

# 3 Electrical Specifications

## 3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

**Table 3-1 Absolute Maximum Ratings**

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDDMEM power supplies voltage	-0.3	1.32	V
DDR_VDD1 power supplies voltage	-0.5	1.98	V
DDRPLL power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	1.98	V
VDDIO33 power supplies voltage	-0.5	3.63	V
VDDIO18 power supplies voltage	-0.5	1.98	V
VDDIO33_CIM power supplies voltage	-0.5	3.63	V
VDDIO18_CIM power supplies voltage	-0.5	1.98	V
VDDIO33_SD power supplies voltage	-0.5	3.63	V
VDD core power supplies voltage	-0.2	1.1	V
PLLVDD power supplies voltage	-0.2	1.1	V
PLLAVID power supplies voltage	-0.5	1.98	V
AVDEFUSE power supplies voltage	-0.5	1.98	V
VDDIORTC power supplies voltage	-0.5	1.98	
VDDRTC power supplies voltage	-0.2	1.1	V
USB_AVD33 power supplies voltage	-0.5	3.6	V
USB_AVD18 power supplies voltage	-0.5	1.98	
USB_AVD09 power supplies voltage	-0.2	1.1	V
CODEC_AVDD power supplies voltage	-0.5	1.98	V
SADC_AVDD	-0.5	1.98	
CSI_AVD18	-0.5	1.98	
CSI_AVD09	-0.2	1.1	
DSI_AVD18	-0.5	1.98	
DSI_AVD09	-0.2	1.1	
Input voltage to VDDMEM supplied non-supply pins	-0.3	1.32	V
Input voltage to VDDIO supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO33 supplied non-supply pins	-0.3	3.6	V
Input voltage to VDDIO33_CIM supplied non-supply pins	-0.3	3.6	
Input voltage to VDDIO33_SD supplied non-supply pins	-0.3	3.6	
Input voltage to VDDIORTC supplied non-supply pins	-0.3	1.98	V
Input voltage to USB_AVD33 supplied non-supply pins	-0.3	3.6	V
Input voltage to CODEC_AVDD supplied non-supply pins	-0.3	1.98	V
Input voltage to SADC_AVDD supplied non-supply pins	-0.3	1.98	V
Input voltage to CSI_AVD18 supplied non-supply pins	-0.3	1.98	
Output voltage from VDDMEM supplied non-supply pins	-0.3	1.32	
Output voltage from VDDIO supplied non-supply pins	-0.3	1.98	V
Output voltage from VDDIO33 supplied non-supply pins	-0.3	3.6	V
Output voltage from VDDIO33_CIM supplied non-supply pins	-0.3	3.6	V

Output voltage from VDDIO18_CIM supplied non-supply pins	-0.3	1.98	
Output voltage from VDDIORTC supplied non-supply pins	-0.3	1.98	V
Output voltage from USB_AVD33 supplied non-supply pins	-0.3	3.6	V
Output voltage from CODEC_AVDD supplied non-supply pins	-0.3	1.98	V
Output voltage from DSI_AVD18 supplied non-supply pins	-0.3	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

### 3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for LPDDR3	1.14	1.2	1.3	V
	VDDMEM voltage for LPDDR2	1.08	1.2	1.32	V
VDDR	DDR_VDD1 voltage	1.7	1.8	1.95	V
VDDRPLL	DDRPLL voltage	1.62	1.8	1.98	V
VIO(1.8V)	VDDIO voltage	1.71	1.8	1.89	V
VIO18	VDDIO18 voltage	1.71	1.8	1.89	V
VIO33	VDDIO33 voltage	3.135	3.3	3.465	V
VCIM33(3.3V)	VDDIO33_CIM voltage, use as 3.3V	3.135	3.3	3.465	V
VCIM33(1.8V)	VDDIO33_CIM voltage, use as 1.8V	1.71	1.8	1.89	
VCIM18	VDDIO18_CIM voltage	1.71	1.8	1.89	V
VSD33(3.3V)	VDDIO33_SD voltage, use as 3.3V	3.135	3.3	3.465	V
VSD33(1.8V)	VDDIO33_SD voltage, use as 1.8V	1.71	1.8	1.89	V
VCORE	VDD core voltage	0.9	0.9	1	V
VLPLLVDD	PLLVDD voltage	0.9	0.9	1	V
VLPLLAVIDD	PLLAVIDD voltage	1.71	1.8	1.89	
VEFUSE	AVDEFUSE voltage	1.71	1.8	1.89	V
VRTCIO18	VDDIORTC voltage	1.71	1.8	1.89	V
VRTC	VDDRTC voltage	0.9	0.9	1	
VUSB33	USB_AVD33 voltage	3.135	3.3	3.465	V
VUSB18	USB_AVD18 voltage	1.71	1.8	1.89	
VUSB09	USB_AVD09 voltage	0.9	0.9	1	V
VCDC	CODEC_AVDD voltage	1.71	1.8	1.89	V
VADC	SADC_AVDD voltage	1.71	1.8	1.89	V
VCSI18	CSI_AVD18 voltage	1.62	1.8	1.98	V
VCSI09	CSI_AVD09 voltage	0.9	0.9	1	V
VDSI18	DSI_AVD18 voltage	1.71	1.8	1.89	V
VDSI09	DSI_AVD09 voltage	0.9	0.9	1	V

Table 3-3 Recommended operating conditions for  
VDDIO/VDDIO33/VDDIO33\_SD/VDDIO33\_CIM/VDDIO33\_SD/VDDIORTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VIH18	Input high voltage for 1.8V I/O application	1.17	1.8	1.98	V
VIL18	Input low voltage for 1.8V I/O application	-0.3	0	0.63	V
VIH33	Input high voltage for 3.3V I/O application	2.0	3.3	3.465	V
VIL33	Input low voltage for 3.3V I/O application	-0.3	0	0.8	V

**Table 3-4 Recommended operating conditions for others**

Symbol	Description	Min	Typical	Max	Unit
TA	Ambient temperature	-40		85	°C

### 3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

**Table 3-5 DC characteristics for VREF**

Symbol	Parameter	Min	Typical	Max	Unit
VREF	Reference voltage supply	0.49	0.5	0.51	VMEM

**Table 3-6 DC characteristics for VDDIO/VDDIORTC supplied pins for 1.8V application**

Symbol	Parameter	Min	Typical	Max	Unit
$V_T$	Threshold point	0.82	0.89	0.97	V
$V_{T+}$	Schmitt trig low to high threshold point	0.96	1.03	1.1	V
$V_{T-}$	Schmitt trig high to low threshold point	0.64	0.75	0.86	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	0.81	0.88	0.97	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	0.82	0.89	0.98	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	0.95	1.02	1.09	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	0.63	0.75	0.85	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	0.96	1.05	1.11	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	0.65	0.76	0.86	V
$I_L$	Input Leakage Current @ $V_I=1.8V$ or 0V			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $V_I=1.8V$ or 0V			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	60	89	137	k $\Omega$
$R_{PD}$	Pull-down Resistor	61	104	196	k $\Omega$
$V_{OL}$	Output low voltage			0.45	V
$V_{OH}$	Output high voltage	1.35			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	11.1	18.2	25.6	mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	13.1	19.1	26.2	mA

**Table 3-7 DC characteristics for VDDIO33\_SD supplied pins for 1.8V application**

<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Typical</b>	<b>Max</b>	<b>Unit</b>
$V_T$	Threshold point	0.76	0.94	1.24	V
$V_{T+}$	Schmitt trig low to high threshold point	0.94	1.09	1.36	V
$V_{T-}$	Schmitt trig high to low threshold point	0.68	0.89	1.2	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	0.74	0.92	1.22	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	0.76	0.95	1.25	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	0.93	1.07	1.34	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	0.66	0.88	1.18	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	0.95	1.1	1.388	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	0.68	0.9	1.22	V
$I_L$	Input Leakage Current @ $V_i=1.8V$ or 0V			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $V_i=1.8V$ or 0V			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	33	59	91	k $\Omega$
$R_{PD}$	Pull-down Resistor	34	61	108	k $\Omega$
$V_{OL}$	Output low voltage			0.4	V
$V_{OH}$	Output high voltage	2.475			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	(DS2,DS1,DS0) = 000	4.5	7.7	11.3 mA
		(DS2,DS1,DS0) = 001	6.7	11.4	16.7 mA
		(DS2,DS1,DS0) = 010	9	15.2	22.1 mA
		(DS2,DS1,DS0) = 011	11.2	18.8	27.3 mA
		(DS2,DS1,DS0) = 100	13.4	22.6	32.7 mA
		(DS2,DS1,DS0) = 101	15.6	26.2	37.8 mA
		(DS2,DS1,DS0) = 110	17.7	29.7	42.8 mA
		(DS2,DS1,DS0) = 111	19.9	33.2	47.7 mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	(DS2,DS1,DS0) = 000	2.6	6.3	11.9 mA
		(DS2,DS1,DS0) = 001	3.8	9.4	17.7 mA
		(DS2,DS1,DS0) = 010	5.1	12.6	23.7 mA
		(DS2,DS1,DS0) = 011	6.4	15.7	29.4 mA
		(DS2,DS1,DS0) = 100	7.6	18.8	35.2 mA
		(DS2,DS1,DS0) = 101	8.9	21.8	40.9 mA
		(DS2,DS1,DS0) = 110	10.1	24.9	46.6 mA
		(DS2,DS1,DS0) = 111	11.4	27.9	52.2 mA

**Table 3-8 DC characteristics for VDDIO33\_SD supplied pins for 3.3V application**

<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Typical</b>	<b>Max</b>	<b>Unit</b>
$V_T$	Threshold point	1.39	1.5	1.65	V
$V_{T+}$	Schmitt trig low to high threshold point	1.62	1.75	1.9	V
$V_{T-}$	Schmitt trig high to low threshold point	1.18	1.29	1.44	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	1.36	1.48	1.64	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	1.4	1.52	1.66	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	1.62	1.75	1.89	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	1.16	1.28	1.43	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	1.64	1.77	1.91	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	1.19	1.31	1.45	V
$I_L$	Input Leakage Current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	34	51	81	k $\Omega$
$R_{PD}$	Pull-down Resistor	35	51	88	k $\Omega$
$V_{OL}$	Output low voltage			0.4	V
$V_{OH}$	Output high voltage	2.4			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	(DS2,DS1,DS0) = 000	2.8	5.4	9.8 mA
		(DS2,DS1,DS0) = 001	4.1	8.0	14.6 mA
		(DS2,DS1,DS0) = 010	5.5	10.7	19.4 mA
		(DS2,DS1,DS0) = 011	6.8	13.2	23.9 mA
		(DS2,DS1,DS0) = 100	8.2	15.9	28.7 mA
		(DS2,DS1,DS0) = 101	9.6	18.4	33.2 mA
		(DS2,DS1,DS0) = 110	10.9	20.9	37.6 mA
		(DS2,DS1,DS0) = 111	12.2	23.4	42.0 mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	(DS2,DS1,DS0) = 000	4.4	7.6	13.5 mA
		(DS2,DS1,DS0) = 001	6.6	11.4	20.2 mA
		(DS2,DS1,DS0) = 010	8.8	15.2	26.9 mA
		(DS2,DS1,DS0) = 011	10.9	18.9	33.5 mA
		(DS2,DS1,DS0) = 100	13.1	22.6	40.1 mA
		(DS2,DS1,DS0) = 101	15.2	26.3	46.7 mA
		(DS2,DS1,DS0) = 110	17.4	30.1	53.3 mA
		(DS2,DS1,DS0) = 111	19.6	23.7	59.7 mA

Table 3-9 DC characteristics for VDDIO33/VDDIO18 supplied pins for 3.3V application

Symbol	Parameter	Min	Typical	Max	Unit
$V_T$	Threshold point	1.02	1.17	1.36	V
$V_{T+}$	Schmitt trig low to high threshold point	1.22	1.34	1.5	V
$V_{T-}$	Schmitt trig high to low threshold point	0.96	1.13	1.33	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	1	1.15	1.34	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	1.03	1.19	1.38	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	1.21	1.32	1.47	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	0.94	1.1	1.3	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	1.23	1.35	1.52	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	0.97	1.14	1.34	V
$I_L$	Input Leakage Current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	26	46	71	$k\Omega$
$R_{PD}$	Pull-down Resistor	27	48	103	$k\Omega$
$V_{OL}$	Output low voltage			0.4	V
$V_{OH}$	Output high voltage	2.4			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	(DS2,DS1,DS0) = 000	4	6.3	8.9 mA
		(DS2,DS1,DS0) = 001	6	9.4	13.3 mA
		(DS2,DS1,DS0) = 010	8	12.5	17.6 mA
		(DS2,DS1,DS0) = 011	9.9	15.5	21.8 mA
		(DS2,DS1,DS0) = 100	11.9	18.6	26.1 mA
		(DS2,DS1,DS0) = 101	13.9	21.6	30.2 mA
		(DS2,DS1,DS0) = 110	15.8	24.5	34.2 mA
		(DS2,DS1,DS0) = 111	17.7	27.4	38.1 mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	(DS2,DS1,DS0) = 000	5.9	9.3	14.2 mA
		(DS2,DS1,DS0) = 001	8.8	13.9	21.2 mA
		(DS2,DS1,DS0) = 010	11.7	18.5	28.2 mA
		(DS2,DS1,DS0) = 011	14.6	23.1	35.2 mA
		(DS2,DS1,DS0) = 100	17.5	27.7	42.2 mA
		(DS2,DS1,DS0) = 101	20.3	32.2	49.1 mA
		(DS2,DS1,DS0) = 110	23.2	36.8	56 mA
		(DS2,DS1,DS0) = 111	26.1	41.3	62.8 mA

**Table 3-10 DC characteristics for VDDIO33\_CIM/VDDIO18\_CIM supplied pins for 3.3V application**

Symbol	Parameter	Min	Typical	Max	Unit
$V_T$	Threshold point	0.76	0.94	1.24	V
$V_{T+}$	Schmitt trig low to high threshold point	0.94	1.09	1.37	V
$V_{T-}$	Schmitt trig high to low threshold point	0.68	0.89	1.21	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	0.74	0.93	1.22	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	0.76	0.95	1.26	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	0.93	1.08	1.34	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	0.67	0.88	1.18	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	0.95	1.1	1.38	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	0.68	0.9	1.22	V
$I_L$	Input Leakage Current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $VI=1.8V$ or $0V$			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	33	59	91	$k\Omega$
$R_{PD}$	Pull-down Resistor	34	61	108	$k\Omega$
$V_{OL}$	Output low voltage			0.4	V
$V_{OH}$	Output high voltage	2.4			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	$(DS1,DS0) = 00$	2.8	5.4	9.8 mA
		$(DS1,DS0) = 01$	4.1	8.0	14.6 mA
		$(DS1,DS0) = 10$	5.5	10.6	19.3 mA
		$(DS1,DS0) = 11$	6.8	13.2	23.8 mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	$(DS1,DS0) = 00$	4.4	7.6	13.5 mA
		$(DS1,DS0) = 01$	6.6	11.4	20.2 mA
		$(DS1,DS0) = 10$	8.8	15.2	26.9 mA
		$(DS1,DS0) = 11$	10.9	18.9	33.6 mA

**Table 3-11 DC characteristics for VDDIO33\_CIM/VDDIO18\_CIM supplied pins for 1.8V application**

Symbol	Parameter	Min	Typical	Max	Unit
$V_T$	Threshold point	0.85	0.95	1.08	V
$V_{T+}$	Schmitt trig low to high threshold point	0.97	1.06	1.17	V
$V_{T-}$	Schmitt trig high to low threshold point	0.7	0.82	0.94	V
$V_{TPU}$	Threshold point with pull-up resistor enabled	0.85	0.95	1.07	V
$V_{TPD}$	Threshold point with pull-down resistor enabled	0.86	0.96	1.09	V
$V_{TPU+}$	Schmitt trig low to high threshold point with pull-up resistor enabled	0.97	1.06	1.16	V
$V_{TPU-}$	Schmitt trig high to low threshold point with pull-down resistor enabled	0.69	0.81	0.93	V
$V_{TPD+}$	Schmitt trig low to high threshold point with pull-down resistor enabled	0.98	1.07	1.18	V
$V_{TPD-}$	Schmitt trig high to low threshold point with pull-up resistor enabled	0.7	0.82	0.95	V
$I_L$	Input Leakage Current @ $VI=1.8V$ or 0V			$\pm 10$	$\mu A$
$I_{OZ}$	Tri-State output leakage current @ $VI=1.8V$ or 0V			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor	33	59	90	$k\Omega$
$R_{PD}$	Pull-down Resistor	34	61	95	$k\Omega$
$V_{OL}$	Output low voltage			0.45	V
$V_{OH}$	Output high voltage	1.4			V
$I_{OL}$	Low level output current @ $V_{OL}(\max)$	(DS1,DS0) = 00	4.5	7.6	11.2 mA
		(DS1,DS0) = 01	6.7	11.4	16.6 mA
		(DS1,DS0) = 10	8.9	15.1	22 mA
		(DS1,DS0) = 11	11.1	18.7	27.2 mA
$I_{OH}$	High level output current @ $V_{OH}(\min)$	(DS1,DS0) = 00	2.6	6.3	11.9 mA
		(DS1,DS0) = 01	3.8	9.5	17.8 mA
		(DS1,DS0) = 10	5.1	12.6	23.7 mA
		(DS1,DS0) = 11	6.4	15.7	29.4 mA

### 3.4 Audio codec

Measurement conditions: $T = 25^\circ\text{C}$ , AVDD = 1.8 V, DVDD = 0.9V, 1KHz Sine Input, FS = 48KHZ					
Parameter	Test conditions	Min.	Type	Max.	Unit
Analog Supply		1.62	1.8	1.98	V
Digital Supply		0.81	0.9	0.99	V
Temperature		-40		125	°C
ADC					
SNR	A-weighted		92		
THD			-81		
Bias Voltage		0.5*A VDD		0.85*AV DD	V
Bias Current				3	mA
Mic Gain		0		20	dB
ALC Gain		-18		28.5	dB
Gain Step Size			1.5		dB
input Resistance		8		88	kΩ
input Capacitance			10		pF
DAC					
SNR	A-weighted		93		dB
THD	60mWΩ		-70		dB
	30mWΩ		-75		dB
	600Ω		-80		dB
Programmable Gain		-39		6	dB
Gain Step Size			1.5		
Output Resistance				1	Ω
Output Capacitance			20		pF
Power Supply Rejection	1KHZ		55		dB
Power Consumption					
Standby			0.1		mA

## 3.5 Power On, Reset and BOOT

### 3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X2000/E processor with a specific sequence of power and reset to ensure proper operation. Figure 3-1 shows this sequence and Table 3-12 gives the timing parameters. Following are the name of the power.

VDDIORTC: VDDIORTC

VDDRRTC: VDDRRTC

VDDIO18: all other 1.8V power supplies, include VDDIO, VDDIO18, PLLAVDD, VDDIO18\_CIM, CSI\_AVD18, DSI\_AVD18, USB\_AVD18, CODEC\_AVDD, SADC\_AVDD, DDRPLL, DDR\_VDD1

VMEM: VDDMEM

VDDIO33: all 3.3V power supplies, include VDDIO33, VDDIO33\_CIM, VDDIO33\_SD,

AVDUSB33

VDD: all other 0.9V power supplies: VDD, PLLVDD, DSI\_AVD09, CSI\_AVD09, USB\_AVD09

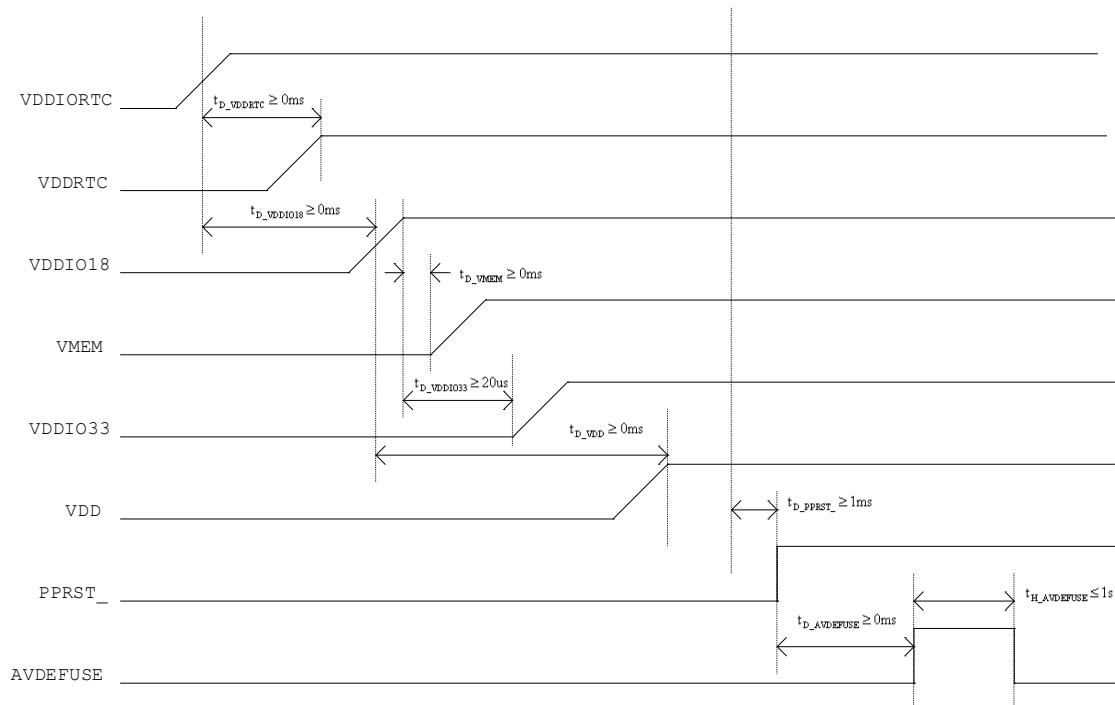
AVDEFUSE: AVDEFUSE

**Table 3-12 Power-On Timing Parameters**

Symbol	Parameter	Min	Max	Unit
$t_{D\_VDDRRTC}$	Delay between VDDIORTC arriving 50% to VDDRRTC arriving 90% <sup>[1]</sup>	0	–	ms
$t_{D\_VDDIO18}$	Delay between VDDIORTC arriving 50% to VDDIO18 arriving 50% <sup>[1]</sup>	0	–	ms
$t_{D\_VMEM}$	Delay between VDDIO18 arriving 90% to VMEM to be turned on	0	–	ms
$t_{D\_VDDIO33}$	Delay between VDDIO18 arriving 90% to VDDIO33 to be turned on	20	–	us
$t_{D\_VDD}$	Delay between VDDIO18 arriving 50% to VDD arriving 90% <sup>[1]</sup>	0	–	ms
$t_{D\_PPRST\_}$	Delay between all power rails get stable and power-on reset PPRST_ de-asserted <sup>[2]</sup>	TBD <sup>[3]</sup>	–	ms <sup>[2]</sup>
$t_{D\_AVDEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms
$t_{H\_AVDEFUSE}$	E-fuse programming time	–	1	s

**NOTES:**

- 1 The power rails have same skew.
- 2 The PPRST\_ must be kept at least 1ms. After PPRST\_ is deasserted, the corresponding chip reset will be extended at least 10ms.
- 3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.



**Figure 3-1 Power-On Timing Diagram**

### 3.5.2 Reset procedure

There 3 reset sources: 1 PPRST\_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

#### 1 PPRST\_ pin reset.

This reset is triggered when PPRST\_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 10ms (512 clock whose frequency is exclk/512) after rising edge of PPRST\_.

#### 2 WDT reset.

This reset happens in case of WDT timeout.

#### 3 Hibernating reset.

This reset happens in case of wakeup the main power from power down. The reset keeps for about 125ms as default and can be programmed up to 1s, plus 10ms (512 clock whose frequency is exclk/512), start after WKUP\_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function, except JTAG relate TCK/TMS/TDI /TDO which reset to function mode, and most of their internal pull-up/down resistor are set to on. The PWRON is output 1. The oscillators are on.

### 3.5.3 BOOT

The boot sequence of the X2000/E is controlled by boot\_sel [2:0], GPIO PE27/26/25 PAD

**Table 3-13 Boot Configuration of X2000/E**

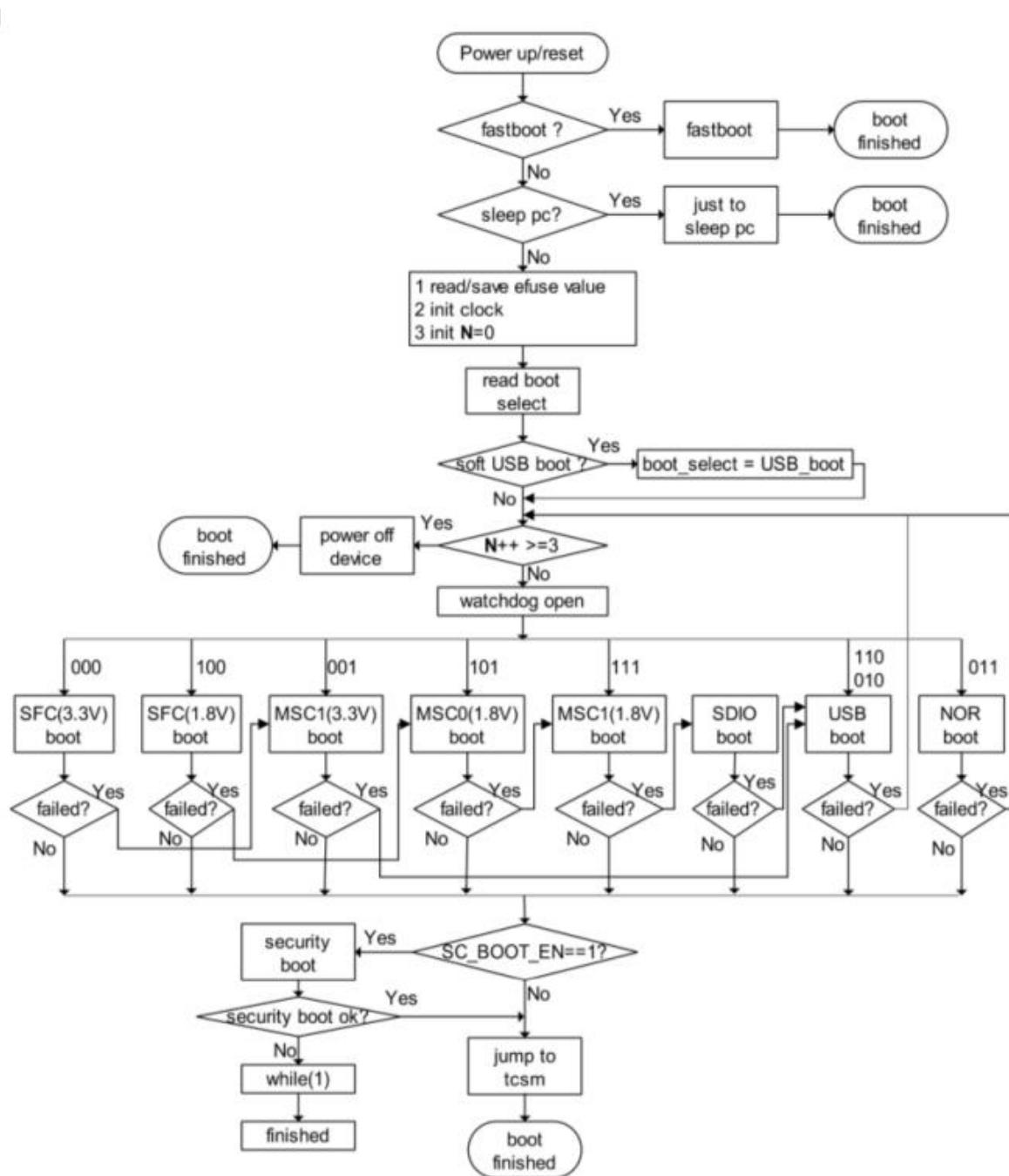
boot_sel[2]	boot_sel[1]	boot_sel[0]	Boot configuration
0	0	0	SFC0@PE 3.3v
0	0	1	MSC1@PE 3.3v
X	1	0	USB
0	1	1	Nor
1	0	0	SFC0@PD 1.8v
1	0	1	MSC0@PD 1.8v
1	1	1	MSC1@PE 1.8v

X: means "Don't Care"

After reset, the boot program on the internal boot ROM executes as follows:

- 1 Disable all interrupts, prepare the program running environment.
- 2 Read and save efuse values, efuse values to determine whether to improve system clock frequency, set MSC 4bit transmission data, gpio HI-Z, USB eye diagram.
- 3 Initialize clock and read boot\_sel[2:0] to determine the boot method.
- 4 If it is boot from MMC/SD card at MSC0/MSC2, its function pins MSC\_D0, MSC\_CLK, MSC\_CMD are initialized, the boot program loads the 24KB data from MMC/SD card to SRAM and jump to it. Only one data bus which is MSC\_D0 is used. The clock EXTCLK/122 is used initially. When reading data, the clock EXTCLK/4 is used. If the msc\_bus\_width\_4 efuse values is set to 1, function pins MSC\_D0, MSC\_D1, MSC\_D2, MSC\_D3 are initialized for 4bit data transmission.
- 5 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.
- 6 If it is boot from SPI nor/nand at SFC, its function pins SFC\_CLK, SFC\_CE, SFC\_DR, SFC\_DT, SFC\_WP, SFC\_HOL are initialized, the boot program loads the spl size bytes code from nor/nand to SRAM and jump to it.

**NOTE:** The X2000/E's SRAM is 32KB, its address is from 0xB2400000 to 0xB2408000.

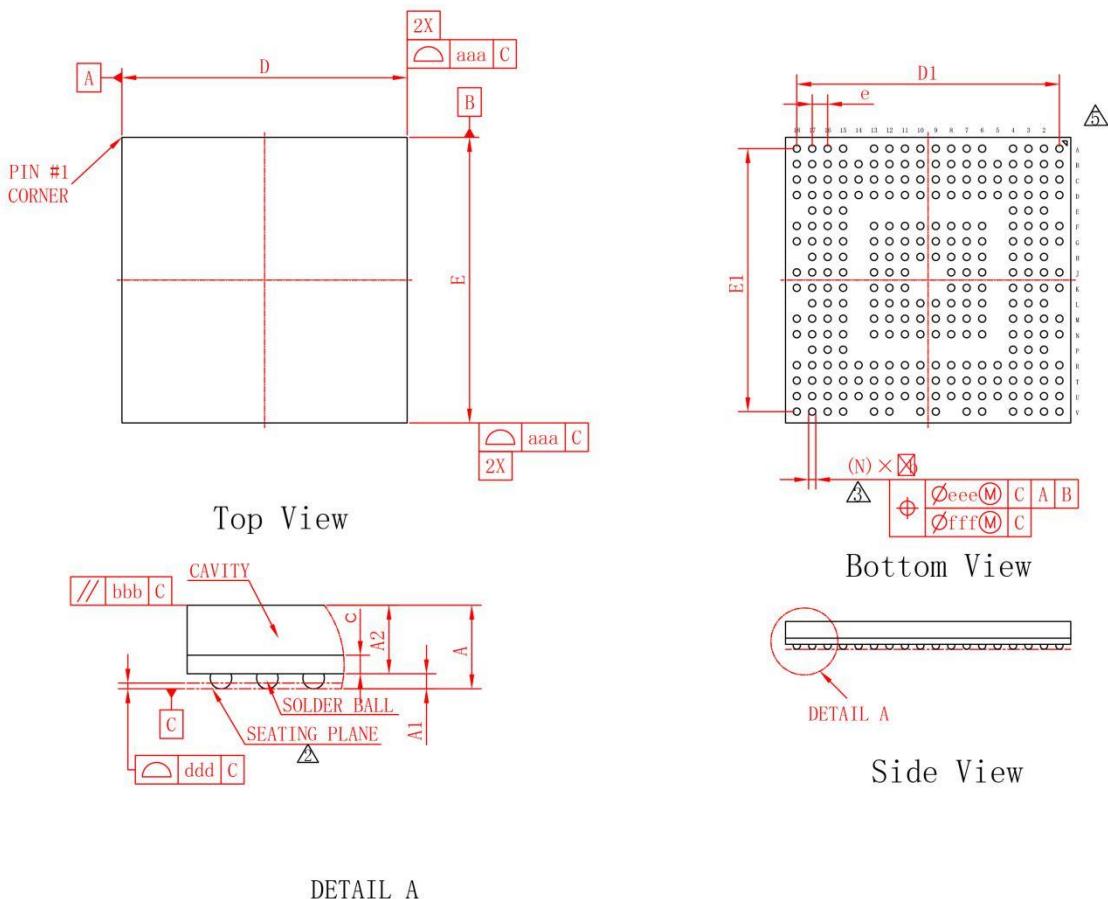


# 4 Packaging Information

## 4.1 Overview

X2000/E processor is offered in 270-pin BGA package, which is 12mm x 12mm x 1.2mm outline, 18 x 18 matrix ball grid array and 0.65mm ball pitch, show in Figure 4-1.

## 4.2 Device Dimensions



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.270	---	---	0.050
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.220	0.260	0.300	0.009	0.010	0.012
D	11.900	12.000	12.100	0.469	0.472	0.476
E	11.900	12.000	12.100	0.469	0.472	0.476
D1	---	11.050	---	---	0.435	---
E1	---	11.050	---	---	0.435	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	270			270		
MD/ME	18/18			18/18		

**Figure 4-1 X2000/E package outline drawing**

Notes:

1. BALL PAD OPENING: 0.270mm;
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C;
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd;
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;

### 4.3 Solder Ball Materials

Both the top (joint) and bottom solder ball materials of X2000/E are SAC125.

### 4.4 Moisture Sensitivity Level

X2000/E package moisture sensitivity is level 3.