1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consump-tion and high noise immunity. On chip memory inclu-des 1K words of ROM, and 41 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- Fully COMS static design
- 8-bit data bus
- On chip EPROM size : 1 K words
- Internal RAM size : 41 bytes
- 36 single word instructions
- 14-bit instructions
- 2-level stacks
- Operating voltage : 2.5 V ~ 5.0 V
- Operating frequency : 4 MHz or 8 MHz
- The most fast execution time is 500 ns under 8 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Sleep Mode for power saving
- Oscillator mode:
  INTRC－Internal 4/8 MHz RC oscillator
- Power on start-up time : 20 ms
- 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
- On-chip RC oscillator based Watchdog Timer(WDT)
- Wake-up from sleep on pin change

3. Applications

The application areas of this P509(A) range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC pe-ripheral … etc.

4. Pin Assignment

P509ST2621

PB0	1	6	PB3
VSS	2	5	VDD
PB1	3	4	PB2/RTCC

P509ST2623

PB0	1	6	/MCLR
VSS	2	5	VDD
PB1	3	4	PB2/RTCC

P509P11/S11/TSS11

VDD	1	8	VSS
PB5	2	7	PB0
PB4	3	6	PB1
PB3	4	5	PB2/RTCC

P509P13/S13/TSS13

VDD	1	8	VSS
PB5	2	7	PB0
PB4	3	6	PB1
/MCLR	4	5	PB2/RTCC

5. Pin Function Description

Pin Name	I/O	Function Description
PB0,PB1,PB3~PB5	I/O	Port B, TTL input level, PB3 input only.
RTCC/PB2	I/O	Real Time Clock/Counter, Schmitt Trigger input levels.
/MCLR	I	Master Clear, Schmitt Trigger input levels.
VDD		Power supply
VSS		Ground

6. Memory Map

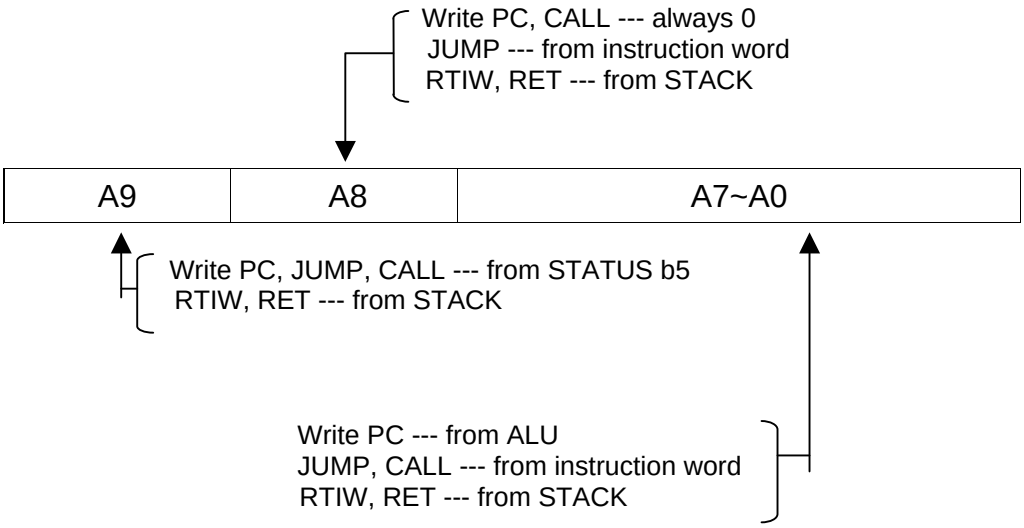
(A) Register Map

Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS
04	MSR
05	OSCCON
06	Port B
07~1F	General purpose registers
BANK1	
30~3F	General purpose registers

(1) IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

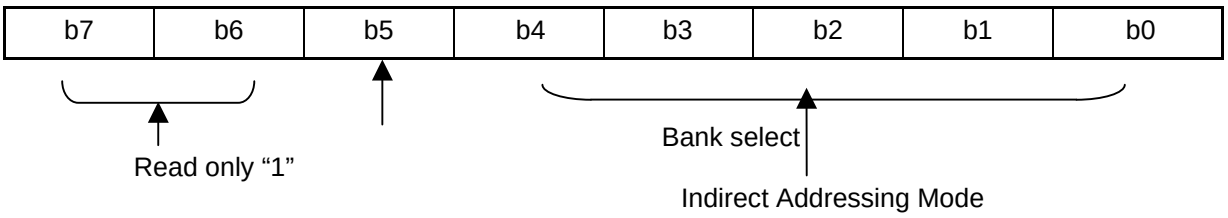
(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down bit
4	TF	WDT Timer overflow Flag bit
5	PAGE	ROM page select bit
6	——	Unimplemented
7	PCWUF	Pin change wake up from sleep

(5) MSR (Memory Bank Select Register) : R4



(6)OSCCON : R5 use CPIO instructions

Bit	Symbol	Function		
0	PUGP2	PB2 Pull-High Set Bit 1=Enable 0=Disable		
1	PUGP3*	PB3 Pull-High Set Bit When PBPHB=1 , 1=Enable 0=Disable (Power on Mode) When PBPHB=0 , 0=Enable 1=Disable		
2	PUGP4**	PB4 Pull-High Set Bit 1=Enable 0=Disable		
3	PUGP5**	PB5 Pull-High Set Bit 1=Enable 0=Disable		
6—4	IRCS2—0	Value	4 MHz INTRC	8 MHz INTRC
		0 0 0	15 KHz	31 KHz
		0 0 1	62 KHz	125 KHz
		0 1 0	125 KHz	250 KHz
		0 1 1	250 KHz	500 KHz
		1 0 0	500 KHz	1 MHz
		1 0 1	1 MHz	2 MHz
		1 1 0	2 MHz	4 MHz
		1 1 1	4 MHz	8 MHz
7	PUGP1*	PB1 Pull-High Set Bit When PBPHB=1 , 1=Enable 0=Disable (Power on Mode) When PBPHB=0 , 0=Enable 1=Disable		

Note1 * :

PB0 pull high	PB1 pull high	PB3 pull high	
enable	enable	enable	PBPHB=0,PUGP1=0,PUGP3=0
enable	enable	disable	PBPHB=0,PUGP1=0,PUGP3=1
enable	disable	enable	PBPHB=0,PUGP1=1,PUGP3=0
enable	disable	disable	PBPHB=0,PUGP1=1,PUGP3=1
disable	enable	enable	PBPHB=1,PUGP1=1,PUGP3=1
disable	enable	disable	PBPHB=1,PUGP1=1,PUGP3=0
disable	disable	enable	PBPHB=1,PUGP1=0,PUGP3=1
disable	disable	disable	PBPHB=1,PUGP1=0,PUGP3=0

Note2 * : PUGP5~3 don’t set “1” at the same time

(7) PORT B : R6

PB5~PB0, I/O Register, PB3 input only.

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		
6	PBPHB	PB0/PB1/PB3 pull-high : 0 — Enable 1 — Disable		
7	PBWUB	PB0~PB5 wake-up : 0 — Enable 1 — Disable		

(9) CPIO B (Control Port I/O Mode Register)
The CPIO register is “write-only”
＝“0”, I/O pin in output mode;
＝“1”, I/O pin in input mode.

(10) Configurable options for EPROM (Set by writer) :

Oscillator Frequency
4 MHz
8 MHz

Oscillator Type	Oscillator Start-up Time
INTRC Oscillator	20ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-edge Detect
PED Disable
PED Enable (1.8V / 1.8V always enable / 2.1V always enable)

Security state
Security Disable
Security Enable

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.

8. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR Reset	WDT Reset
IAR	00h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	02h	0000 0000	0000 0000	0000 0000
STATUS	03h	0001 1xxx	#00# #uuu	#00# #uuu
MSR	04h	111x xxxx	110u uuuu	11uu uuuu
OSCCON	05h	0111 0000	0111 0000	0111 0000
PORT B	06h	--xx xxxx	--uu uuuu	--uu uuuu
TMR		1111 1111	1111 1111	1111 1111
CPIO B		--11 1111	--11 1111	--11 1111

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status: bit 7	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	0	u	u
/MCLR reset during SLEEP	0	1	0
WDT reset (not during SLEEP)	0	0	1
WDT reset during SLEEP	0	0	0
Wake-up from SLEEP on pin change	1	1	0

9. Oscillator start up timer condition :

Oscillator Type	Power-on reset	Subsequest resets
INTRC	20ms	300us

10. Electrical Characteristics

*Note: Temperature=25°C

1.Operation Current :

(1) INRC 4MHz , WDT - enable

2.5V	300uA
3.0V	375uA
4.0V	500uA
5.0V	675uA
5.5V	750uA

These parameters are for reference only.

(2) INRC 4MHz , WDT - enable , PED - enable

2.5V	375uA
3.0V	450uA
4.0V	525uA
5.0V	750uA
5.5V	825uA

These parameters are for reference only.

(3) INRC 8MHz , WDT - enable

2.5V	450uA
3.0V	525uA
4.0V	750uA
5.0V	975uA
5.5V	1.1mA

These parameters are for reference only.

(4) INRC 8MHz , WDT - enable , PED - enable

2.5V	525uA
3.0V	600uA
4.0V	800uA
5.0V	1.1mA
5.5V	1.2mA

These parameters are for reference only.

2. Supply Voltage

	Min	Max
VDD	2.5V	5.0V

These parameters are for reference only.

3. Input Voltage (VDD = 5V)

	Port	Min	Max
Vil	TTL	VSS	1.0V
	Schmitt trigger	VSS	0.6V
Vih	TTL	3.0V	VDD
	Schmitt trigger	3.5V	VDD

These parameters are for reference only.

Input Voltage (VDD = 3V)

	Port	Min	Max
Vil	TTL	VSS	0.6V
	Schmitt trigger	VSS	0.3V
Vih	TTL	2.0V	VDD
	Schmitt trigger	2.2V	VDD

These parameters are for reference only.

4. Output Voltage (VDD = 5V)

	PB	Condition
Voh	3.6V	Ioh = -20mA
Vol	0.9V	Iol = 20mA
Voh	4.2V	Ioh = -5mA
Vol	0.7V	Iol = 5mA

These parameters are for reference only.

Output Voltage (VDD = 3V)

	PB	Condition
Voh	1.7V	Ioh = -10mA
Vol	0.9V	Iol = 10mA
Voh	2.1V	Ioh = -5mA
Vol	0.7V	Iol = 5mA

These parameters are for reference only.

5. PED Voltage

Low level	High level
1.8V +/- 20%	2.1V +/- 20%

These parameters are for reference only.

6. The basic WDT time-out cycle time

VDD	Time
2.5V	24ms
3.0V	21ms
4.0V	19ms
5.0V	18ms

These parameters are for reference only.

8. Pull high/low resistor

VDD	5V	3V
PB0/1/4/5	20K Ohm +/- 20%	40K Ohm +/- 20%
PB2	110K Ohm +/- 20%	220K Ohm +/- 20%
PB3	280K Ohm +/- 20%	630K Ohm +/- 20%
MCLRB	70K Ohm +/- 20%	85K Ohm +/- 20%

These parameters are for reference only.