MD1213

High-Speed Dual-MOSFET Driver

Features

- 6 ns Rise and Fall Time with 1000 pF Load
- 2A Peak Output Source and Sink Currents
- 1.8V to 5V Input CMOS Compatible
- 4.5V to 13V Total Supply Voltage
- Smart Logic Threshold
- Low-Jitter Design
- Two Matched Channels
- Outputs can Swing Below Ground
- Low-Inductance Package
- Thermally Enhanced Package

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-Destructive Testing
- PIN Diode Driver
- CCD Clock Driver/Buffer
- High-Speed Level Translator

General Description

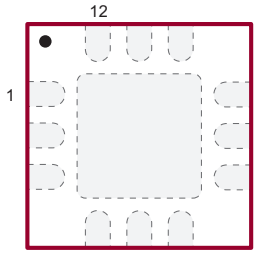
The MD1213 is a high-speed dual-MOSFET driver. It is designed to drive high-voltage P-channel and N-channel MOSFETs for medical ultrasound and other applications requiring a high-output current for a capacitive load. The high-speed input stage of the MD1213 can operate from 1.8V to 5V logic interface with an optimum operating input signal range of 1.8V to 3.3V. An adaptive threshold circuit is used to set the level translator switch threshold to the average of the input logic `0` and logic `1` levels. The input logic levels may be ground referenced even though the driver is putting out bipolar signals. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

The output stage of the MD1213 has separate power connections enabling the output signal L and H levels to be chosen independently from the supply voltages used for the majority of the circuit. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V to –5V, and the output L and H levels may be varied anywhere over the range of –5V to +5V. The output stage is capable of peak currents of up to ±2A, depending on the supply voltages used and load capacitance present.

The OE pin serves a dual purpose. First, its logic H level is used to compute the threshold voltage level for the channel input level translators. Second, when OE is low, the outputs are disabled with the A output high and the B output low. This assists in properly pre-charging the AC coupling capacitors that may be used in series in the gate drive circuit of an external PMOS and NMOS transistor pair.

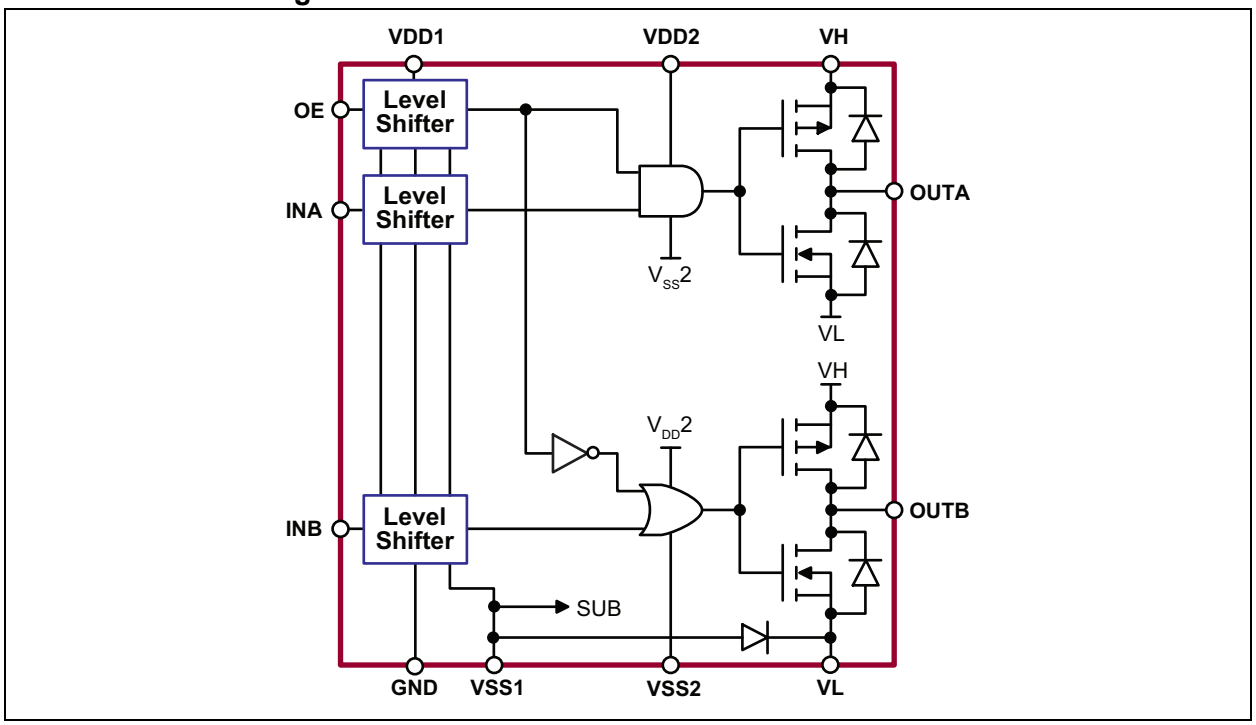
Package Type

12-lead QFN
(Top view)

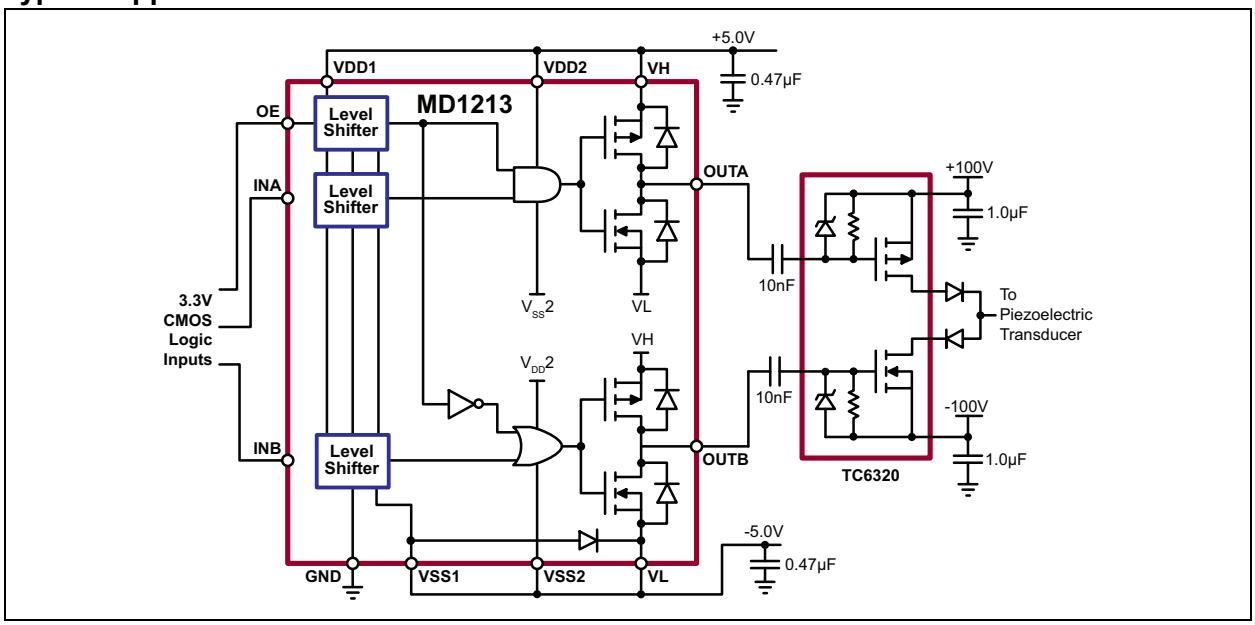


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Level Translator Supply Voltage, $V_{DD}–V_{SS}$ .....–0.5V to +13.5V
Output High Supply Voltage, V_H ..... V_L–0.5V to V_{DD} + 0.5V
Output Low Supply Voltage, V_L ..... V_{SS}–0.5V to V_H+ 0.5V
Low-Side Supply Voltage, V_{SS} ..... –7V to + 0.5V
Logic Input Pins ..... V_{SS}–0.5V to GND +7V
Maximum Junction Temperature, T_J ..... +125°C
Operating Ambient Temperature, T_A ..... –40°C to +85°C
Storage Temperature, T_S .....–65°C to +150°C
ESD Rating (**Note 1**) ..... ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Device is ESD sensitive. Handling precautions are recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified, $V_H = V_{DD}1 = V_{DD}2 = 12V$, $V_L = V_{SS}1 = V_{SS}2 = 0V$, $V_{OE} = 3.3V$, $T_A = 25°C$.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Level Translator Supply Voltage	$V_{DD}–V_{SS}$	4.5	—	13	V	$2.5V \le V_{DD} \le 13V$
Level Translator Negative Supply Voltage	V_{SS}	–5.5	—	0	V	
Output High Supply Voltage	V_H	V_{SS} +2	—	V_{DD}	V	
Output Low Supply Voltage	V_L	V_{SS}	—	V_{DD} –2	V	
$V_{DD}1$ Quiescent Current	I_{DD1Q}	—	0.55	—	mA	No input transitions
$V_{DD}2$ Quiescent Current	I_{DD2Q}	—	—	10	µA	
V_H Quiescent Current	I_{HQ}	—	—	10	µA	
$V_{DD}1$ Average Current	$I_{DD}1$	—	0.88	—	mA	One channel on at 5 MHz, no load
$V_{DD}2$ Average Current	$I_{DD}2$	—	6.6	—	mA	
V_H Average Current	I_H	—	23	—	mA	
Input Logic Voltage High	V_{IH}	V_{OE}–0.3	—	5	V	For logic inputs INA and INB
Input logic Voltage Low	V_{IL}	0	—	0.3	V	
Input Logic Current High	I_{IH}	—	—	1	µA	
Input Logic Current Low	I_{IL}	—	—	1	µA	
OE Input Logic Voltage High	V_{IH}	1.8	—	5	V	For logic input OE
OE Input Logic Voltage Low	V_{IL}	0	—	0.3	V	
OE Input Logic Impedance to GND	R_{IN}	12	20	30	KΩ	
Logic Input Capacitance	C_{IN}	—	5	10	pF	All inputs
Output Sink Resistance	R_{SINK}	—	—	12.5	Ω	I_{SINK} = 50 mA
Output Source Resistance	R_{SOURCE}	—	—	12.5	Ω	I_{SOURCE} = 50 mA
Peak Output Sink Current	I_{SINK}	—	2	—	A	
Peak Output Source Current	I_{SOURCE}	—	2	—	A	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD}1 = V_{DD}2 = 12V$, $V_L = V_{SS}1 = V_{SS}2 = 0V$, $V_{OE} = 3.3V$, $T_A = 25°C$.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Inputs or OE Rise and Fall Time	t_{irf}	—	—	10	ns	Logic input edge speed requirement
Propagation Delay when Output is from Low to High	t_{PLH}	—	7	—	ns	C_{LOAD} = 1000 pF, input signal rise/fall time of 2 ns (See **Timing Diagram** and Figure 3-1.)
Propagation Delay when Output is from High to Low	t_{PHL}	—	7	—	ns	
Propagation Delay OE to Outputs	t_{POE}	—	9	—	ns	C_{LOAD} = 1000 pF, input signal rise/fall time of 2 ns (See **Timing Diagram**.)
Output Rise Time	t_r	—	6	—	ns	
Output Fall Time	t_f	—	6	—	ns	
Rise and Fall Time Matching	$\lvert t_r - t_f \rvert$	—	1	—	ns	For each channel
Propagation Low to High and High-to-low Matching	$\lvert t_{PLH} - t_{PHL} \rvert$	—	1	—	ns	
Propagation Delay Match	Δt_{dm}	—	±2	—	ns	Device-to-device delay match

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	—	—	+125	°C	
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
12-lead QFN	θ_{JA}	—	47	—	°C/W	Note 1
Thermal Resistance to Case	θ_{JC}	—	7	—	°C/W	

Note 1: On an 1 oz. 4-layer 3” x 4” PCB with thermal pad and thermal via array

Timing Diagram

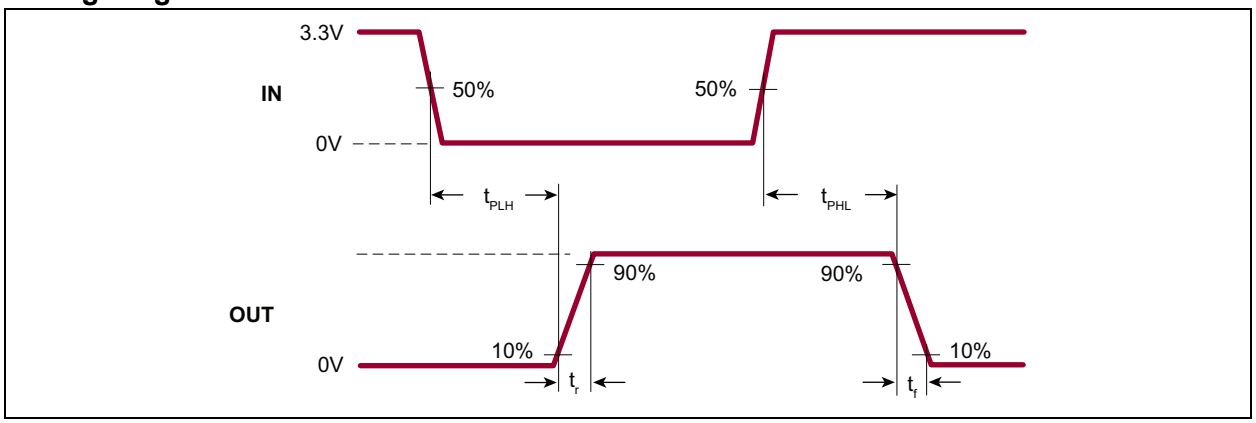


TABLE 1-1: TRUTH FUNCTION TABLE

Logic Input			Output	
OE	**INA**	**INB**	**OUTA**	**OUTB**
H	L	L	V_H	V_H
H	L	H	V_H	V_L
H	H	L	V_L	V_H
H	H	H	V_L	V_L
L	X	X	V_H	V_L

2.0 PIN DESCRIPTION

The details on the pins of MD1213 are listed on Table 2-1. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	INA	Logic input. Controls OUTA when OE is high. Input logic high will cause the output to swing to VL. Input logic low will cause the output to swing to VH. (See Figure 3-2.)
2	VL	Supply voltage for N-channel output stage
3	INB	Logic input. Controls OUTB when OE is high. Input logic high will cause the output to swing to VL. Input logic low will cause the output to swing to VH. (See Figure 3-2.)
4	GND	Logic input ground reference
5	VSS1	Low-side analog circuit and level translator supply voltage. VSS1 must be at the lowest potential of the chip. Thermal Pad and Pin 5 must be connected externally.
6	VSS2	Low-side gate drive supply voltage. VSS2 should be at the same potential as VSS1.
7	OUTB	Output driver. Swings from VH to VL. Intended to drive the gate of an external N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTB will swing to VL, turning off the external N-channel MOSFET.
8	VH	Supply voltage for P-channel output stage
9	OUTA	Output driver. Swings from VH to VL. Intended to drive the gate of an external P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTA will swing to VH, turning off the external P-channel MOSFET.
10	VDD2	High-side gate drive supply voltage
11	VDD1	High-side analog circuit and level shifter supply voltage. Should be at the same potential as VDD2.
12	OE	Output-enable logic input. When OE is high, $(V_{OE} + V_{GND})/2$ sets the threshold transition between logic level high and low for INA and INB. When OE is low, OUTA is at VH and OUTB is at VL regardless of INA and INB.
Thermal Pad		Index Pad and Thermal Pad are connected internally.

3.0 APPLICATION INFORMATION

For proper operation of the MD1213, low-inductance bypass capacitors should be used on the various supply pins. The GND input pin should be connected to the digital ground. The INA, INB and OE pins should be connected to their logic source with a swing of GND to logic level 1.8V to 5V. Good PCB layout trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1213 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effect of the load capacitance. Because of this speed and the high transient currents due to the capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the $V_{SS}1$, $V_{SS}2$, and V_L pins should have low-inductance feed-through connections to a ground plane. The power connections $V_{DD}1$ and $V_{DD}2$ should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads. A common capacitor and voltage source may be used for these two pins, which should always have the same applied DC voltage. For applications sensitive to jitter and noise, separate decoupling networks may be used for $V_{DD}1$ and $V_{DD}2$.

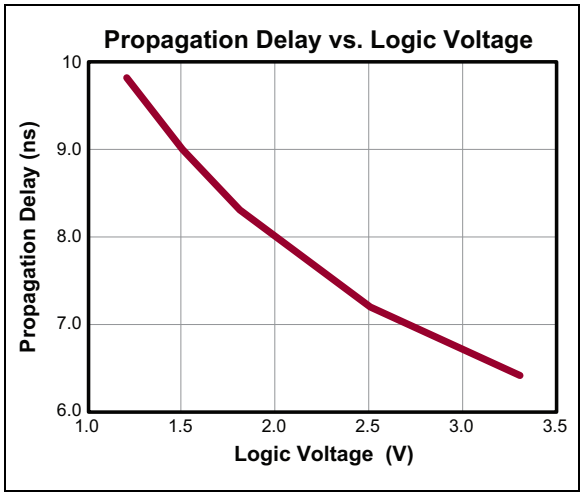


FIGURE 3-1: *Propagation Delay.*

The supplied voltages of V_H and V_L determine the output logic levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with a suitable bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1 µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead going to the capacitor.

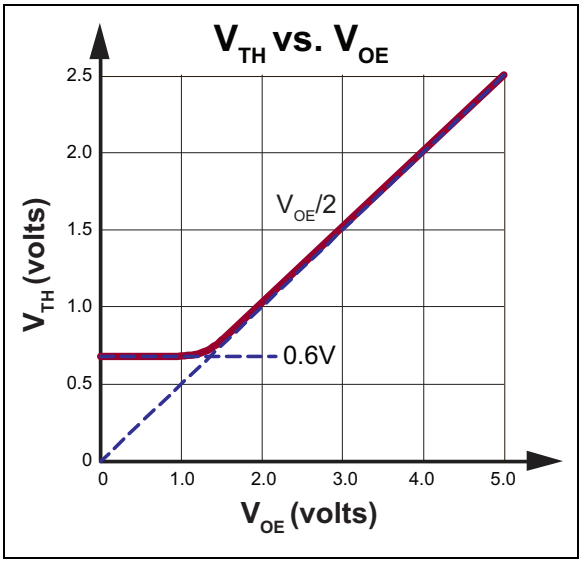


FIGURE 3-2: *Logic Input Threshold.*

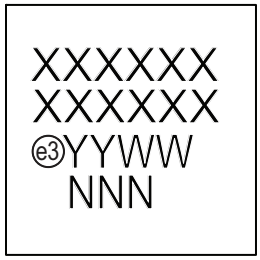
Pay particular attention to minimizing trace lengths and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases, it may be desirable to add a small series resistor in series with the output signal to obtain better waveform integrity at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

Focus on parasitic coupling from the driver output to the input signal terminals. This feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Make sure that the circulating ground return current from a capacitive load will not react with common inductance and cause noise voltages in the input logic circuitry.

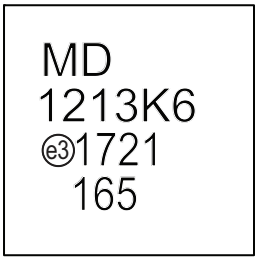
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

12-lead QFN



Example

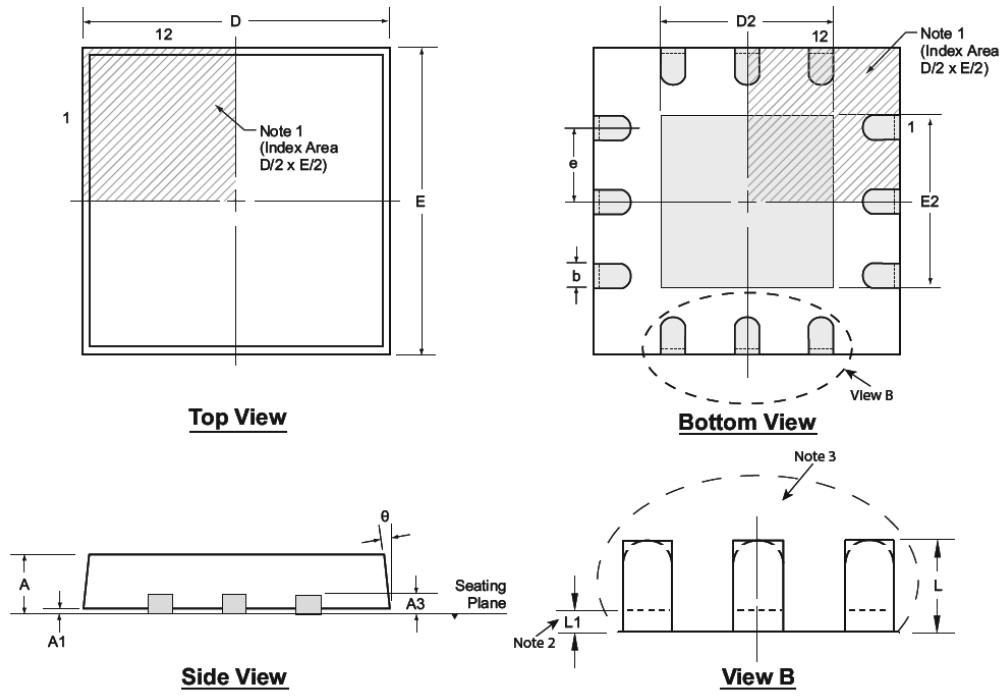


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

12-Lead QFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.80mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	0.75	3.85*	0.75	0.80 BSC	0.35	0.00	0°
	NOM	0.90	0.02		0.30	4.00	1.70	4.00	1.70		0.55	-	-
	MAX	1.00	0.05		0.35	4.15*	2.25	4.15*	2.25		0.75	0.15	14°

JEDEC Registration MO-220, Variation VGGB, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision B (June 2017)

The following is the list of modifications:

- Updated the operating ambient temperature in Absolute Maximum Ratings† and in the Temperature Specifications table.
- Made minor text changes throughout the document.

Revision A (April 2017)

- Converted Supertex Doc# DSFP-MD1213 to Microchip DS20005713B
- Updated the package marking format
- Changed the quantity of the 12-lead QFN K6 package from 3000/Reel to 5000/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	MD1213	=	High-Speed Dual-MOSFET Driver
Package:	K6	=	12-lead QFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	5000/Reel for a K6 Package

Example:

a) MD1213K6-G: High-Speed Dual-MOSFET Driver 12-lead (4x4) QFN, 5000/Reel

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