PN26G01AWSIUG
3.3V 1G-BIT SPI NAND FLASH MEMORY

A1.7

2017-5-4

Future routine revisions will occur when appropriate, without notice. Contact PARAGON TECHNOLOGY LIMITED, sales office to obtain the latest specifications and before placing your product order. Please also pay attention to information published by XTX TECHNOLOGY LIMITED by various means, including X T X TECHNOLOGY LIMITED. Home page (http://www.xtxtech.com)

1. Overview

The PN26G01A is a 1G-bit (128M-byte) SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The PN26G01A supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O option.

2. Features

- **1Gbit of NAND Flash memory**
  - Single-level cell (SLC) technology
  - Page size : 2176 bytes(2048 + 128 bytes)
  - Block size : 64 pages(128K + 8K bytes)
  - Device size: 1Gb(1024 blocks)

- **Serial Interface**
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3

- **High Performance**
  - 108MHz for fast read
  - Quad I/O data transfer up to 432Mbits/s
  - 2176/2048/64/16 wrap read option
  - 2K-Byte cache for fast random read
  - Cache read and cache program

- **Advanced Security Features**
  - Write protect all/portion of memory via software
  - Individual Block array protection
  - Lockable 16K-Byte OTP region
  - 64-Bit Unique ID for each device

- **Program/Erase/Read Speed**
  - Page Program time : 300us typical (without ECC)
  - BLOCK ERASE time : 3ms typical
  - PAGE READ time : 120us maximum (without ECC)

- **Single Supply Voltage : 2.7V~3.6V**

- **Advanced Security Features**
  - Internal ECC option, per 512 bytes
  - Internal data move by page with ECC
  - Promised golden block0

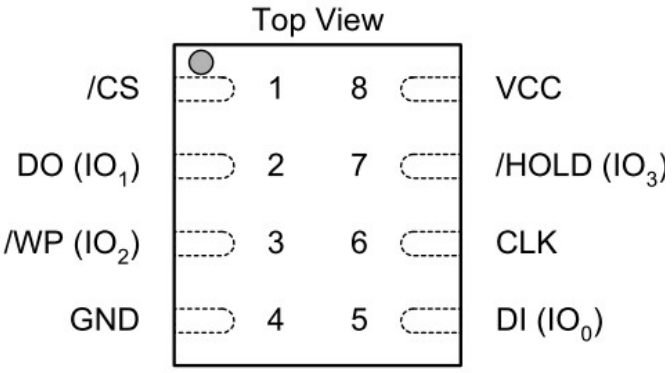
- **Package**
  - 8-pin WSON (8*6mm)
  - 24-pin TFBGA (8*6mm)
  - All Packages are RoHS Compliant and Halogen-free

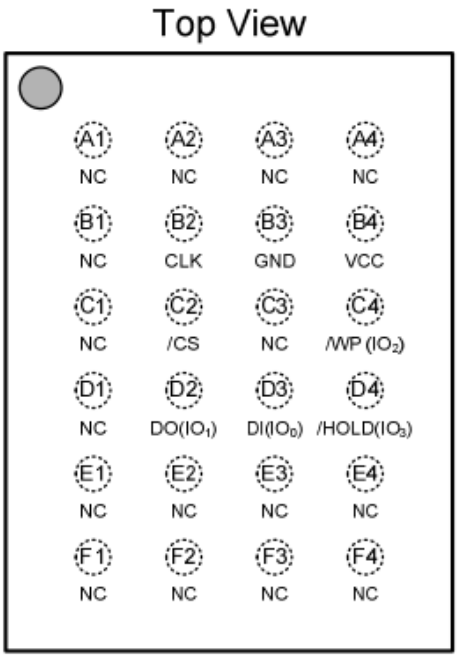
- **Minimum 100,000 Program/Erase Cycles**

- **Data retention: 10 years**

3. Packaging Type and Pin Configurations

PN26G01A is offered in an 8-pin WSON 8x6-mm as shown in Figure 1. Package diagram and dimension are illustrated at the end of this datasheet.



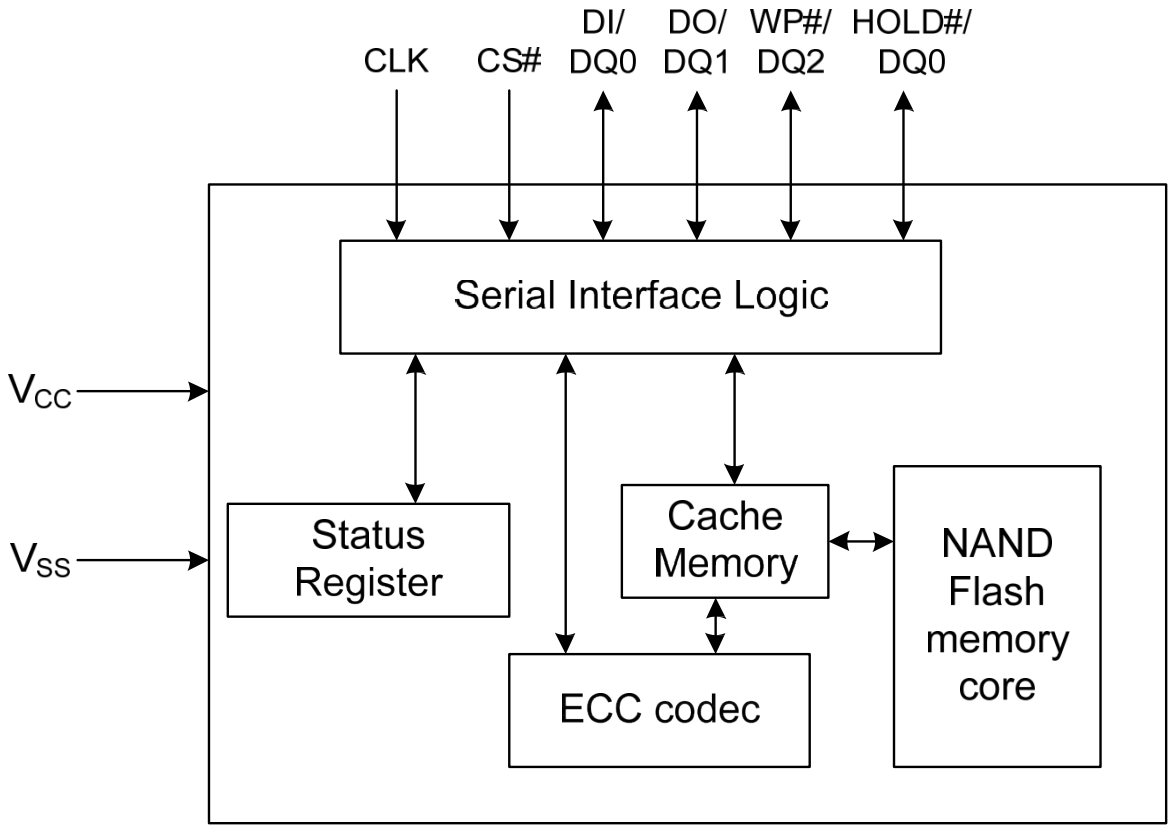


3.1 Pin Description

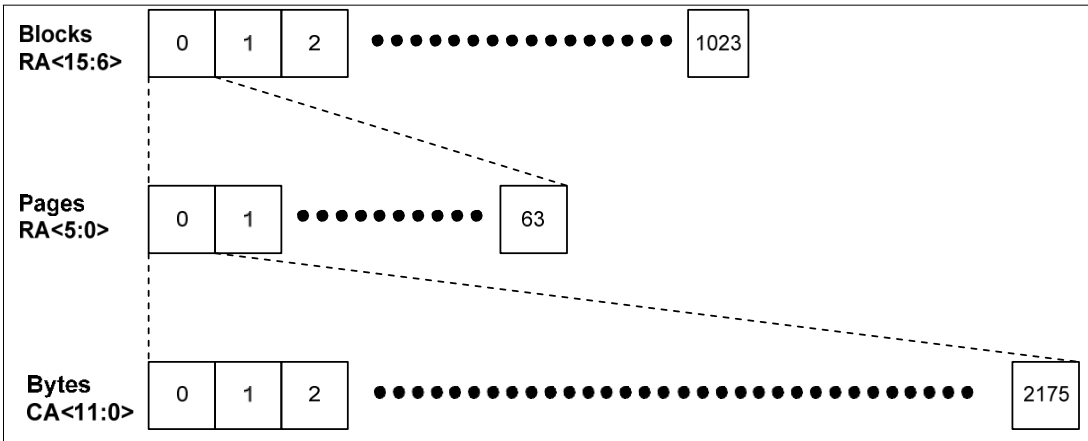
PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ_1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (DQ_0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD# (DQ_3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Note:
1 DQ_0 and DQ_1 are used for Dual SPI instructions.
2 DQ_0 – DQ_3 are used for Quad SPI/DDR instructions

4. Block Diagram



5. Memory Mapping



Note:

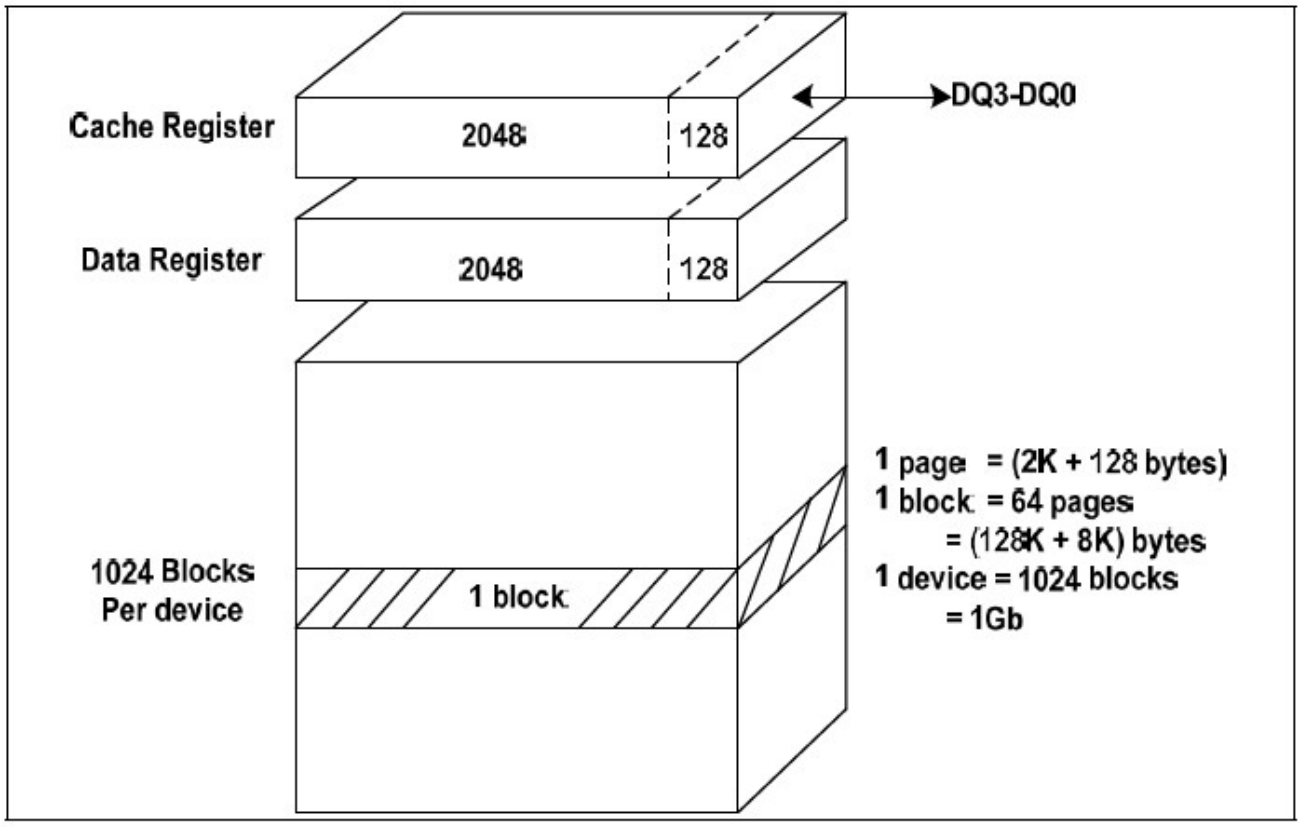
1. **CA**: Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however,only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are "out of bounds, " do not exists in the device, and cannot be addressed.
2. **RA**: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

6. Array Organization

Table 2 Array Organization

Each device has	Each block has	Each page has	Unit
128M + 8M	128K + 8K	2K + 128	bytes
1024 x 64	64	-	Pages
1024	-	-	Blocks

Figure 4 Array Organization



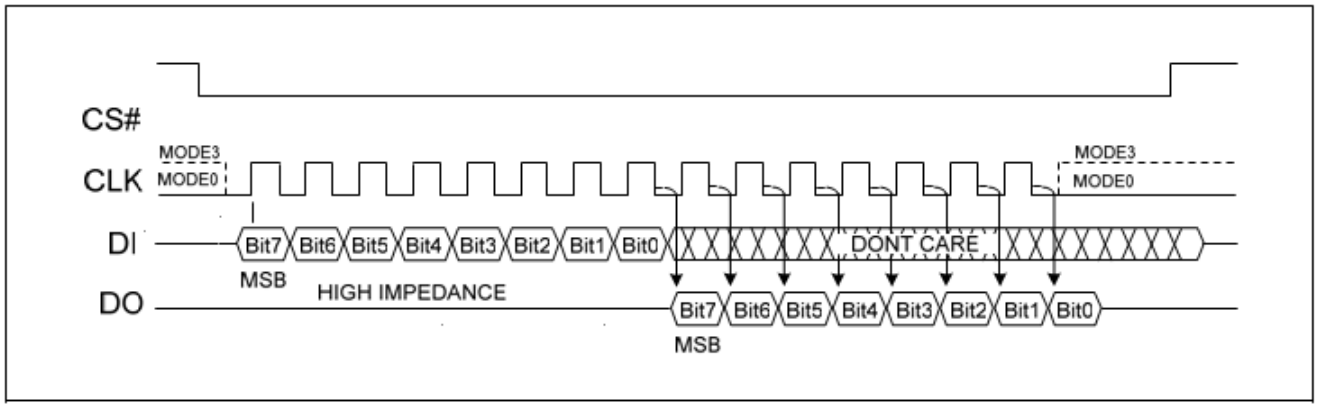
7. DEVICE OPERATION

7.1 SPI Modes

.Standard SPI

The PN26G01A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.



SPI SDR Modes Supported

.Dual SPI

The PN26G01A supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ0 and DQ1.

.Quad SPI

The PN26G01A supports Quad SPI operation when using the x4 and Quad IO instructions. These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. T When using Quad SPI instructions the DI and DO pins become bidirectional DQ0 and DQ1 and the WP # and HOLD# pins become DQ2 and DQ3 respectively. Quad SPI instructions require the Quad Enable bit (QE) to be set.

7.2 Pin Description

CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ0, DQ1, DQ2, DQ3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

Serial Input (DI) / DQ0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal.

DI becomes DQ0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

Serial Output (DO) / DQ1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal.

DO becomes DQ1 -an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

Write Protect (WP#) / DQ2

When WP# is driven Low (VIL), during a SET FEATURES command and while the BRWD bit of the Status Register is set to a 1, it is not possible to write to the Status Registers. This prevents any alteration of the Block Protect (BP2, BP1,BP0), INV and CMP bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect(BP2, BP1,BP0), INV and CMP bits, are also hardware protected against data modification if WP# is Low during a SET FEATURES command. The WP# function is not available when the Quad mode is enabled (QE=1).

The WP# function is replaced by DQ2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

Hold (HOLD#) / DQ3

For Standard SPI and Dual SPI operations, the HOLD# signal allows the PN26G01A operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Output (DO) is high impedance, and Serial Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

The HOLD# function is not available when the Quad mode is enabled (QE =1). The Hold function is replaced by DQ3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

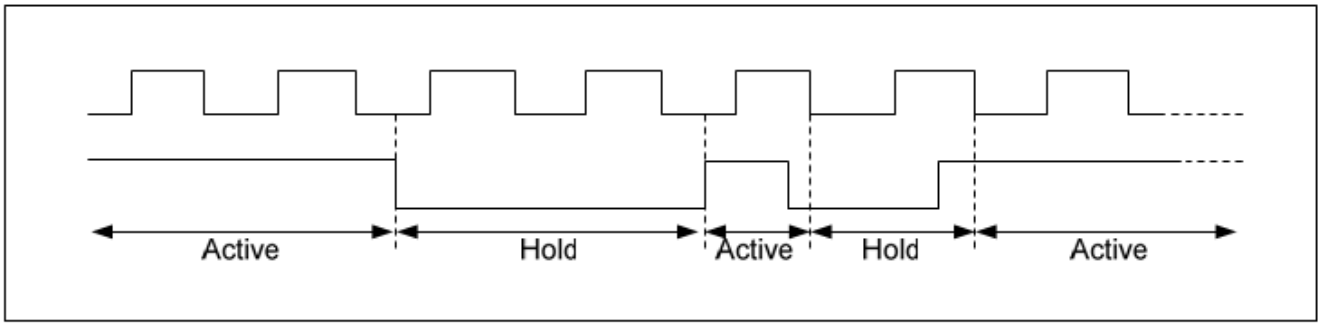


Figure 6 Hold Condition Waveform

7.3 Command Set Tables

Table 1 Standard SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
WRITE ENABLE WRITE DISABLE	**06h** **04h**					
GET FEATURES	**0Fh**	A7-A0	(D7-D0)			
SET FEATURES	**1Fh**	A7-A0	D7-D0			
PAGE READ READ FROM CACHE	**13h** **03h/0Bh**	A23-A16 A15-A8(2)	A15-A7 A7-A0	A7-A0 dummy	 (D7-D0)	 wrap
Cache Read Read ID	**31h** **9Fh**	 A7-A0	 (MID) (8)	 (DID) (8)	 	 wrap
READ UID PROGRAM LOAD	**4Bh** **02h**	dummy A15-A8(6)	dummy A7-A0	dummy D7-D0	dummy Next byte	(D7-D0) Byte N
PROGRAM LOAD RANDOM DATA(9)	**84h**	A15-A8(6)	A7-A0	D7-D0	Next byte	Byte N
Cache Program	**15h**					
BLOCK ERASE	**D8h**	A23-A16	A15-A7	A7-A0		
Reset	**FFh**					
INDIVIDUAL BLOCK LOCK	**36h**	A23-A16	A15-A8	A7-A0		
INDIVIDUAL BLOCK UNLOCK	**39h**	A23-A16	A15-A8	A7-A0		
Read Block Lock	**3Dh**	A23-A16	A15-A8	A7-A0	(D7-D0)	
GLOBAL BLOCK LOCK	**7Eh**					
GLOBAL BLOCK UNLOCK	**98h**					

Table 2 Dual SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x 2	**3Bh**	A15-A8(2)	A7-A0	dummy	(D7-D0)x2	wrap
READ FROM CACHE DUAL IO	**BBh**	A15-A0(3)	dummy(4)	(D7-D0)x2		wrap

Table 3 Quad SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x4 READ FROM CACHE QUAD IO	**6Bh** **EBh**	A15-A8(2) A15-A0(5)	A7-A0 (D7-D0)x4	dummy	(D7-D0)x4	wrap wrap
PROGRAM LOAD x4	**32h**	A15-A8(6)	A7-A0	D7-D0 x4	Next byte	Byte N
PROGRAM LOAD RANDOM DATA x4(9)	**C4h/34h**	A15-A8(6)	A7-A0	D7-D0 x4	Next byte	Byte N
PROGRAM LOAD RANDOM DATA Quad IO(9)	**72h**	A15-A0(7)	D7-D0 x4	Next byte		Byte N

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The x8 clock = wrap<3:0>, A11-A8
3. The x8 clock = wrap<3:0>, A11-A0

4. The x8 clock = dummy<7:0>,D7-D0
5. The x8 clock = wrap<3:0>,A11-A0,dummy<7:0>,D7-D0
6. The x8 clock = dummy<3:0>,A11-A8
7. The x8 clock = dummy<3:0>,A11-A0,D7-D0,D7-D0
8. MID is Manufacture ID(A1h for XTX), DID is Device ID(E1h for current device)
9. Only available in Internal Data Move operation
10. 10. A<23:22>=00, A<21:12> is RA<15:6>, A<11:0> is dummy bits

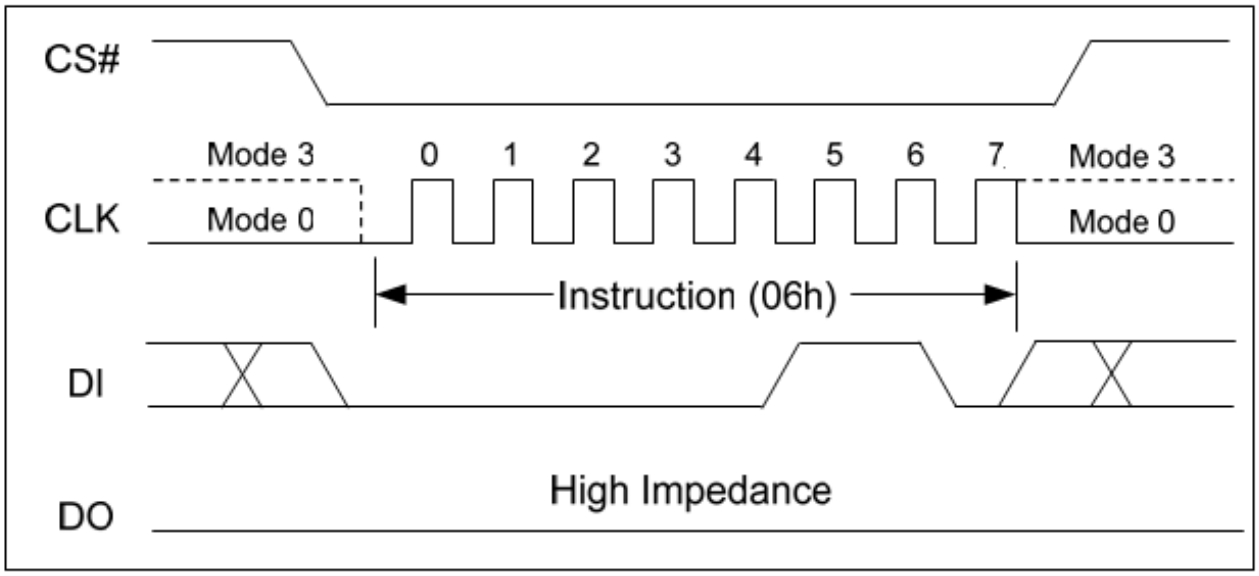
7.4 WRITE OPERATIONS

7.4.1 Write Enable (WREN) (06H)

The WRITE ENABLE (WREN) command sets the WEL bit in the status register to 1. The WEL bit must be set prior to following operations that changes the contents of the memory array:

- Page Program
- OTP Program
- OTP Lock
- BLOCK ERASE

Figure4. Write Enable Sequence Diagram

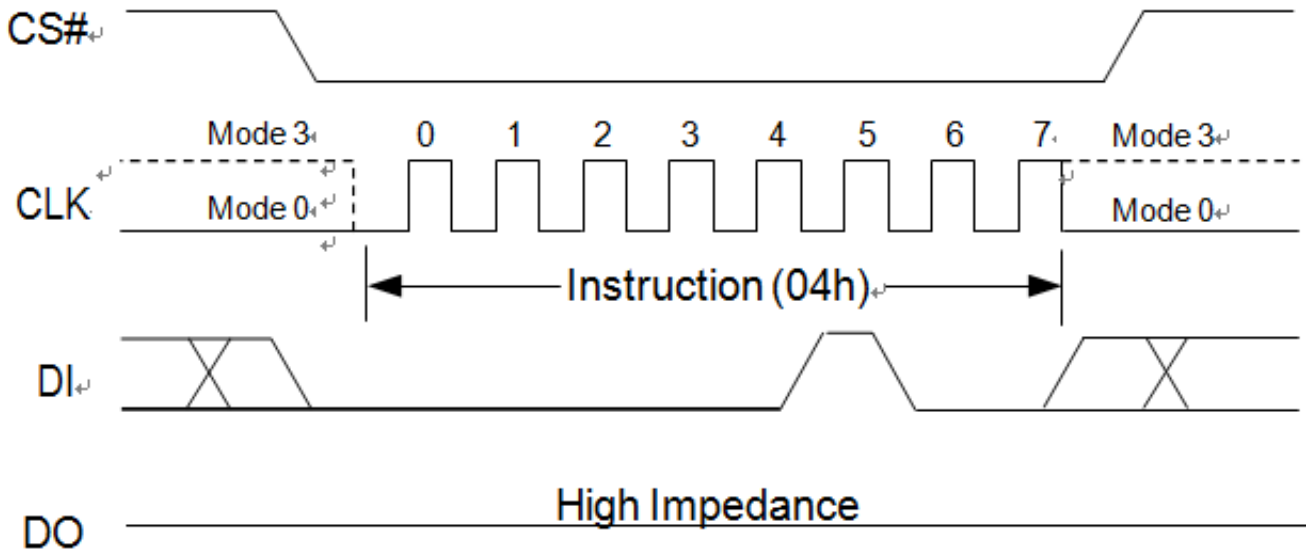


7.4.2 WRITE DISABLE (WRDI) (04h)

The WRITE DISABLE (WRDI) command resets the WEL bit in the status register to 0. The WEL bit is automatically reset after Power-up and upon completion of the following operations:

- Page Program
- OTP Program
- OTP Lock
- BLOCK ERASE

Figure5. Write Disable Sequence Diagram



7.5 FEATURE OPERATIONS

7.5.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown the following table). The status register is mostly read, except WEL, which is writable bit with the WREN (06h) command.

When a feature is set, it remains active until he deice is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table2. Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Feature	90h	Reserved	Reserved	Reserved	ECC_EN	Reserved	Reserved	Reserved	Reserved
Block Lock	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	WPS	Reserved	Reserved	Reserved	Reserved	QE
Status	C0h	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Note:

1. If BRWD is enabled and WP# is low, then the block lock register (BP2-BP0, INV and CMP) cannot be changed.
2. If QE is enabled, the quad IO operations can be executed.
3. All the reserved bits must be held low when the feature is set.
4. The features in the feature byte B0H are all volatile except OTP_PRT bit.

Figure9. Get Features Sequence Diagram

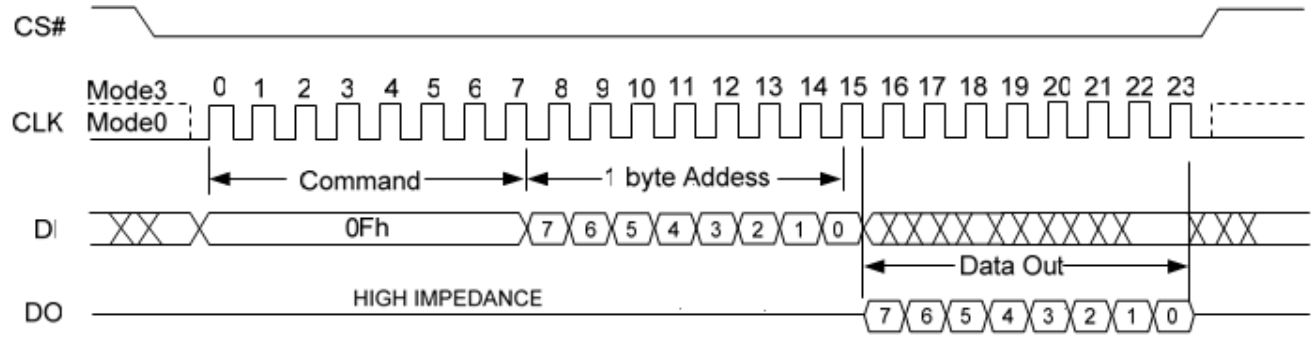
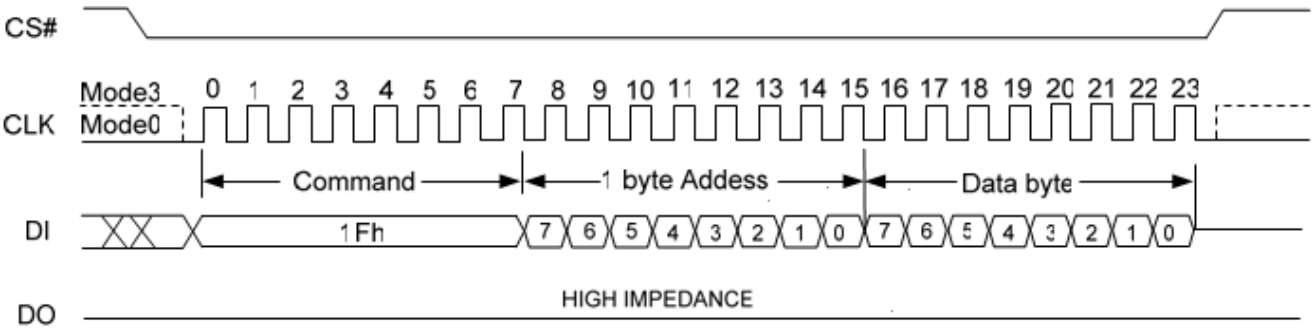


Figure10. Set Features Sequence Diagram



7.6 READ OPERATIONS

7.6.1 Page Read

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

1. 13h (PAGE READ TO CACHE)
2. 0Fh (GET FEATURES command to read the status)
3. 0Bh or 03h (READ FROM CACHE)
4. READ FROM CACHE Operation
   a) 3Bh (READ FROM CACHE x2)
   b) 6Bh (READ FROM CACHE x4)
   c) BBh (READ FROM CACHE DUAL IO)
   d) EBh (READ FROM CACHE QUAD IO)

The PAGE READ command requires a 24-bit address consisting of 8 dummy bits followed by an 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation (refer to the Status Register section). Following a status of successful completion, the READ FROM CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh) command must be issued in order to read the data out of the cache.

The READ FROM CACHE command requires 4 wrap mode configure bits, followed by 12-bit column address for the starting byte address. The starting byte address must be in 0 to 2175. After the end of the cache register is reached, the data wraps around the beginning boundary automatically until CS# is pulled high to terminate this operation..

Table3. Wrap configure bit table

	Wrap Length (byte)
00xx	2176
01xx	2048
10xx	64
11xx	16

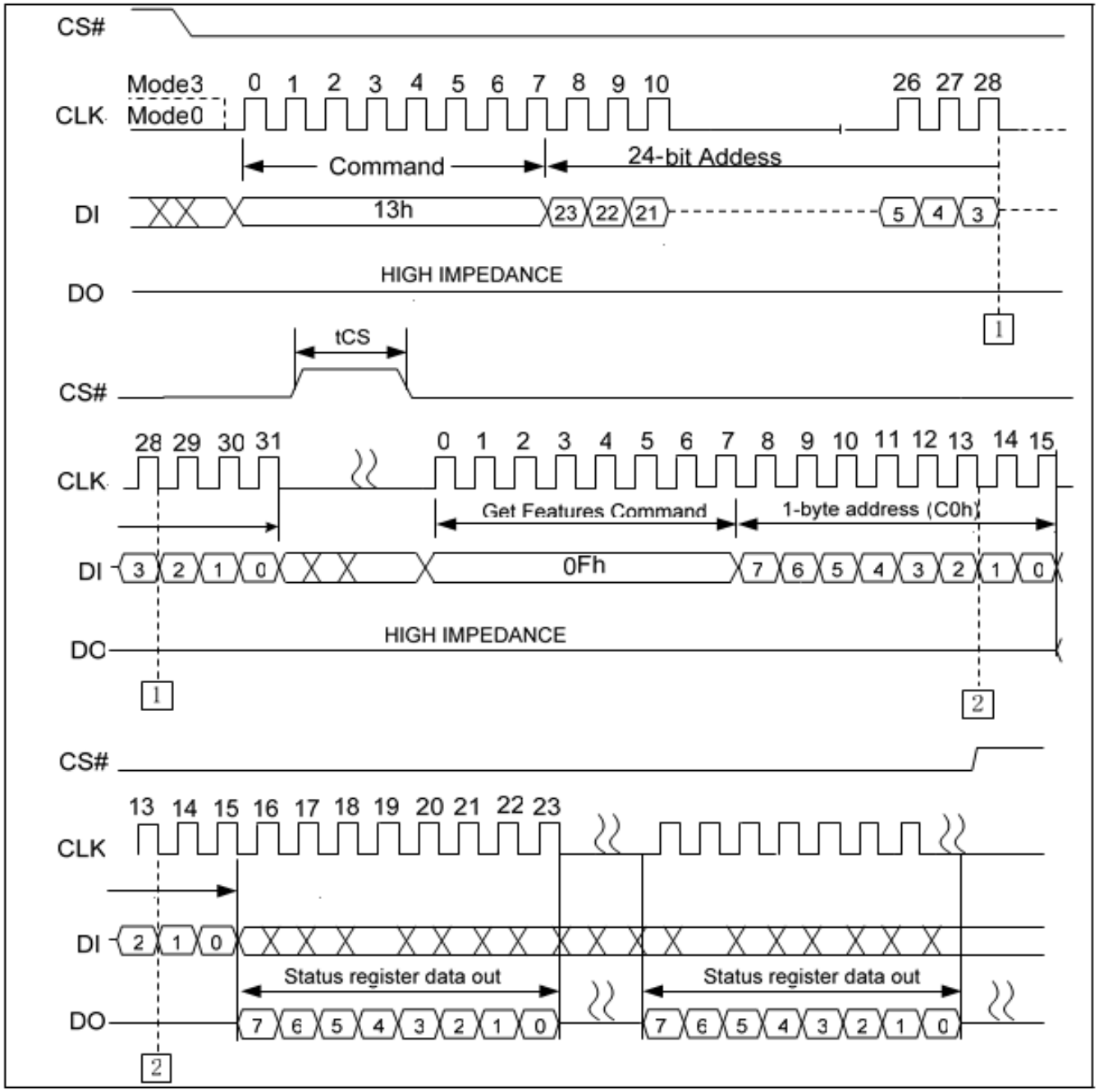
7.6.2 Page Read to Cache (13H)

The Page Read (to buffer) and Next Page Read and Last Page Read command can be used to increase READ operation speed when accessing sequential pages.

A normal PAGE READ (13H+24-bit address) command sequence is issued (see Figure 8 for details). The device is busy for tRD time during the time it takes to transfer the first page of data from the memory to the data register. Following a status of successful completion, the Page Read (to buffer) or Next Page Read (31H) command is latched into the command register. The device is busy for tDCBSYR1 while data is being transferred from the data register to the cache register. When the data register contents are transferred to the cache register, another Page Read is automatically started as part of the Page Read (to buffer) or Next Page Read (31H) command. Data is transferred from the memory array to the data register at the same time data is being output (RANDOM DATA READ 03H/0BH/3BH/6BH/BBH/EBH) from the cache register. If the total time to output data exceeds tRD, then the PAGE READ is hidden. The second and subsequent pages of data are transferred to the cache register by issuing additional Page Read (to buffer) or Next Page Read(31H) command. The device is busy for tDCBSYR1. This time can vary, depending on whether the previous memory-to-data-register transfer was completed before issuing the next Page Read (to buffer) or Next Page Read (31H) command. If the data transfer from memory to the data register is not completed before the Page Read (to buffer) or Next Page Read (31H) command is issued, the device is busy until the transfer is complete. It is not necessary to output a whole page of data before issuing another Page Read (to buffer) or Next Page Read (31H) command. The device is busy until the previous PAGE READ is complete and the data has been transferred to the cache register.

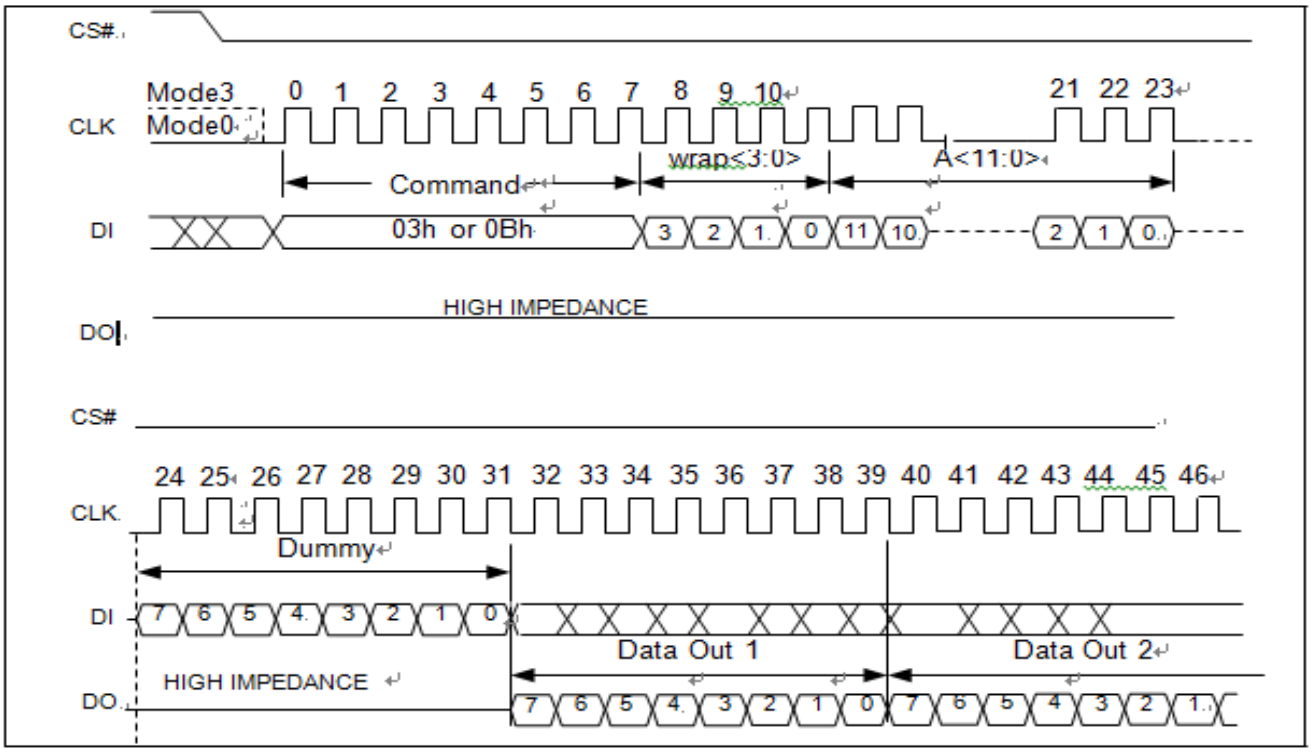
To read out the last page of data, the Last Page Read (3FH) command is issued. This command transfers data from the data register to the cache register without another PAGE READ (see Figure 9 for details). The ECC Enable bit (ECC_EN) of feature (90 [4]) must be set to enable for the page read to buffer command.

Figure11. Page Read to cache Sequence Diagram



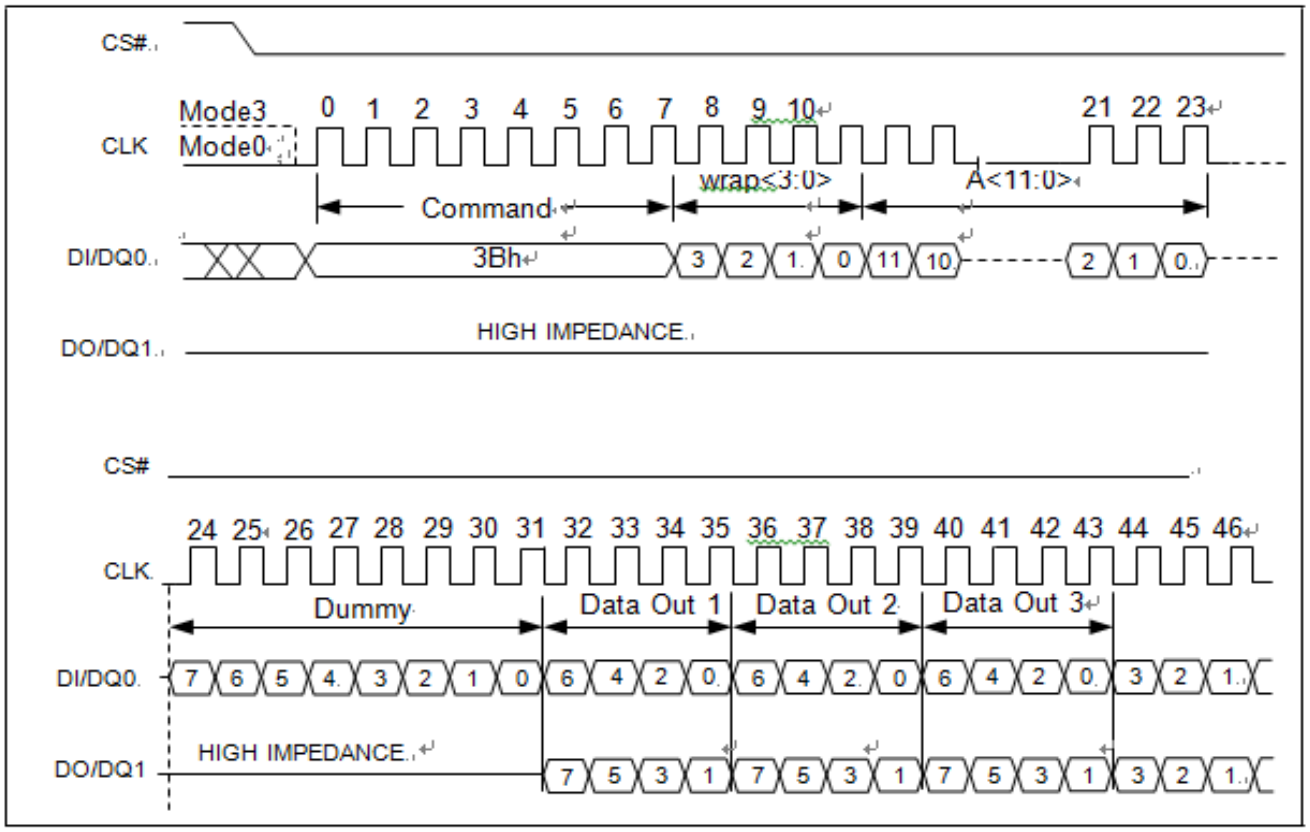
7.6.3 Read From Cache (03H or 0BH)

Figure12. Read From Cache Sequence Diagram



7.6.4 Read From Cache x2 (3BH)

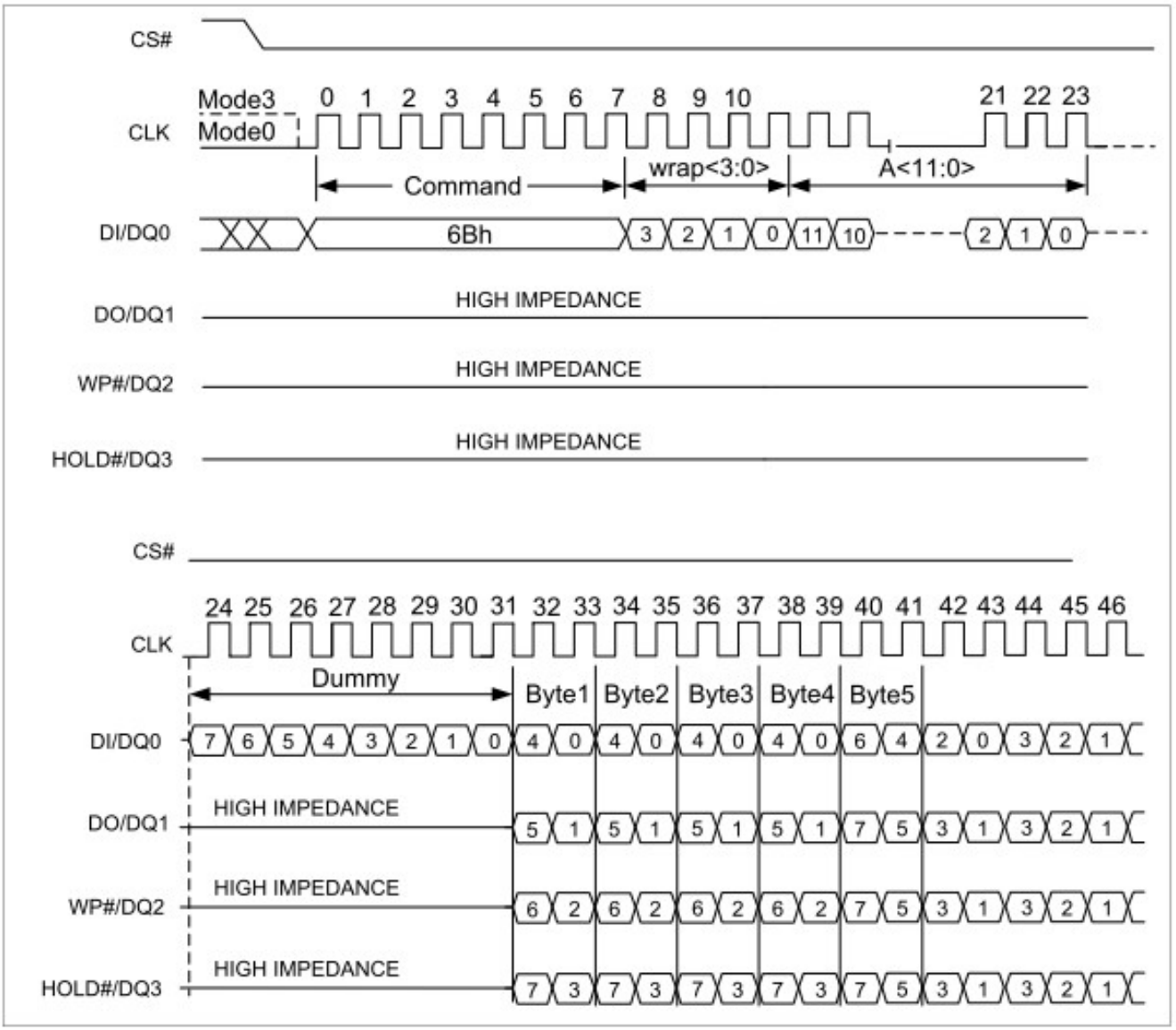
Figure13. Read From Cache x2 Sequence Diagram



7.6.5 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the read from cache x4 command. The ECC Enable bit (ECC_EN) of feature (90 [4]) must be set to enable for the page read to buffer command

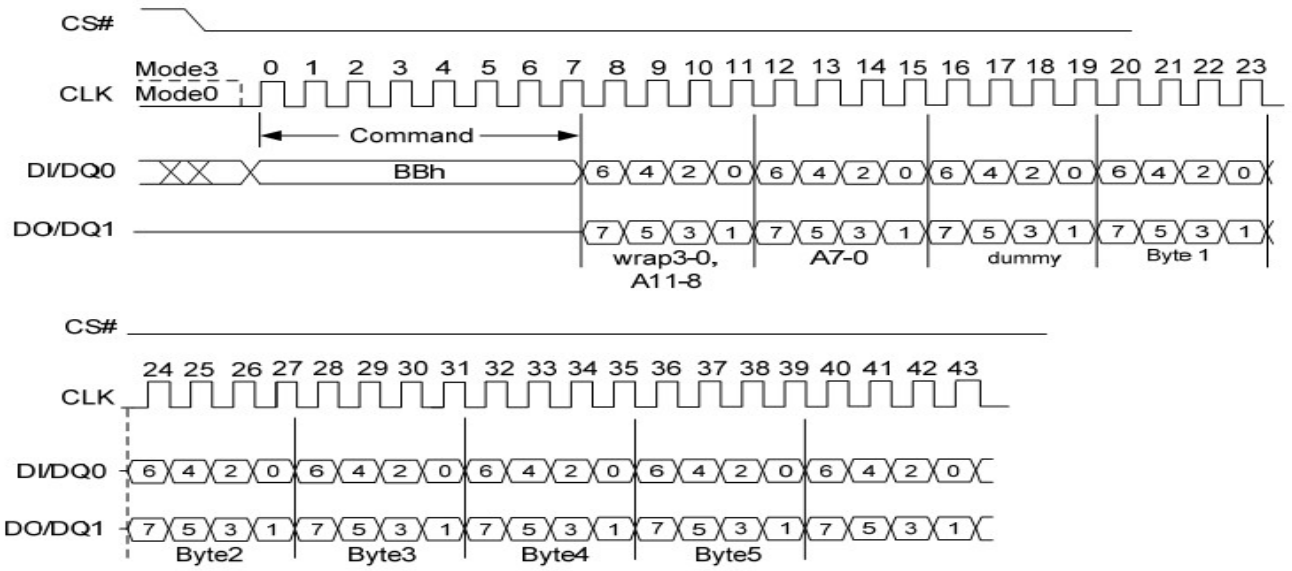
Figure12. Read From Cache x4 Sequence Diagram



7.6.6 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH) but with the capability to input the 4 Wrap bits, followed by a 12-bit column address for the starting byte address and a dummy byte by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary by the Wrap<3:0>.

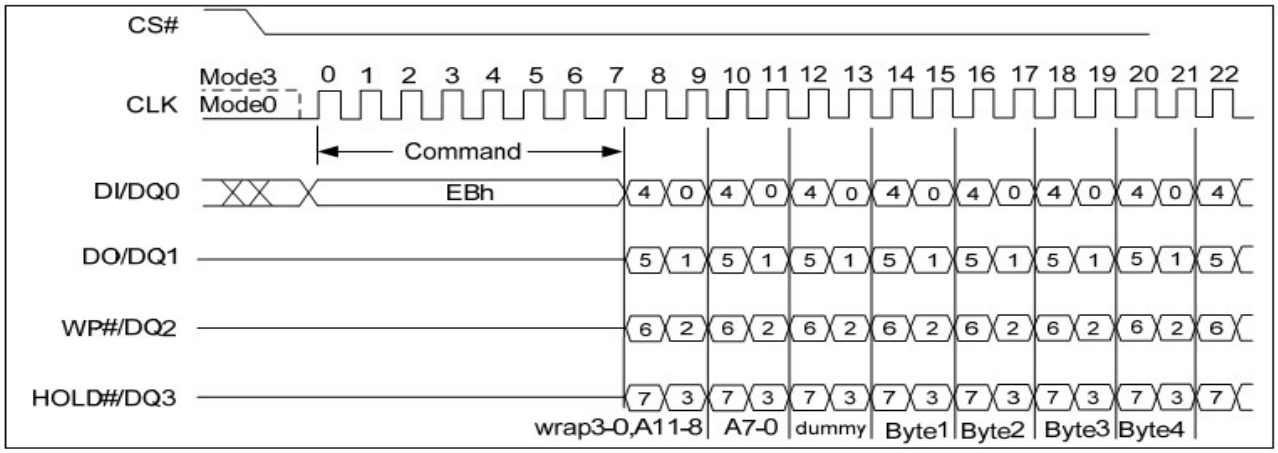
Figure13. Read From Cache Dual IO Sequence Diagram



7.6.7 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command but with the capability to input the 4 wrap bits, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the boundary by the Wrap<3:0>. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the read from cache quad IO command. The ECC Enable bit (ECC_EN) of feature (90 [4]) must be set to enable for the page read to buffer command.

Figure14. Read From Cache Quad IO Sequence Diagram



7.6.8 Read ID (9FH)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the device configuration.

Figure15. Read ID Sequence Diagram

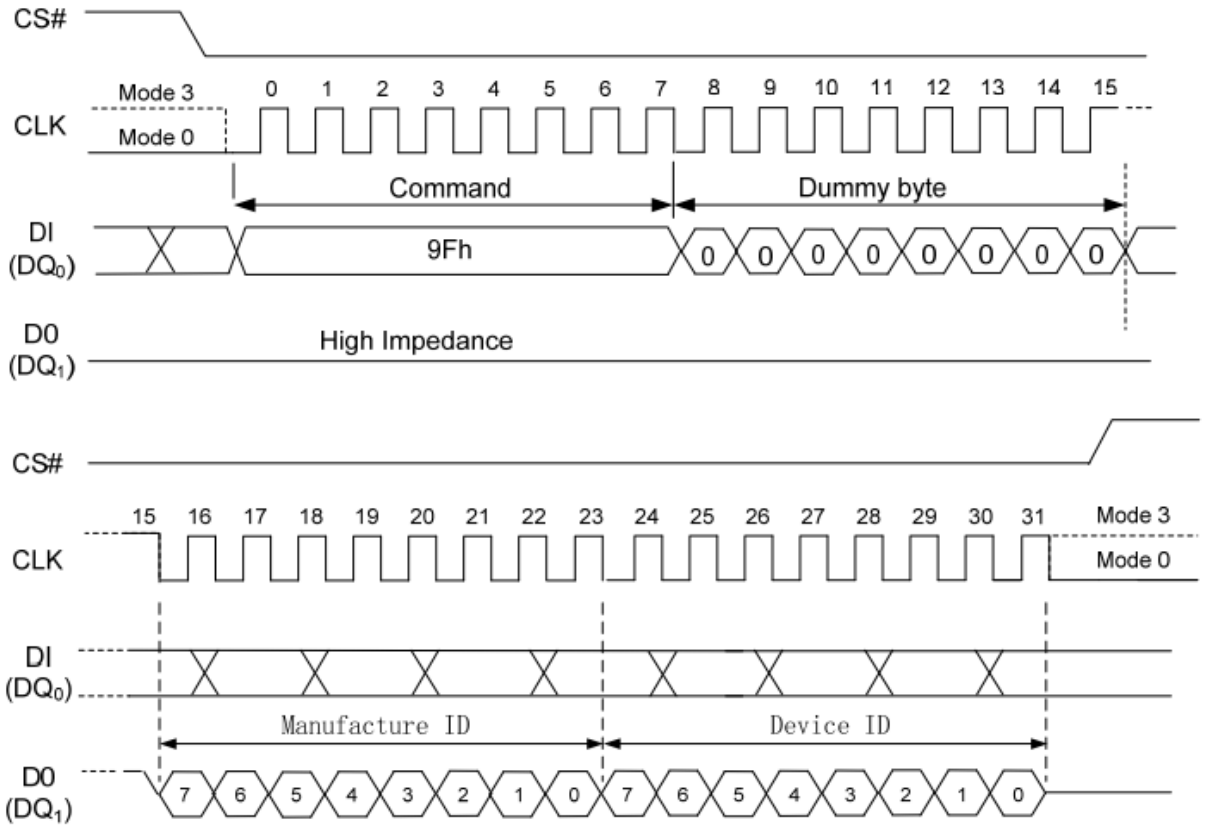


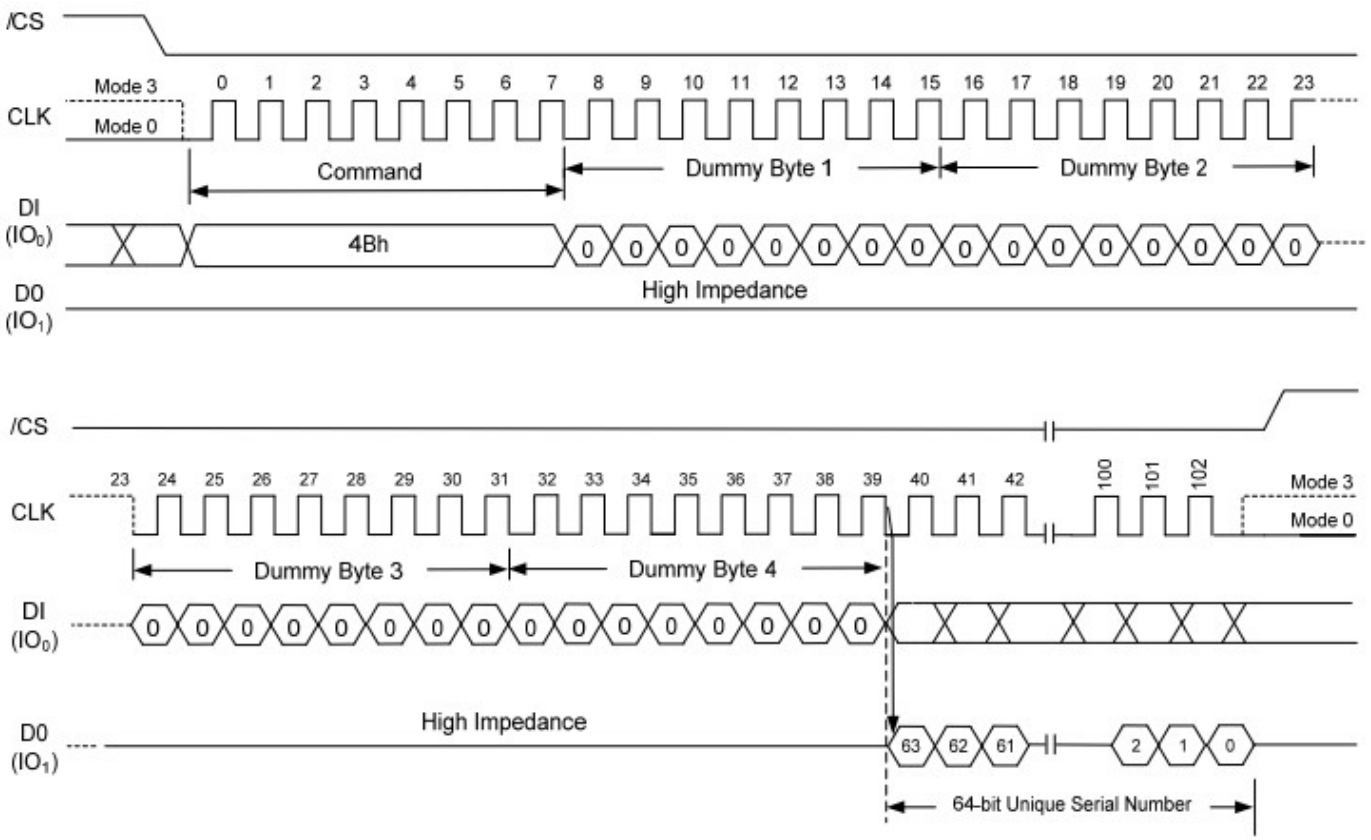
Table4. READ ID Table

Address	Value	Description
Byte 0	A1H	Manufacture ID (Paragon)
Byte 1	E1H	Device ID (SPI NAND 1Gbit)

7.6.9 READ UID (4Bh)

The READ UID instruction accesses a factory-set read-only 64-bit number that is unique to each PN26G01A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

Figure 16 READ UID (4Bh) Timing



7.7 PROGRAM OPERATIONS

7.7.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

The 1st step is to issue a PROGRAM LOAD (02H/32H) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register which is 2176 bytes long. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 19 shows the PROGRAM LOAD operation.

The 2nd step, prior to performing the PROGRAM EXECUTE operation, is to issue a WRITE ENABLE (06H) command. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

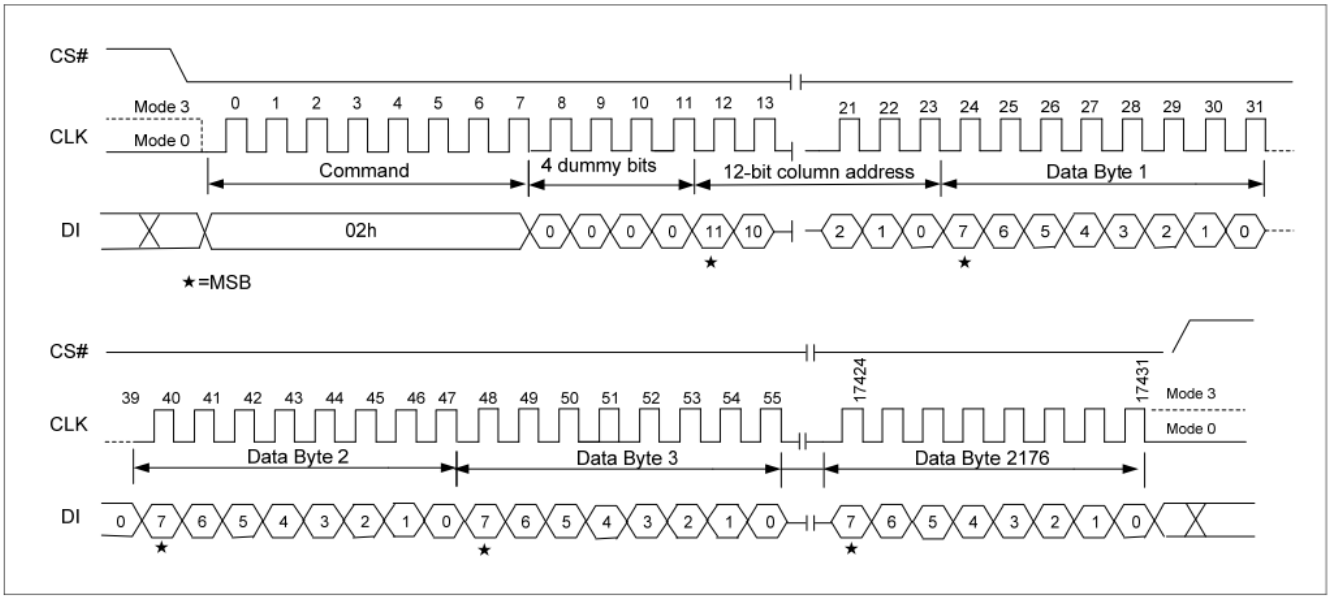
The 3rd step is to issue a PROGRAM EXECUTE (10h) command to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and an 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation is shown in Figure 21.

During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

NOTE : The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. In addition, pages must be sequentially programmed within a block.

7.7.2 Program Load (PL) (02H)

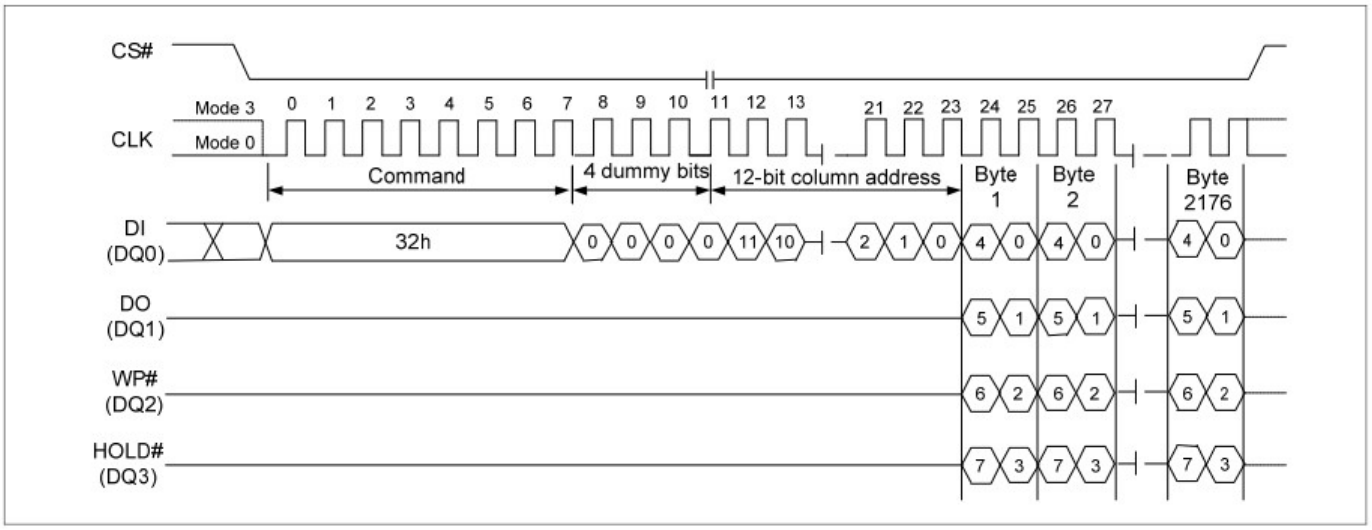
Figure17. Program Load Sequence Diagram



7.7.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the program load x4 command.

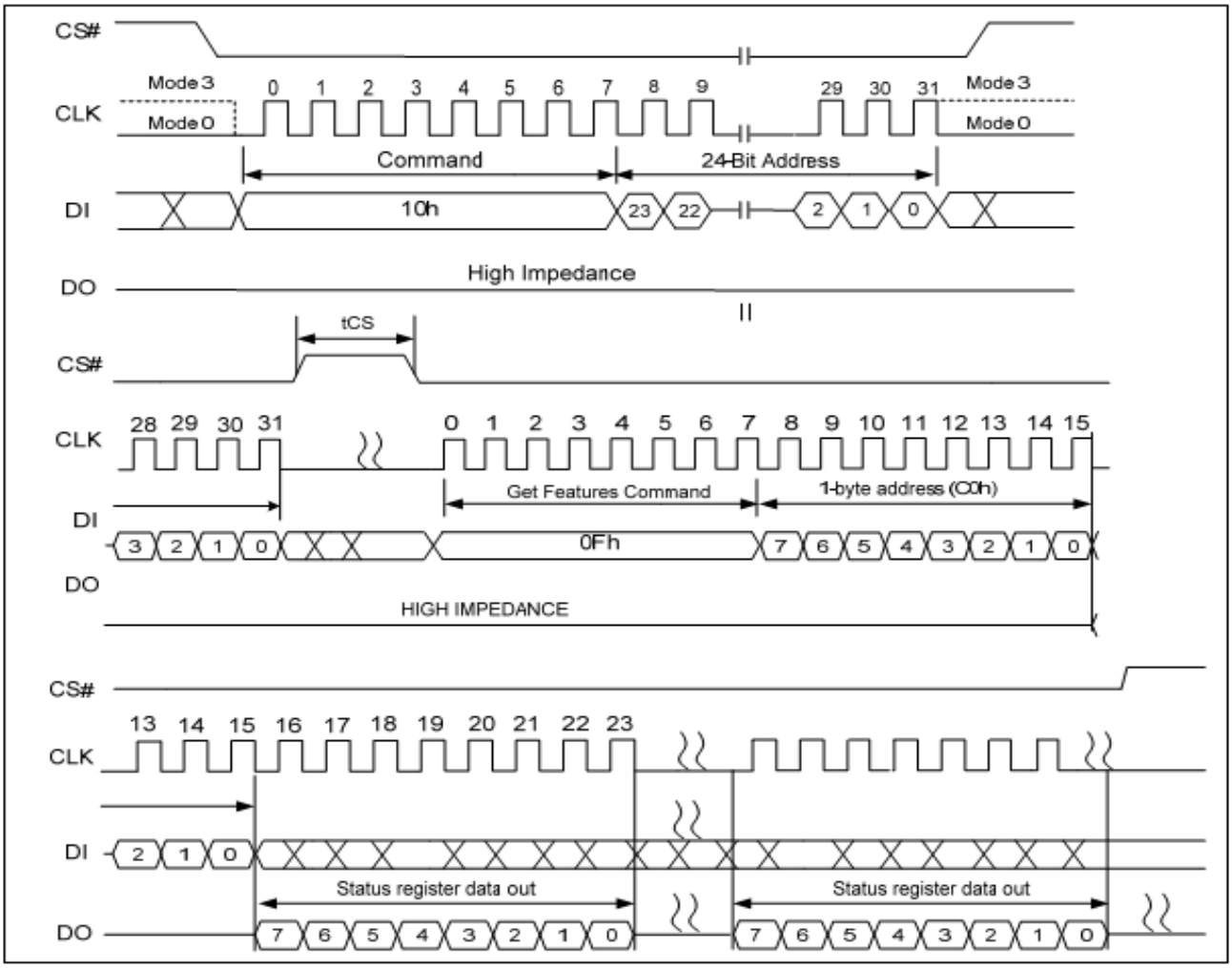
Figure17. Program Load x4 Sequence Diagram



7.7.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation is shown in Figure17. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure18. Program Execute Sequence Diagram



7.7.5 Internal Data Move

The Internal Data Move command sequence programs or replaces data in a page with existing data. The Internal Data Move command sequence is as follows:

- 13H (PAGE READ TO CACHE)
- 84H/C4H/ 34H/72H(PROGRAM LOAD RANDOM DATA : Optional)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

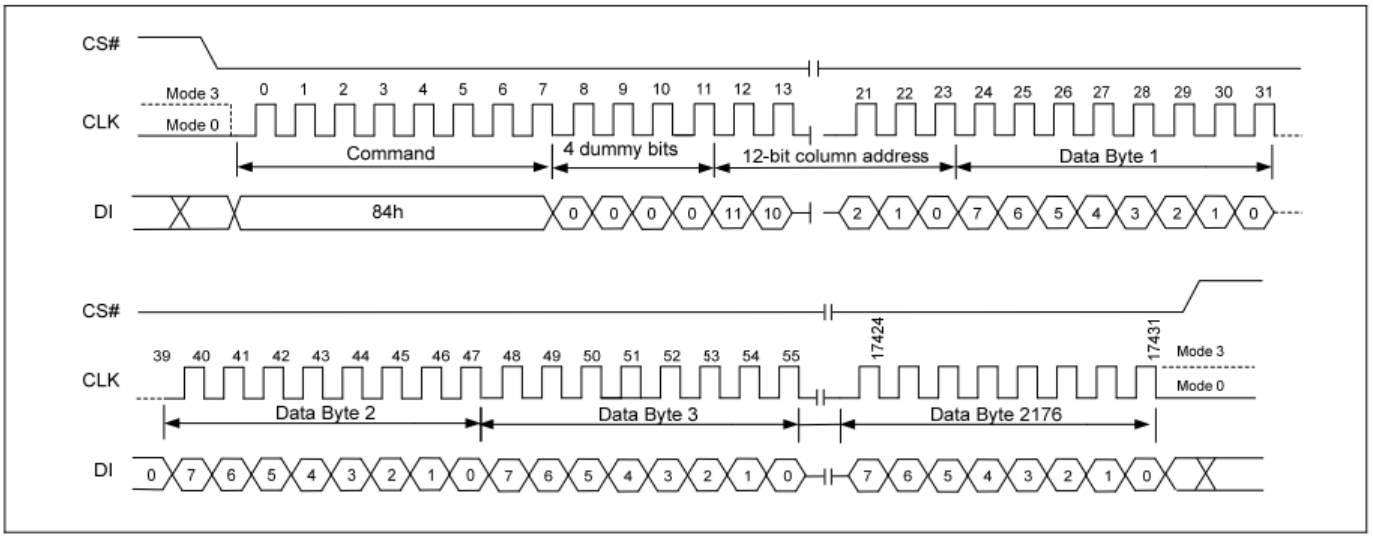
Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command can be issued, if user wants to update bytes of data in the page.

This command consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address. New data is loaded in the 12-bit column address. If the RANDOM DATA is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, then a PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

7.7.6 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

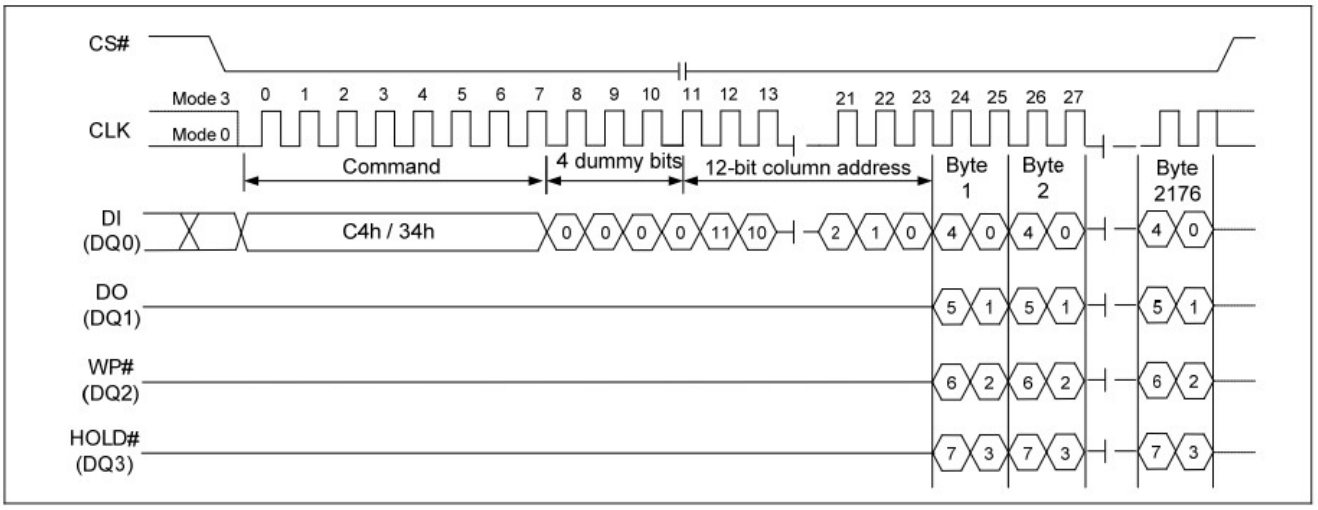
Figure20. Program Load Random Data Sequence Diagram



7.7.7 Program Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the program load random data x4 command.

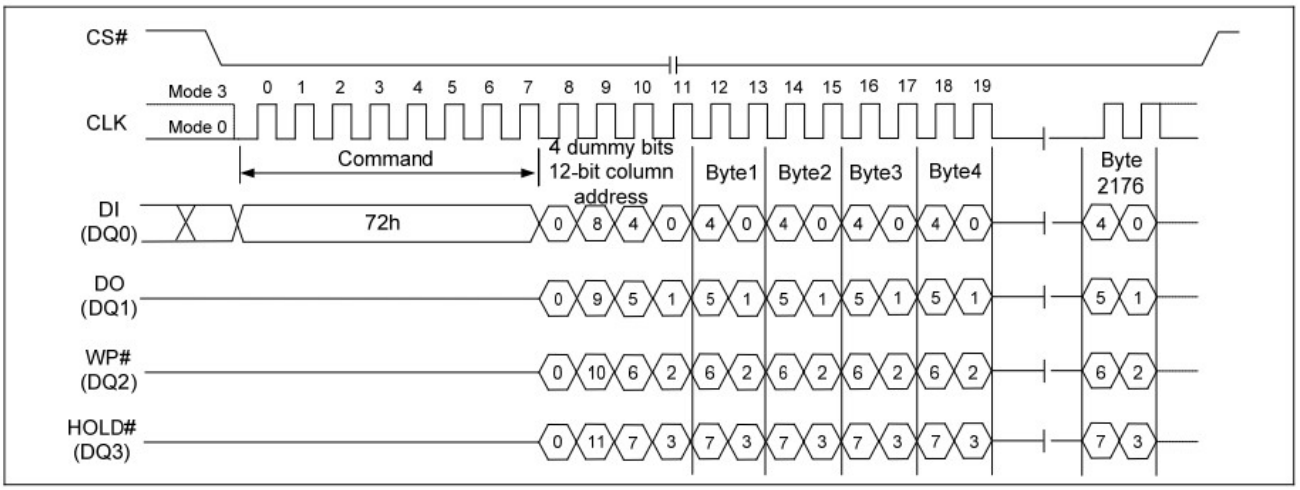
Figure21. Program Load Random Data x4 Sequence Diagram



7.7.8 Program Random Quad IO (72H)

The Program Load Random Data Quad IO command (72H) is similar to the Program Load Random Data x4 command (C4H) but with the capability to input the 4 dummy bits, and a 12-bit column address by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0 [0]) must be set to enable for the program load random data x4 command.

Figure22. Program Load Random Data Quad IO Sequence Diagram



7.8 ERASE OPERATIONS

7.8.1 Block Erase (D8H)

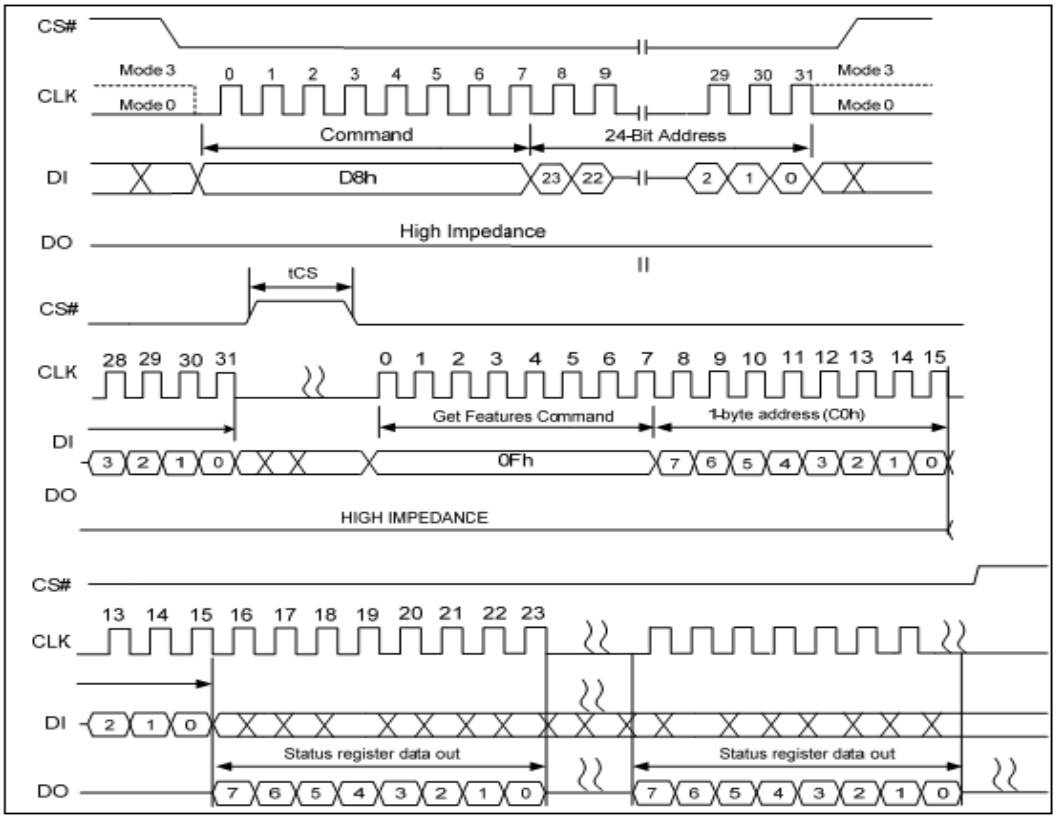
The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block,2176 bytes per page (2048+128 bytes).Each block is 136 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 6 dummy bits followed by an 16-bit row address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation (refer to the Status Register section).

Note: When a BLOCK ERASE operation is in progress, user can issue READ FROM CACHE commands (03H/0BH/3BH/6BH/BBH/EBH) to read the data in the cache.

Figure23. Block Erase Sequence Diagram



7.9 RESET Operation

The RESET (FFh) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state.

7.9.1 RESET (FFh)

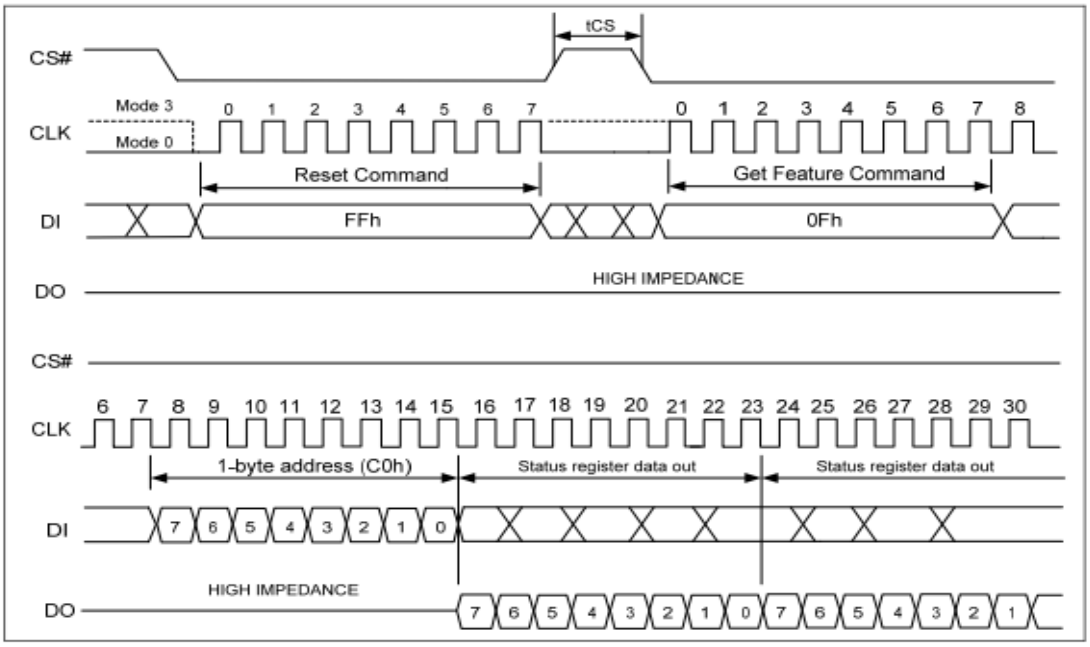


Figure 26 RESET (FFh) Timing

7.10 Write Protection

The WPS feature (B0[5]) is used to select block protection method.

If WPS=0, the write protection will be determined by the combination of CMP, INV, BP[2:0] bits in the Block Lock Register (A0).

Table 6 Block Lock Register Block Protect Bits (WPS=0)

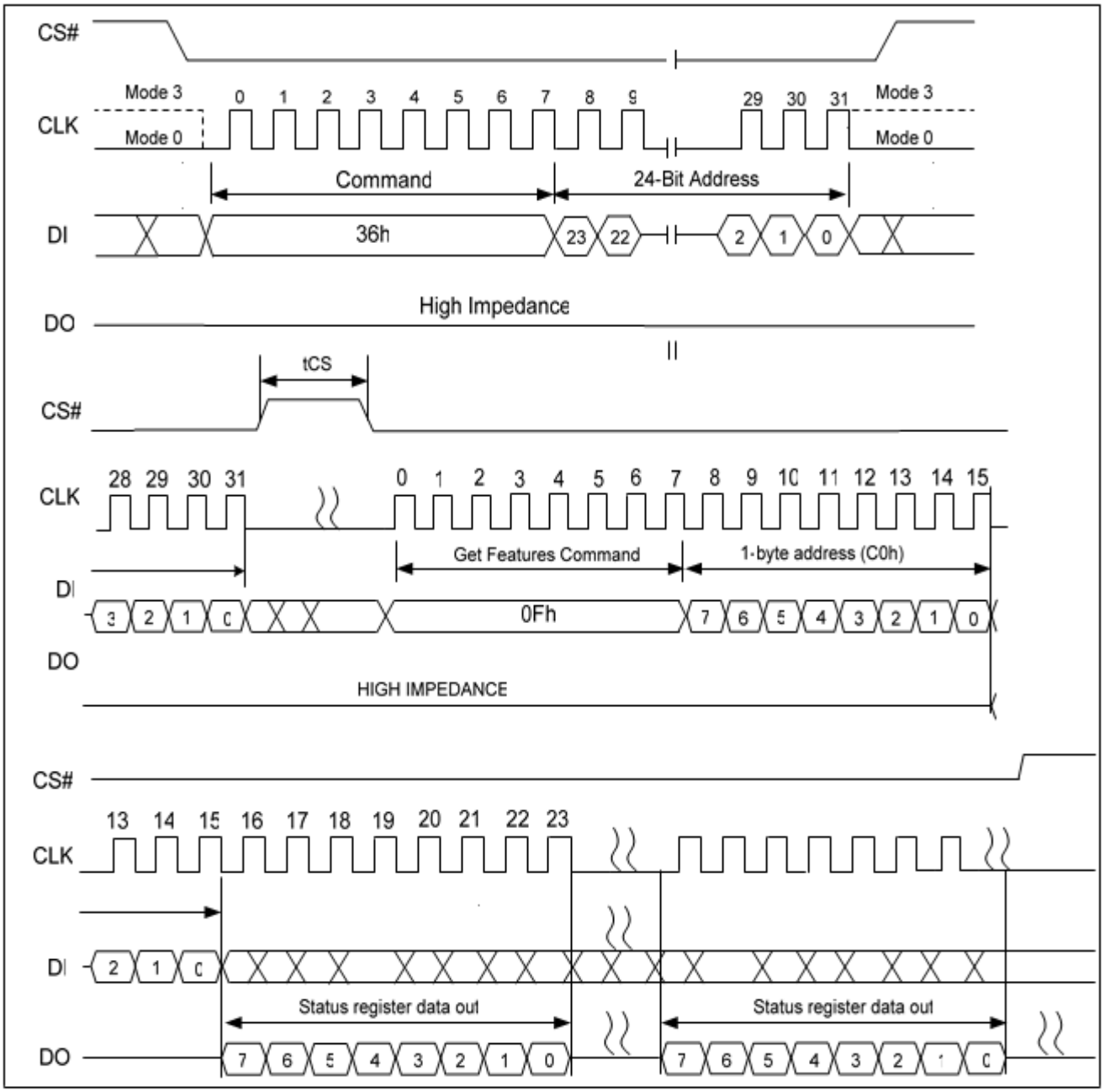
CMP	INV	BP2	BP1	BP0	Protected Row Address	Protected Rows
x 0	x 0	0 0	0 0	0 1	None 0FC00h~0FFFFh	None Upper 1/64
0	0	0	1	0	0F800h~0FFFFh	Upper 1/32
0	0	0	1	1	0F000h~0FFFFh	Upper 1/16
0	0	1	0	0	0E000h~0FFFFh	Upper 1/8
0	0	1	0	1	0C000h~0FFFFh	Upper 1/4
0	0	1	1	0	08000h~0FFFFh	Upper 1/2
x	x	1	1	1	All (default)	All (default)
0	1	0	0	1	00000h ~ 003FFh	Lower 1/64
0	1	0	1	0	00000h ~ 007FFh	Lower 1/32

0	1	0	1	1	00000h ~ 00FFFh	Lower 1/16
CMP	INV	BP2	BP1	BP0	Protected Row Address	Protected Rows
0	1	1	0	0	00000h ~ 01FFFh	Lower 1/8
0	1	1	0	1	00000h ~ 03FFFh	Lower 1/4
0	1	1	1	0	00000h ~ 07FFFh	Lower 1/2
1	0	0	0	1	00000h~0FBFFh	Lower 63/64
1	0	0	1	0	00000h~0FF7Fh	Lower 31/32
1	0	0	1	1	00000h~0EFFFh	Lower 15/16
1	0	1	0	0	00000h~0DFFFh	Lower 7/8
1	0	1	0	1	00000h~0BFFFh	Lower 3/4
1	0	1	1	0	00000h~0003Fh	Block0
1	1	0	0	1	00400h~0FFFFh	Upper 63/64
1	1	0	1	0	00800h~0FFFFh	Upper 31/32
1	1	0	1	1	00FC0h~0FFFFh	Upper 15/16
1	1	1	0	0	02000h~0FFFFh	Upper 7/8
1	1	1	0	1	04000h~0FFFFh	Upper 3/4
1	1	1	1	0	00000h~0003Fh	Block0

If WPS=1, the INDIVIDUAL BLOCK LOCK is enabled. The INDIVIDUAL BLOCK LOCK provides an alternative way to protect the memory array from adverse Erase/Program. The INDIVIDUAL BLOCK LOCK bits are volatile bits. The default values after power up or after Reset are 1, so the entire memory array is being protected.

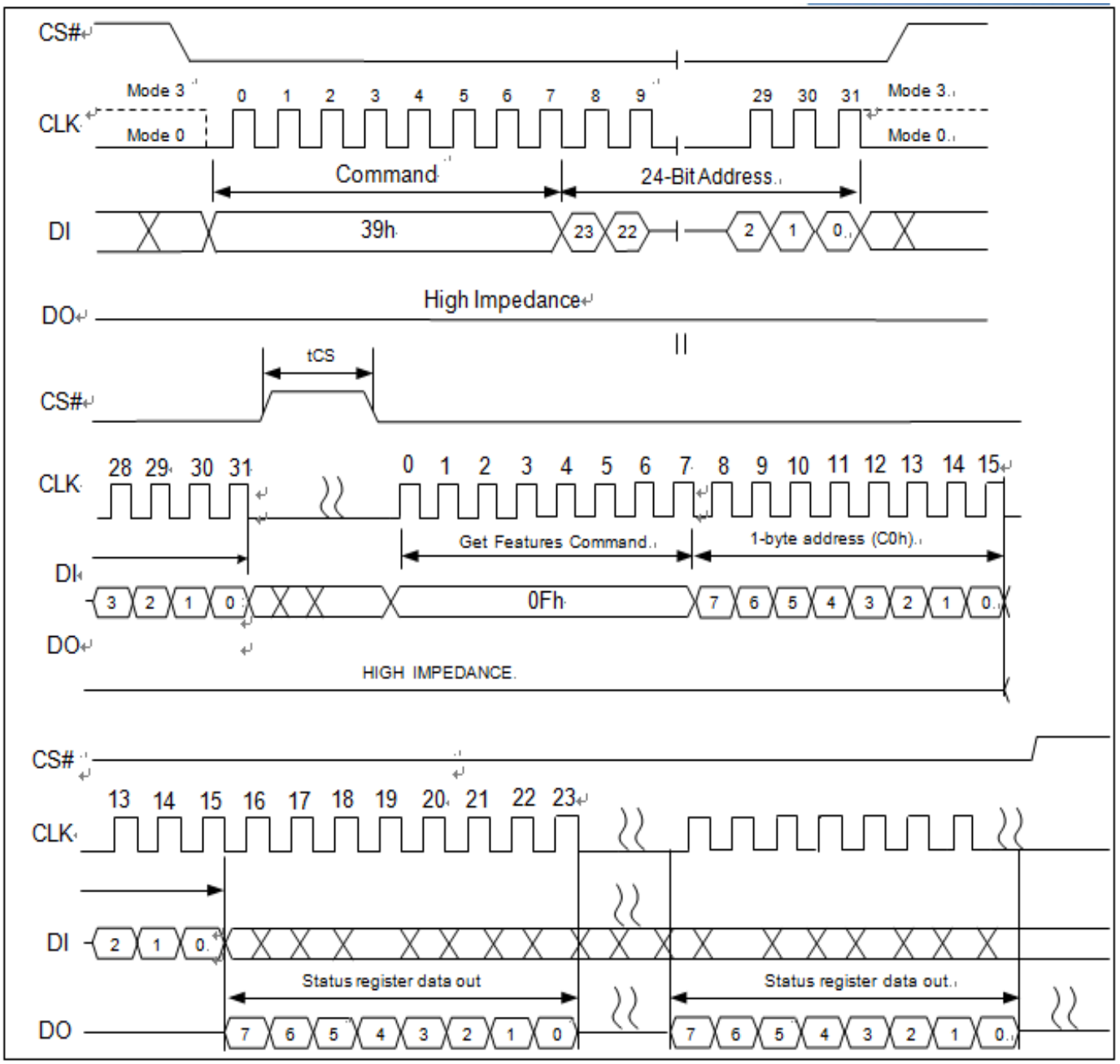
7.10.1 INDIVIDUAL BLOCK LOCK (36h)

The INDIVIDUAL BLOCK LOCK command requires a 24-bit address consisting of 2-bit '0' followed by a 10-bit block address (RA<5:0> is don't care) and 12 dummy bits . After the addresses are registered, the device starts setting the corresponding INDIVIDUAL BLOCK LOCK bit, and is busy for tLCK time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.



7.10.2 INDIVIDUAL BLOCK UNLOCK (39h)

The INDIVIDUAL BLOCK UNLOCK command requires a 24-bit address consisting of 2bit '0' followed by a 10-bit block address (RA<5:0> is don't care) and 12 dummy bits. After the addresses are registered, the device starts resetting the corresponding INDIVIDUAL BLOCK LOCK bit, and is busy for tLCK time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.



7.10.3 READ BLOCK LOCK (3Dh)

The READ BLOCK LOCK command can be used to read out the lock bit of a specific block. The READ BLOCK LOCK command requires a 24-bit address consisting of 2-bit '0' followed by a 10- bit block address (RA<5:0> is don't care) and 12 dummy bits. The Block Lock bit value will be shifted out on the DO pin at the falling edge of CLK shown in Figure 29. If the least significant bit (LSB) is 1, the corresponding block is locked; if LSB=0, the corresponding block is unlocked, ERASE/PROGRAM operation can be performed.

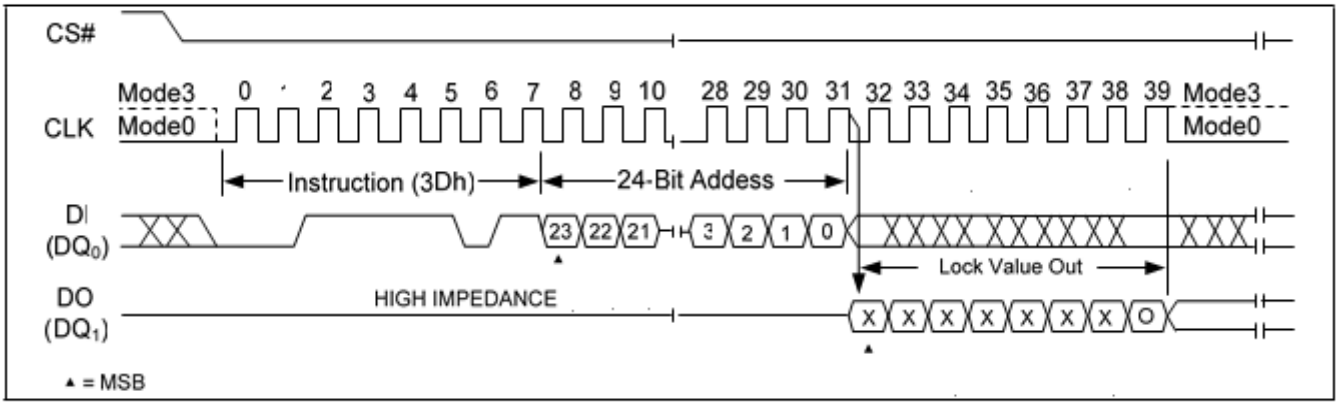


Figure 29 Read Block Lock Command (3Dh) Timing

7.10.4 GLOBAL BLOCK LOCK (7Eh)

All Block Lock bits can be set to 1 by the GLOBAL BLOCK LOCK instruction. After CS# being driven high as shown in Figure 30, the device starts setting all the INDIVIDUAL BLOCK LOCK bits, and is busy for tLCK time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

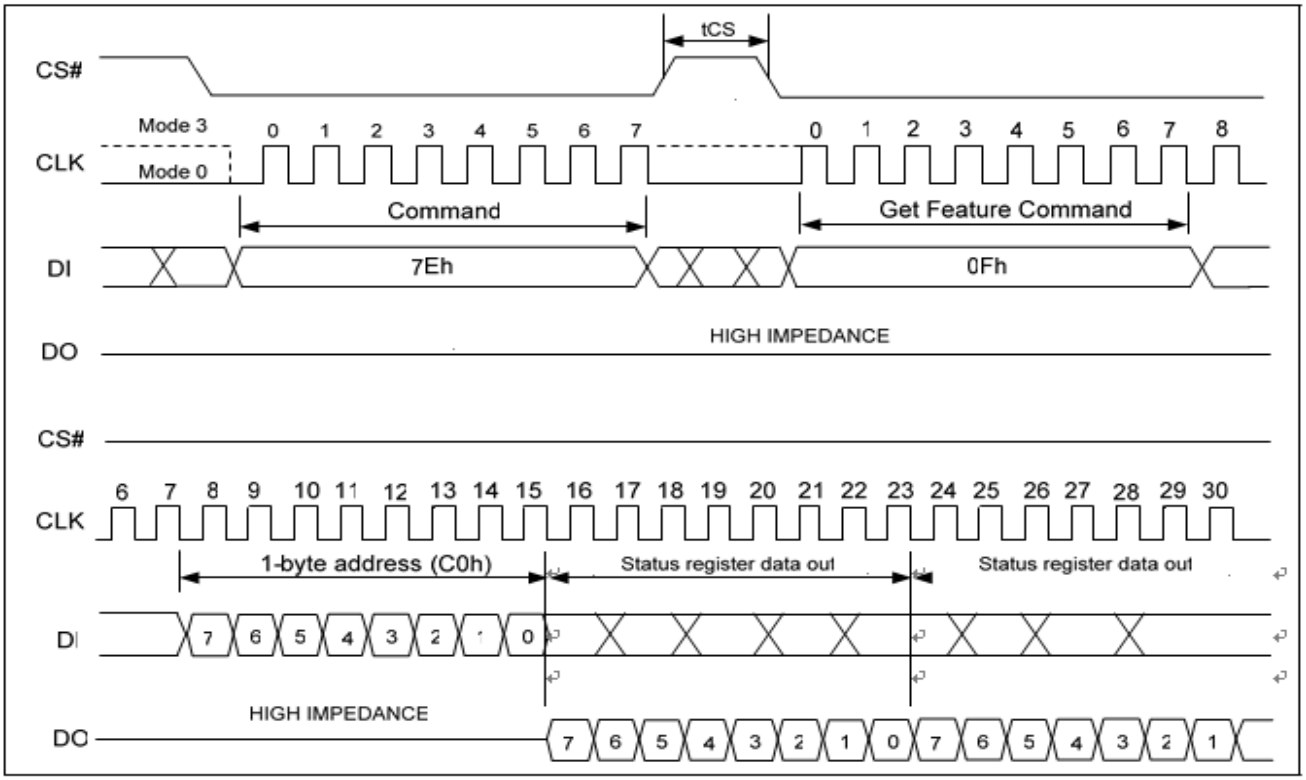


Figure 30 GLOBAL BLOCK LOCK (7Eh) Timing

7.10.5 GLOBAL BLOCK UNLOCK (98h)

All Block Lock bits can be cleared to 1 by the GLOBAL BLOCK LOCK instruction. After CS# being driven high as shown in Figure 31, the device starts setting all the INDIVIDUAL BLOCK LOCK bits, and is busy for tLCK time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

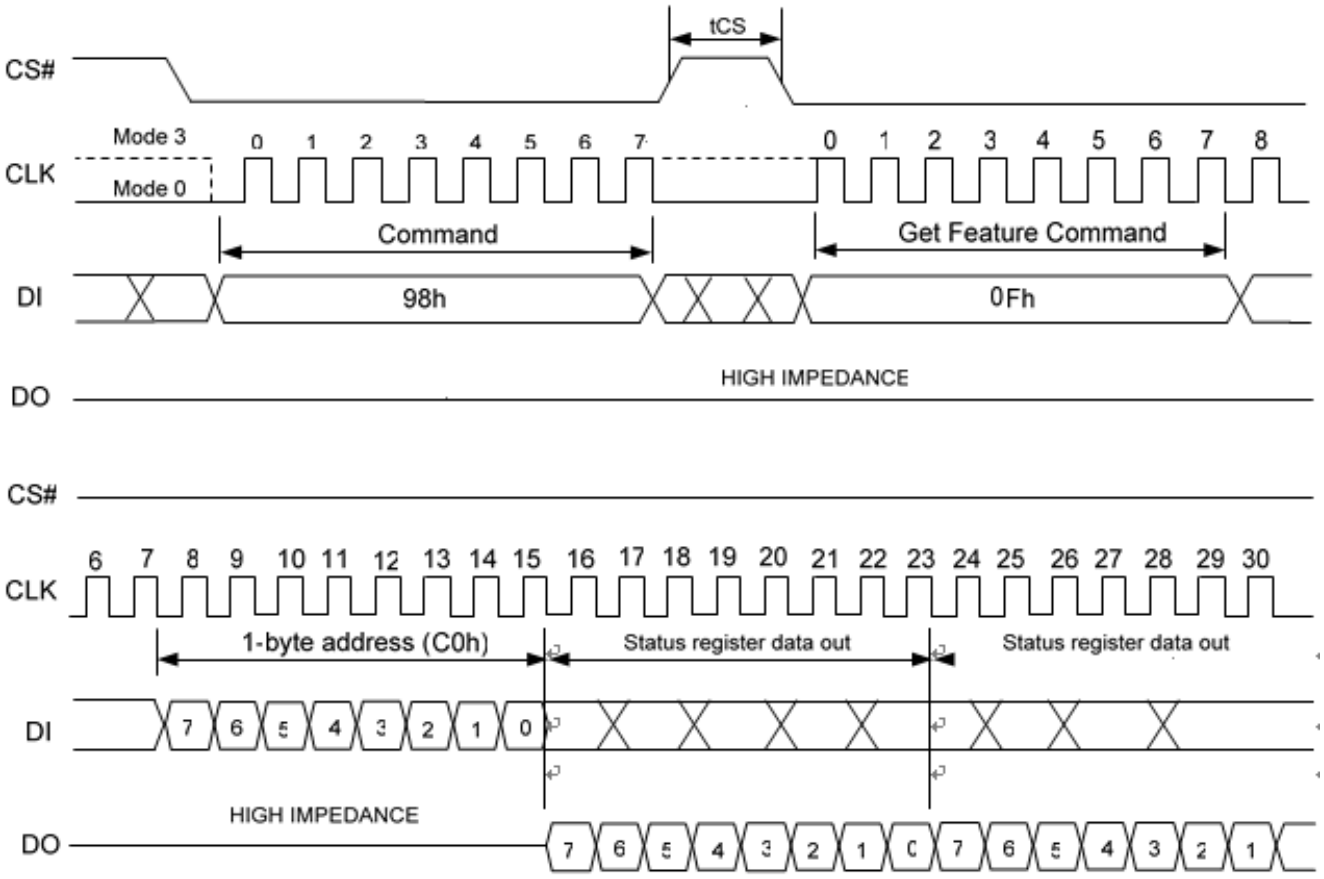


Figure 31 GLOBAL BLOCK UNLOCK Command (98h) Timing

8. Status Register

The device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0h (see Feature Operation).

Table 7 Status Register Bit Description

Bit	Bit Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	WRITE ENABLE Latch	This bit indicates the current status of the WRITE ENABLE latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit indicates that PROGRAM EXECUTE 、 PAGE READ 、 BLOCK ERASE、RESET、GLOBAL BLOCK LOCK/UNLOCK and INDIVIDUAL BLOCK LOCK/UNLOCK is in progress.
ECCS1 ECCS0	ECC Status	ECCS provides ECC Status as follows: 00b = No bit errors were detected during the previous read algorithm. 01b = bit errors were detected and corrected, error bit number = 1~7. 10b = Internal error was detected and the data not promised correctly. 11b = 8bit errors were detected and corrected, error bit number is going to exceed the tolerance. Bit errors cannot be detected and corrected if their number exceeds the tolerance. Therefore, block data should be refreshed when ECC status is equal to 11b. ECCS is set to 00b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECCS is invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN).

9. OTP Region

The device offers a protected, One-Time Programmable NAND Flash memory area. Eight full pages (2176 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 00h–07h can be programmed in sequential order. The PROGRAM LOAD (02H) and PROGRAM EXECUTE (10H) commands can be used to program the pages. Also, the PAGE READ (13H) command and READ FROM CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh) commands can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

OTP Access

To access OTP, perform the following command sequence:

- Issue the SET FEATURES command (1Fh) to set OTP_EN
- Issue the PAGE PROGRAM (if OTP_EN=1) or PAGE READ command

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see the following table.

OTP Protect

- Issue the SET FEATURES command (1FH) to set OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

Table 8 OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

10. Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

All initial bad blocks were mapped to the end of block address during the shipment, ie, all initial bad blocks will be seen starting from Block #1023 reversely.
Additional bad block may develop with use, but this kind of bad blocks will not be mapped to the end of block address .

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 9 Error Management Details

Description	Requirement
Minimum number of valid blocks (N_{VB})	1003
Total available blocks per die	1024
First spare area location	Byte 2048
Bad-block mark	Non FFh

11. ECC Protection

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH).
- Set the feature bit ECC_EN as you want:

1. To enable ECC, Set ECC_EN to 1.
2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below.
- ECC can protect according main and spare areas. WRITEs to the ECC area are ignored.

Power on Read without internal ECC:

The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. However, the data is not promised correctly with ECC disabled.

Table 10 ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC Protected	Number Of Bytes	Area	Description
000H	1FFH	Yes	512	Main 0	User data 0
200H	3FFH	Yes	512	Main 1	User data 1
400H	5FFH	Yes	512	Main 2	User data 2
600H	7FFH	Yes	512	Main 3	User data 3
800H	803H	No	4		800H is reserved for bad block mark
804H	805H	Yes	2	Spare 0	User meta data I
806H	812H	Yes	13	Spare 0	ECC for main/spare 0
813H	814H	Yes	2	Spare 1	User meta data I
815H	821H	Yes	13	Spare 1	ECC for main/spare 1
822H	823H	Yes	2	Spare 2	User meta data I
824H	830H	Yes	13	Spare 2	ECC for main/spare 2
831H	832H	Yes	2	Spare 3	User meta data I
833H	83FH	Yes	13	Spare 3	ECC for main/spare 3
840H	87FH	No	64	Spare 4	User meta data II

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Operating Temperature	-40°C to +85°C
Storage Temperature Voltage on I/O Pin with Respect to Ground	-65°C to +150°C -0.5V to 4.0V
V_{CC}	-0.5V to 4.0V

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

12.2 Pin Capacitance

Applicable over recommended operating range from: T_A = 25°C, f = 1 MHz.

Symbol	Test Condition	Max	Units	Conditions
C	Input Capacitance	6	pF	V_{IN} = 0V
$C^{(1)\ OUT}$	Output Capacitance	8	pF	V_{OUT} = 0V

Note: 1. characterized and is not 100% tested.

12.3 Power-up and Power-Down Timing

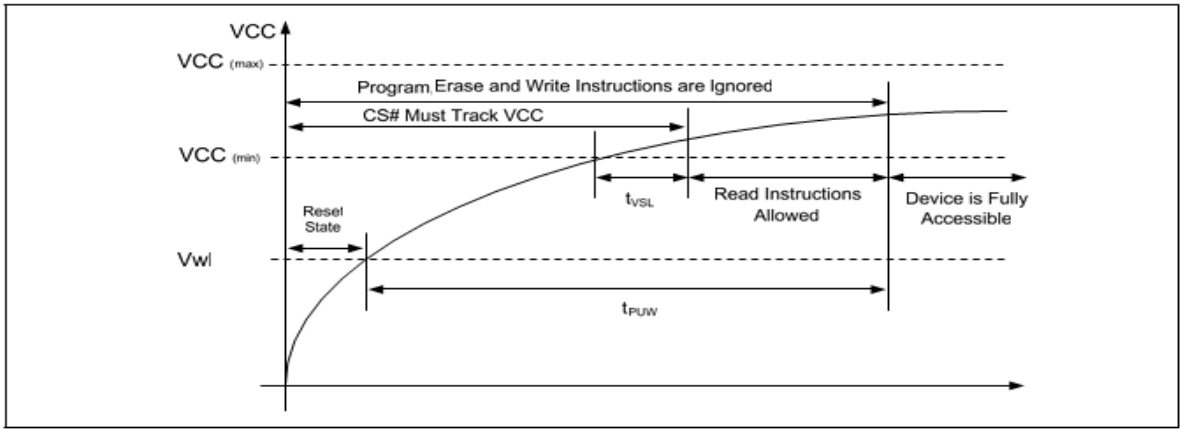


Figure 32 Power-On Timing

Table 11 Power-On Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to CS# Low	t_{VSL}	1		Ms
Time Delay Before Write Instruction	t_{PUW}	6		ms
Write Inhibit Voltage	VWI		2.5	V

12.4 DC Electrical Characteristics

Table 12 DC Characteristics

Applicable over recommended operating range from: TA = -40°C to 85°C, VCC = 2.7V to 3.6V, (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
VCC	Supply Voltage		2.7		3.6	V
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	V_{CC}=3.6V, CS# = VCC, V_{IN} = VSS or VCC			70	µA
I_{CC2}	Operating Current	CLK=0.1VCC/0.9VCC F_{CLK}=108MHz			40	mA
V (1)	Input Low Voltage		-0.5		0.2V_{CC}	V
V	Input High Voltage		0.7V		V +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC}-0.2			V

Notes:

1. V_{IL} min and V_{IH} max are reference only and are not tested.

12.5 AC Measurement Conditions

Table 13 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

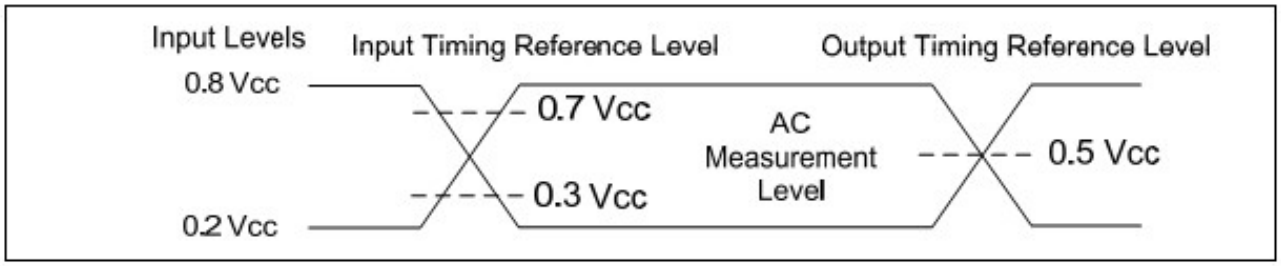


Figure 33 AC Measurement I/O Waveform

12.6 AC Electrical Characteristics

Table 14 AC Characteristics

Applicable over recommended operating range from: TA = -40°C to 85°C, VCC = 2.7V to 3.6V

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_C	Serial Clock Frequency for: all command			108	MHz
t_{CH1}(1)	Serial Clock High Time	4.5			ns
t_{CL1}(1)	Serial Clock Low Time	4.5			ns
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
$t_{(2)SHQZ}$	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			15	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			15	ns
t_{CLQV}	Output Valid from CLK			8	ns
t_{WHSL}	WP# Setup Time before CS# Low	20			ns
t_{SHWL}	WP# Hold Time after CS# High	100			ns
t_{IO_skew}	First IO to last IO data valid time			600	ps

Notes:

1. $T_{CH1}+T_{CL1} >= 1 / F_C$;
2. characterized and not 100% tested.

Table 15 Performance Timing

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
tRST	CS# High to Next Command After Reset(FFh)			500	µS
tRD	Page Read From Array (with ECC)			240	µS
	Page Read From Array (without ECC)			120	
tPROG	Page Program (with ECC)			1400	µS
	Page Program (without ECC)		300	700	
tERS	Block Erase		3	10	ms

13. SPI Serial Timing

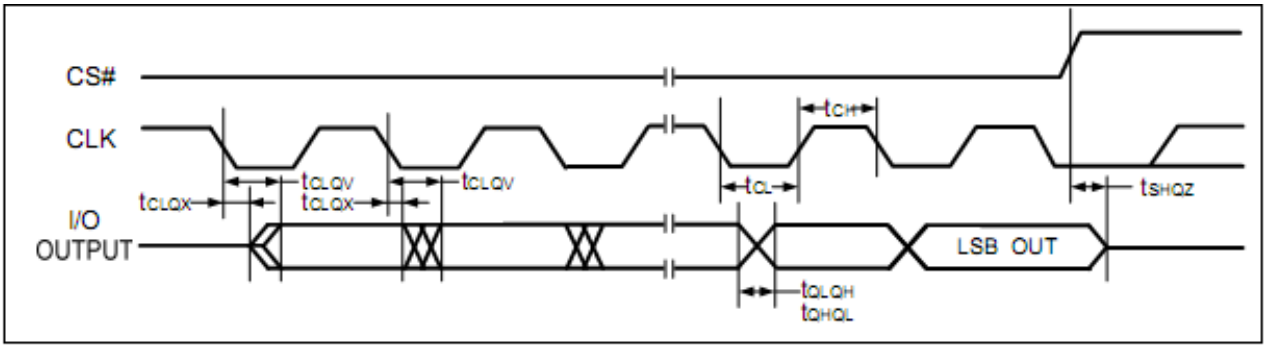


Figure 34 Serial Output Timing

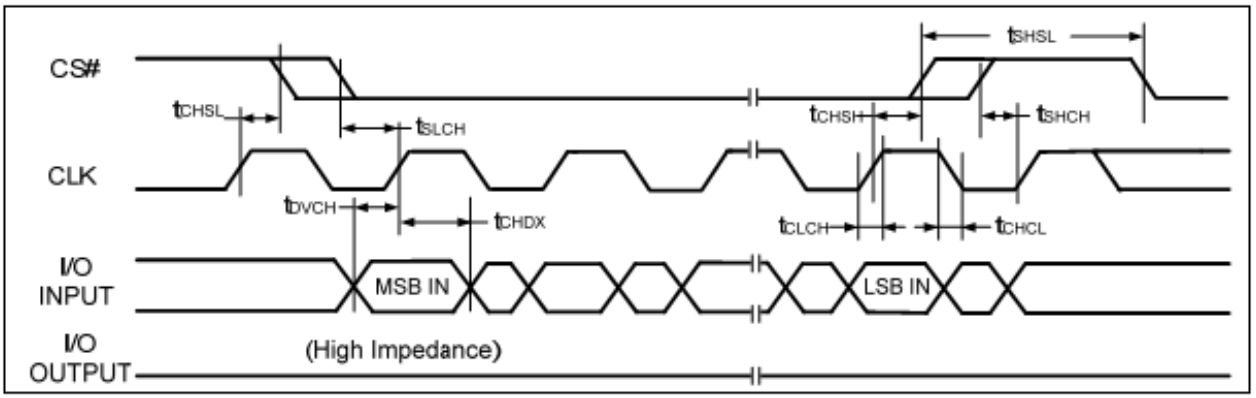


Figure 35 Serial Input Timing

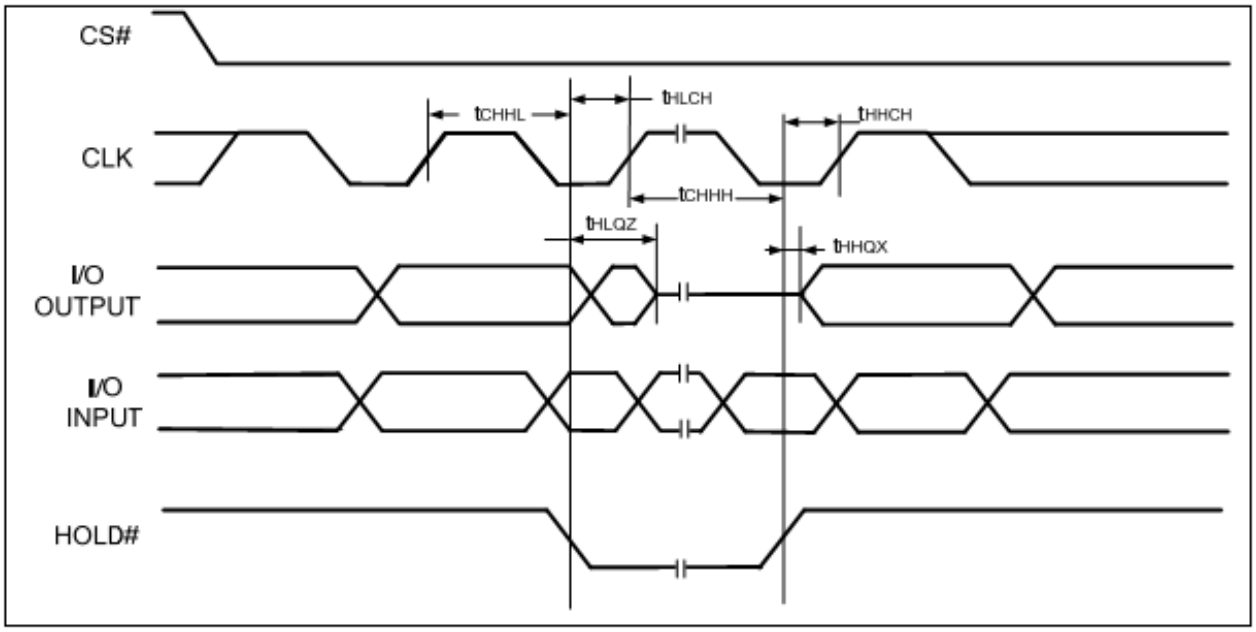


Figure 36 Hold Timing

14. ORDERING INFORMATION

PN 26G 01 A XX I U G

Company Prefix

PN = XTX

Product Family

26G = 2.7~ 3.6V Serial NAND Flash Memory with 2Kb pages, Standard / Dual/ Quad SPI

Product Density

01 = 1G bit
02 = 2G bit
04 = 4G bit

Generation

A = 1st
…

Product Package

WS = 8-pin WSON(8x6mm)
BG = 24 Ball TFBGA(8x6mm)

Product Temperature

I = Industrial (-40℃ to +85℃)
C = Commercial (0℃ to +70℃)

Product Carrier

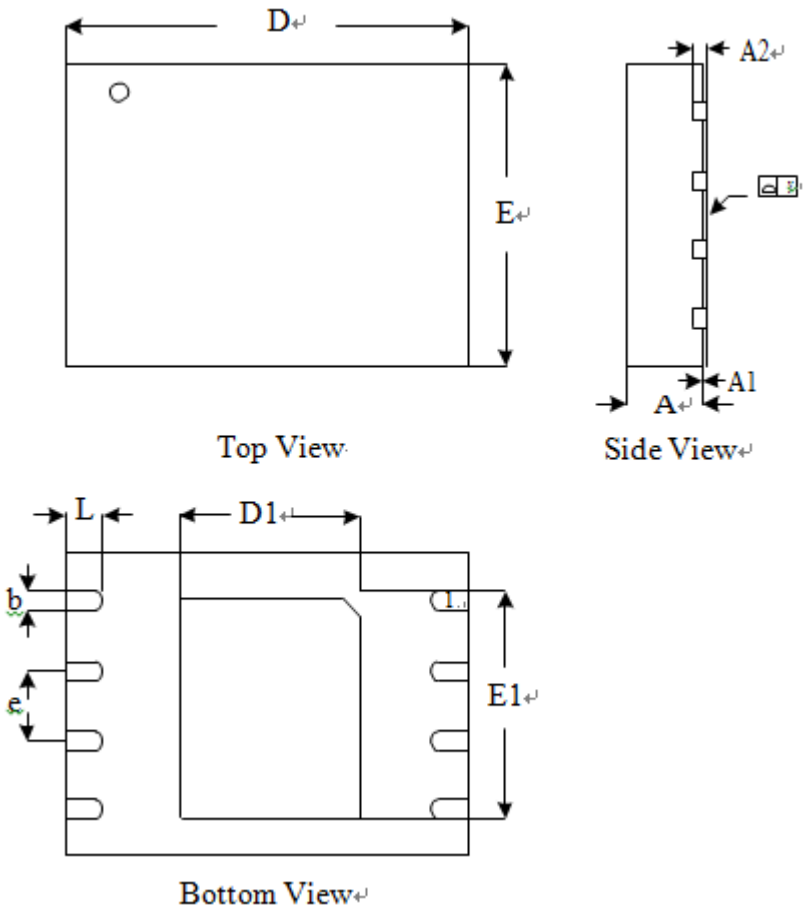
U = Tray
T = Tape and Reel

Green Code

R = RoHS Compliant Package
G = Green/Reach Package

15. PACKAGE INFORMATION

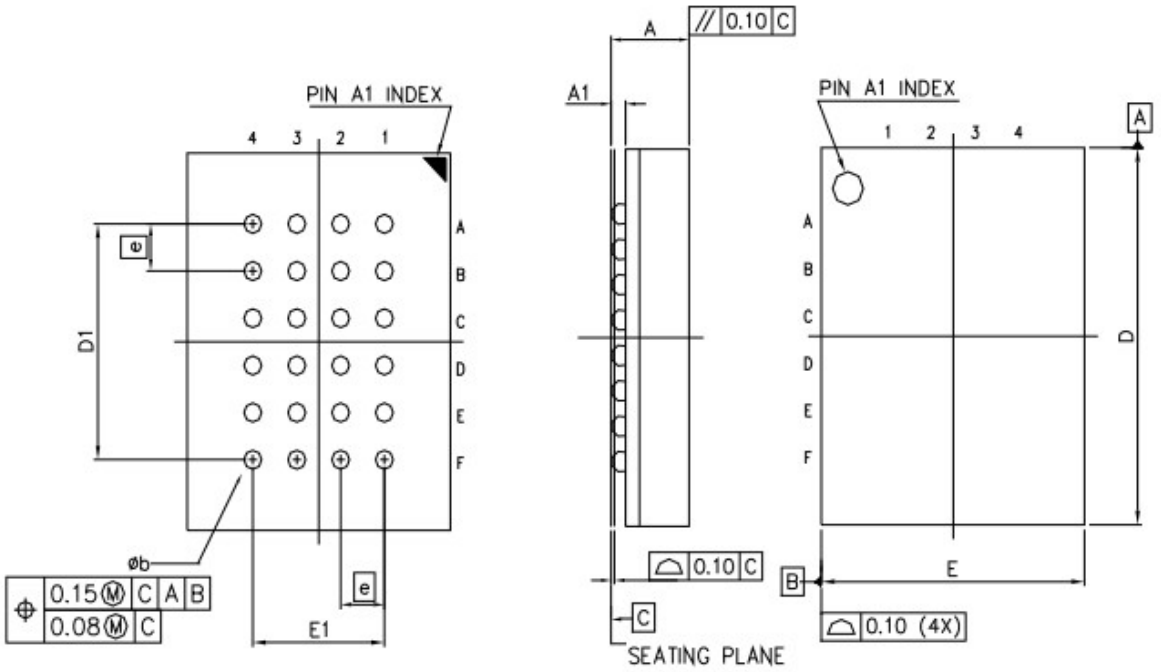
15.1 8-Pad WSON8 (8*6mm)

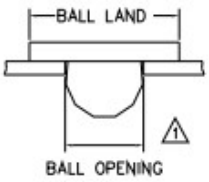


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.70			0.35	7.95	3.25	5.95	4.15		0.00	0.40
	Nom	0.75		0.20	0.40	8.00	3.40	6.00	4.30	1.27		0.50
	Max	0.80	0.05		0.45	8.05	3.50	6.05	4.40		0.05	0.60
Inch	Min	0.028			0.014	0.313	0.128	0.234	0.163		0.00	0.016
	Nom	0.030		0.008	0.016	0.315	0.134	0.236	0.169	0.05		0.020
	Max	0.032	0.002		0.019	0.317	0.138	0.238	0.173		0.002	0.024

15.2 24-Ball TFBGA (8*6mm)





Note:

Ball land: 0.45mm. Ball Opening: 0.35mm

PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	5.00 BSC			0.197 BSC		
E	5.95	6.00	6.05	0.234	0.236	0.238
E1	3.00 BSC			0.118 BSC		
e	1.00 BSC			0.039 BSC		

16. REVISION HISTORY

Version No	Description	Date
A.1.0	Initial Release	2/10/2015
A.1.1	release	4/13/2015
A.1.2	release	5/23/2015
A.1.3	release	9/12/2015
A.1.4	Add 24-Ball TFBGA(6*8mm)	4/1/2016
A1.5	Update ECC_EN bit from B0h bit4 to 90h bit4; tPUW change from 5ms to 6ms on page 38; add initial bad mapping description on page 36 ; Update ECCS0 ECCS1 status description on page 34;	4/5/2017
A1.6	Correct a typo on page2;	4/6/2017
A1.7	Rename company Paragon to XTX & page #11 MID to XTX	May/4/2017