STK3420

Ambient Light Sensor、Proximity Sensor and 3D-Gesture Sensor with Built-in IR LED

Datasheet

Version - 1.0

2015/02/01

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK3420 is an integrated ambient and infrared light to digital converter with a built-in IR LED and I^2C interface. This device provides not only ambient light sensing to allow robust backlight/display brightness control but also infrared sensing to allow proximity estimation and gesture recognition featured with interrupt function.

For ambient light sensing, the STK3420 incorporates a photodiode, timing controller and ADC in a single chip.

For proximity sensing, the STK3420 also incorporates a photodiode, timing controller and ADC in the same chip. The spectral response of STK3420 is optimized for wavelength 940nm infrared light. The STK3420 provides a noise cancellation scheme to highly reject unwanted ambient IR noise.

For gesture recognition, the STK3420 provides multi-photodiodes to distinguish the movement of the object. It can be used to recognize 3D dimensions gesture recognition: left / right / up / down / near / far.

The STK3420 operating voltage range is 2.4V to 3.6V.

Feature

- Integrated ambient light sensor, proximity sensor and 3-D gesture sensor function.

Proximity Sensor

- 16 bits resolution for proximity detection
- Built-in LED driver with flexible setting
  - LED turn-on time : 7 steps IT
  - LED current : 50 / 100 / 150 mA
- Flexible interrupt setting
  - Several interrupt modes meet application requirements.
  - Flag modes are included.
  - Intelligent persistence to speed up the response time : 1 / 2 / 4 / 8 times
- Low noise design
- Ambient IR noise cancellation
  - Immunity to 50Hz/60Hz fluorescent light flicker

Ambient Light Sensor

- Convert ambient light intensity to 16-bit digital data format
- 3rd generation ambient light sensor which closes to human-eye response and suppress IR portion
  - Read the Illuminance directly; unlike conventional solution calculated from two diodes' data
- Flexible digital settings
  - Integration time : 7 steps IT
- Flexible interrupt setting
  - Interrupt while out-of- window
  - Persistence : 1 / 2 / 4 / 8 times
- IR sensing mode

Gesture

- 3-D gesture recognition, left / right / up / down / near / far.
- Background noise cancellation.
- 128 bytes data FIFO.

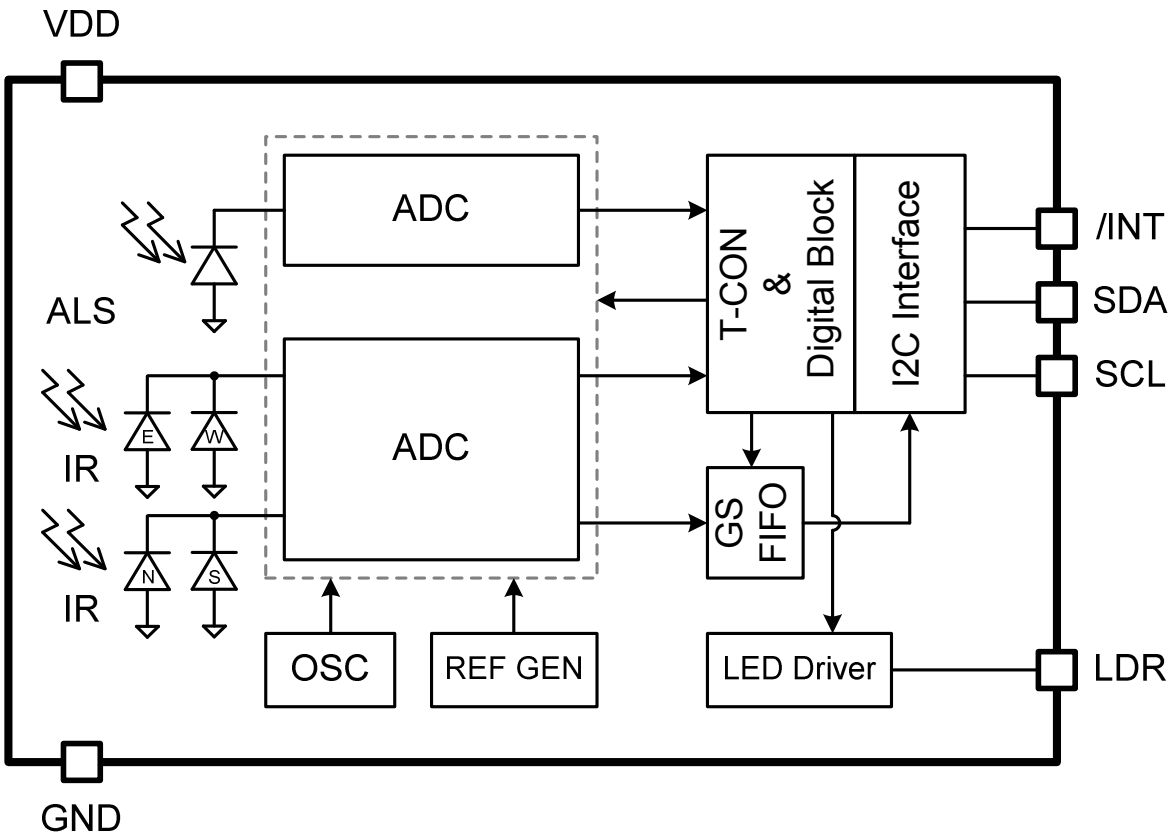
General

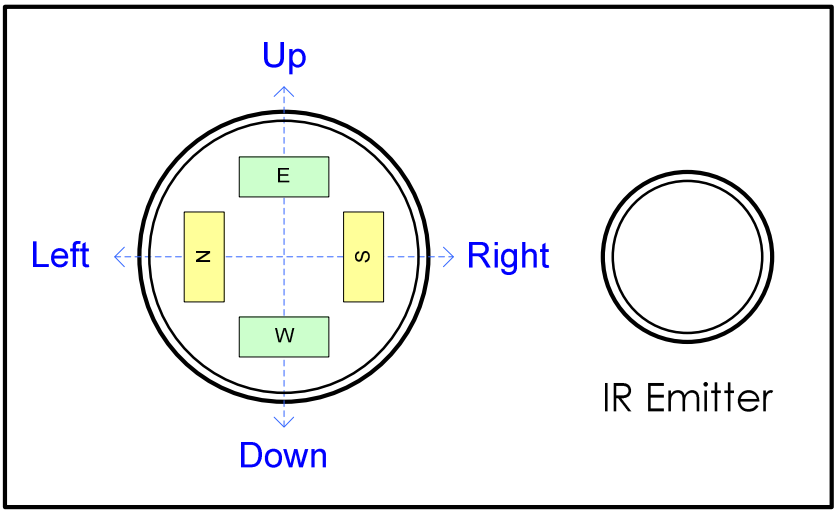
- Fully digital control with I^2C interface
  - 1.7 ~ 3.6V I^2C interface
- Low power design
  - Standby mode
  - Wait mode
- V_{DD} wide operation voltage : 2.4~3.6V
- Excellent temperature compensation: -40 to 85℃
- Package: 3.94x2.36x1.35(mm)
- Lead-free package (RoHS compliant)

Applications

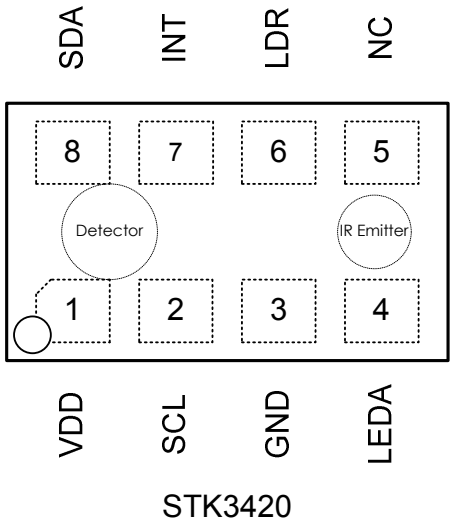
- Mobile Phone, Smart-phone, PDA

2. FUNCTION BLOCK





3. PINOUT DIAGRAM



Top View

4. PIN DESCRIPTION

Pin No.	Pin Name	Dir.	Pin Function
1	VDD	PWR	Power supply: 2.4V to 3.6V.
2	SCL	I	I^2C serial clock line.
3	GND	GND	Ground. The thermal pad is also connected to the GND pin.
4	LEDA	I	Anode of the embedded IR LED, connect to power.
5	NC		No Connect.
6	LDR	I	IR LED driver pin connecting to the cathode of the external IR LED. The sink current of the IR LED driver can be programmed through I^2C.
7	/INT	O	Interrupt pin, LO for interrupt alarming. (Open Drain)
8	SDA	B	I^2C serial data line. (Open Drain)

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connect

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-0.3	—	3.8	V
V_{LEDA}	Voltage of LED's anode	-0.3	—	4.7	V
V_{LDR}	Voltage of LDR			3.8	V
T_a	Operation temperature	-40	—	85	°C
T_s	Storage temperature	-40	—	85	°C

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.4	—	3.6	V
V_{LEDA}	Voltage of LED's anode	2.4	—	4.6	V
f_{I2C}	Clock frequency of I^2C	—	—	400	KHz
T_a	Operation temperature	-40	—	85	°C

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

VDD = VLED = 2.8V, under room temperature 25℃ (unl ess otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Characteristics						
I_{ALS}	ALS only supply current	Note1,2		120		μA
I_{PS}	PS/GS only supply current	Note1,2		260		μA
I_{WAIT}	Supply current at wait state	Note1,2		28		μA
I_{SD}	Shutdown current	Note1,2			2	μA
V_{IH}	Logic high, I^2C	Note6	1.3		VDD	V
V_{IL}	Logic low, I^2C	Note7	—		0.4	V
ALS Characteristics						
λp_1	Peak sensitivity wavelength for ALS			550		nm
ALS_{FSCNT}	Full scale ALS counts				65535	counts
ALS_{DARK}	ALS dark offset	Note2,3,4		0	2	counts
ALS_{SENSE}	ALS sensing tolerance	Note2,3			±10	%
—	Detecting intensity for ALS	Note3				Lux
		Min. (Note9)		0.024		
		Max. (Note10)		6300		
Proximity Characteristics						
λp_2	High sensitivity wavelength range for PS/GS			940		nm
PS/GS_{FSCNT}	Full scale PS/GS counts				65535	counts

PS_{COUNT}	PS counts	Note2	731	860	989	counts
$ILED_{SINK}$	LED sink current	IRDR_LED[1:0] (Note5)				
		00		50		mA
		01		100		mA
		11 (Note8)		150		mA

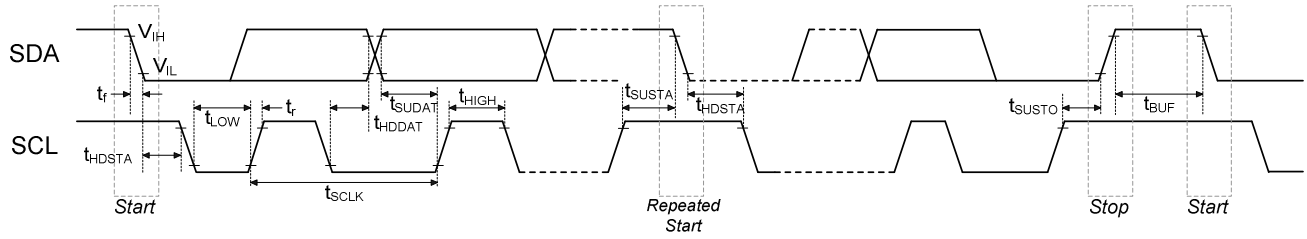
Note 1 : No LED operation current.
Note 2 : IC setting IT_PSGS[3:0] = 4'b0001, IT_ALS[3:0] = 4'b0100, GAIN_ALS[1:0] = 2'b11, IRDR_LED[1:0] = 2'b01. When I_{PS} is tested, all of the GS circuits are enabled.
Note 3 : White LED parallel light source.
Note 4 : $E_{ambient}$ = 0 Lux.
Note 5 : The voltage of LDR pin is fixed at 1V.
Note 6 : I^2C logical high voltage level is specified as worst-case condition when all of the recommended operation supply voltages (VDD) are taken into consideration. The logical high level is different when different supply voltage is applied.
Note 7 : I^2C logical low voltage level is specified as worst-case condition when all of the recommended operation supply voltages (VDD) are taken into consideration. The logical low level is different when different supply voltage is applied.
Note 8 : LED_DIV2 = 1.
Note 9 : IT_ALS[3:0] = 4'b0011, GAIN_ALS[1:0] = 2'b10.
Note 10: IT_ALS[3:0] = 4'b0011, GAIN_ALS[1:0] = 2'b00.

5.2 Timing Chart

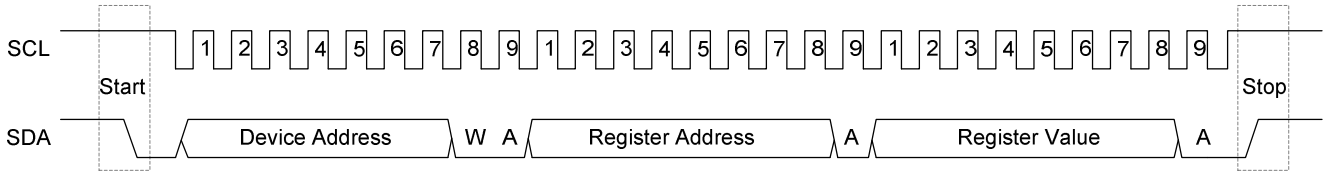
Characteristics of the SDA and SCL I/O

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

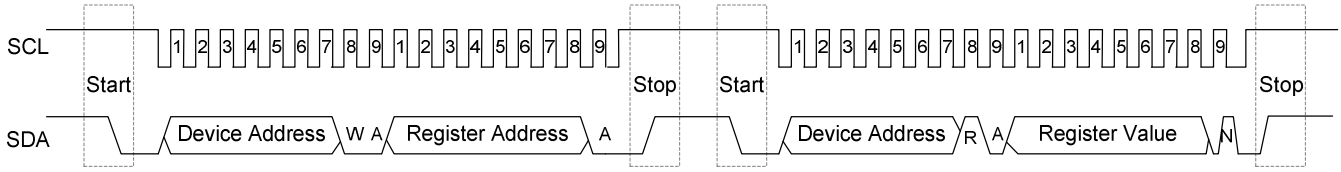
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



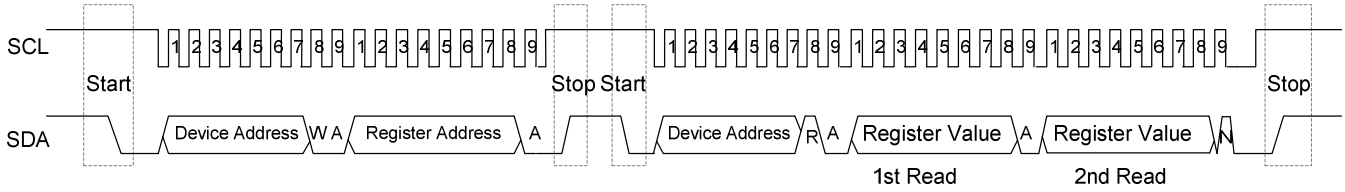
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

6. PRINPICLE OF OPERATION

6.1 Digital Interface

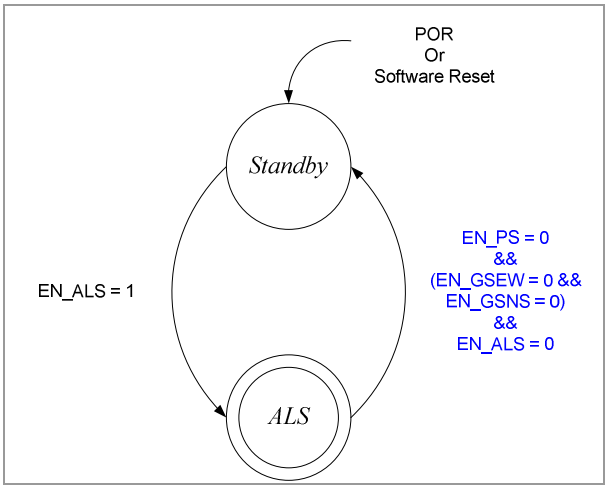
STK3420 contains eight-bit registers accessed via the I^2C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from STK3420. Section 5.2 Timing chart displays the STK3420 I^2C command format for reading and writing operation between host and STK3420.

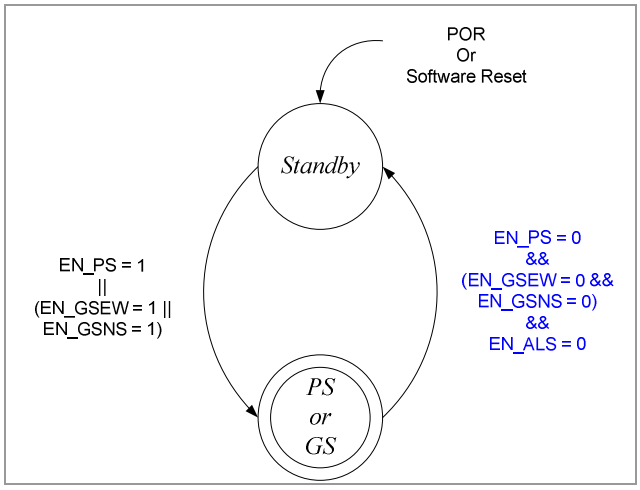
STK3420 provides fixed I^2C slave address of 0x58 using 7 bit addressing protocol.

Slave Address	R/W Command Bit	OPERATION
0x58 (followed by the R/W bit)	0	Write Command to STK3420
	1	Read Data form STK3420

6.2 System Operation

STK3420 has individual ALS and PS/GS operation state, means the ALS and PS/GS of can be operated at the same time. The STK3420 will stay in the *Standby* state only if all the ALS/PS/GS function are disabled.





6.3 ALS Operation

6.3.1 ALS General Operation

The related ALS control bits are summarized below.

ALS Control Bits

General Control	
EN_ALS	Enable ALS function
EN_WAIT_ALS	Enable ALS wait state
IT_ALS[3:0]	ALS integration time
GAIN_ALS[1:0]	ALS gain control
PRST_ALS[1:0]	ALS persistence number

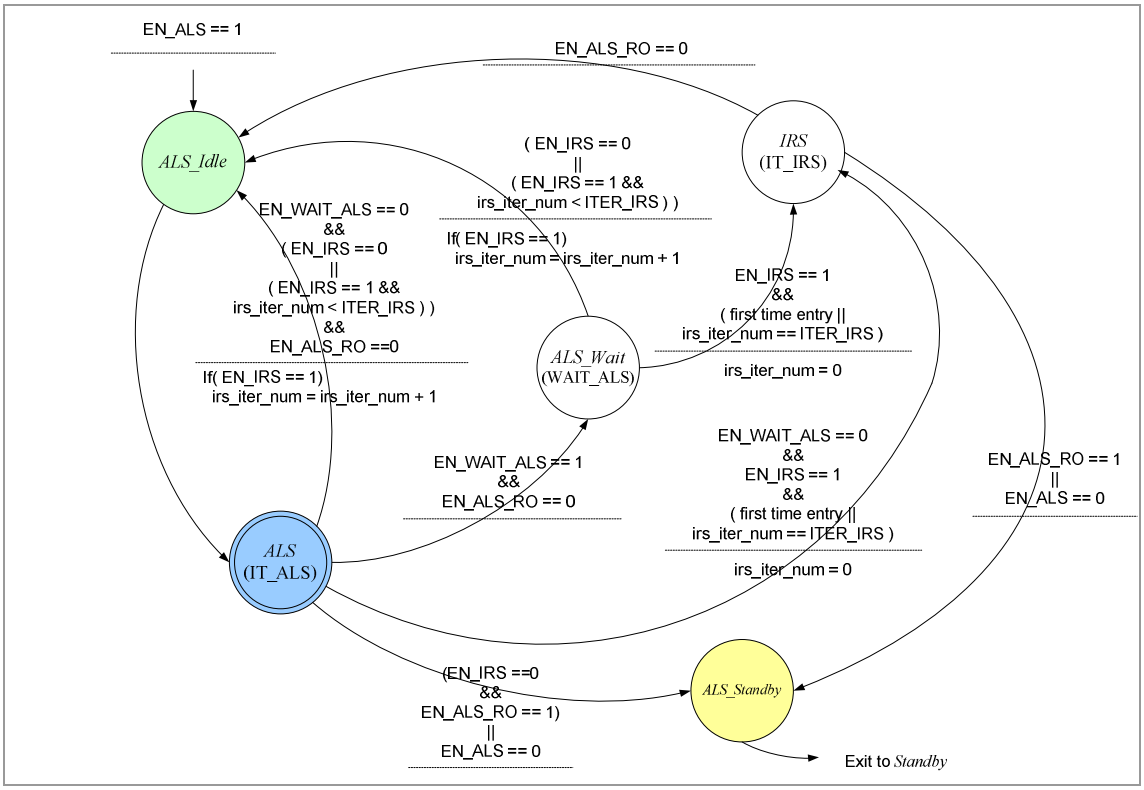
WAIT_ALS[7:0]	ALS wait period
IR-Sensing Control	
EN_IRS	Enable IR-Sensing function
IT_IRS[3:0]	IRS integration time
ITER_IRS[1:0]	IRS iteration numbers
GAIN_IRS[1:0]	IRS gain control
ALS Run-Once Control	
EN_ALS_RO	Enable ALS run once mode
ALS Interrupt Control	
EN_ALS_INT	Enable ALS function interrupt
THDH_ALS[15:0]	ALS out-of-windows high threshold
THDL_ALS[15:0]	ALS out-of-windows low threshold

ALS Data/Status Bits

Data	
DATA_ALS[15:0]	16-bits ALS raw data
DATA_IRS[15:0]	16-bits IRS raw data
Status	
FLG_IRS_DR	Indicate the IRS data ready event
FLG_ALS_DR	Indicate the ALS data ready event
FLG_ALS_INT	Indicate the ALS out-of-windows event

The STK3420 use a photo-diode which spectral response is close to human-eye response to directly sense the ambient light lux level and do not need any complex calculation formula.

The ALS gain GAIN_ALS[1:0] and integration period(IT) IT_ALS[3:0] shall be set before the EN_ALS. ALS wait state can be turned on for saving the operation power. The FLG_ALS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after the DATA_ALS[15:0] is be read out through I^2C.

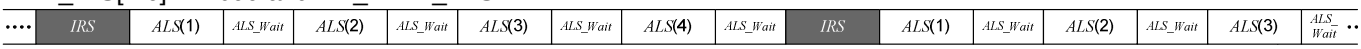


6.3.2 ALS IR-Sensing Mode

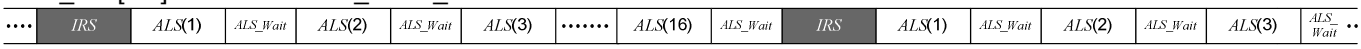
The STK3420 provides IR-Sensing function to sense the IR part energy of the incoming light. The results can be used to distinguish the kind of light source and modify the Lux calculation for this light source.

The IRS function can only be effective when the ALS function is turn on. The EN_IRS shall be set to 1 before EN_ALS is set in order to enable the IRS function. Once the EN_IRS is set to 1, the *IRS* state shall be performed once unconditionally in order to get the first IRS signal as soon as possible no matter what numbers of ITER_IRS is set. The ITER_IRS is used to reduce the overhead of IRS signal acquisition in the whole ALS operation. The IRS signal shall be acquired once every desired numbers set by ITER_IRS[1:0] of ALS signal acquisition. The ITER_IRS can be set to 4/8/16/32.

For example :
ITER_IRS[1:0] = 2'b00 and EN_WAIT_ALS = 1



ITER_IRS[1:0] = 2'b10 and EN_WAIT_ALS = 1



The IRS gain and IT period can be set through GAIN_IRS[1:0] and IT_IRS[3:0]. The FLG_IRS_DR bit shall be asserted once the *IRS* state complete and shall be cleared automatically after the DATA_IRS[15:0] is be read out through I^2C. The FLG_IRS_DR bit also will be reset to 0 if POR/SWRst/EN_IRS = 0/EN_ALS = 0.

6.3.3 ALS Run-Once Mode

STK3420 also provide the ALS run-once function for saving the system power. The run-once function can only be effective when the ALS function is turn on. The EN_ALS_RO shall be set to 1 before EN_ALS is set in order to enable the run-once function. Once the ALS run-once function is enabled, the STK3420 shall perform the whole ALS operation state once, then stay in the *ALS_Standby* state. Keep the EN_ALS_RO = 1 and toggle the EN_ALS bit from 0 to 1 will enable the run-once function again.

6.4.4 ALS Interrupt Description

ALS Out-of-Windows Interrupt
STK3420 provide the ALS data out-of-windows interrupt. Once the EN_ALS_INT is set to 1, then the STK3420 shall issue an ALS interrupt and assert the FLG_ALS_INT bit if the ALS data DATA_ALS[15:0] are outside the user's programmed window defined by THDH_ALS[15:0] and THDL_ALS[15:0]. The FLG_ALS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_ALS = 0. Clear the EN_ALS_INT will also clear the FLG_ALS_INT bit to 0.

ALS persistence numbers PRST_ALS[1:0] is used to avoid the false alarm of ALS out-of-windows event due to environment noise. If ALS persistence is set larger than 1, then the ALS out-of-windows interrupt will not be issued until continuous persistence numbers of ADC conversion results outside the defined windows.

6.4 Proximity Operation

6.4.1 PS General Operation State

The related PS control bits are summarized below.

PS Control Bits

General Control	
EN_PS	Enable PS function

EN_WAIT_PSGS	Enable PS wait state
IT_PSGS[3:0]	PS integration time
PRST_PS[1:0]	PS persistence number
WAIT1_PSGS[7:0]	PS wait period 1
WAIT2_PS[6:0]	PS wait period 2
LED Control	
IRDR_LED[1:0]	Choose LED driving current
LED_DIV2	LED current control
Special Control	
EN_INTELLIGENT_PRST	Enable PS intelligent persistence
PS Interrupt Control	
EN_PS_INT	Enable PS function interrupt
PS_MODE	Choose PS interrupt mode or near-far flag polling mode.
THDH_PS[15:0]	PS near-far detect high threshold
THDL_PS[15:0]	PS near-far detect low threshold

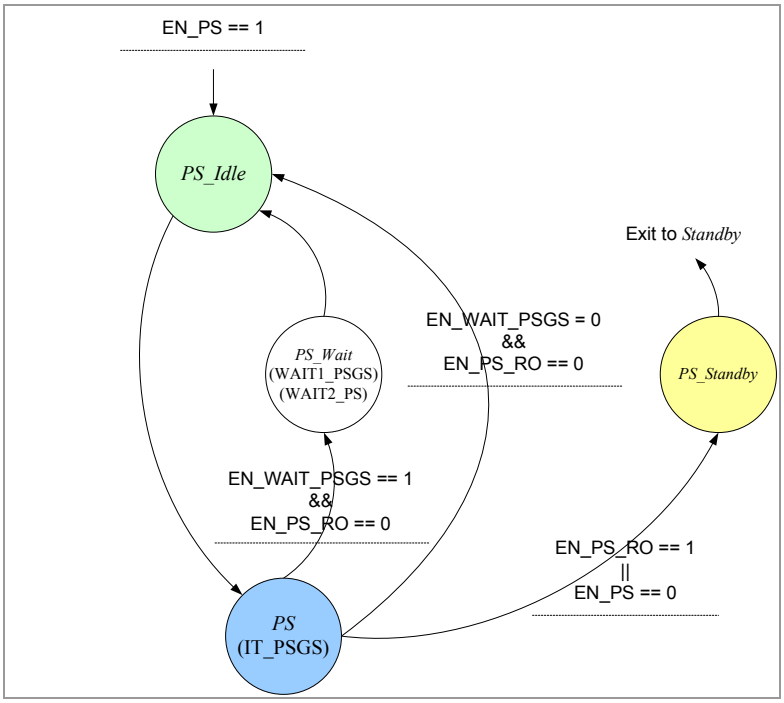
PS Data/Status Bits

Data	
DATA_PS[15:0]	16-bits PS raw data
Status	
FLG_NF	Indicate the current object near/far state
FLG_PS_INT	Indicate the object near/far state changed event
FLG_PS_DR	Indicate the PS data ready event

The STK3420 provides the proximity detection function which is done by emitting an IR signal and detect the reflected IR signal by the surface of the proximity object.

The PS and Gesture function share the same integration period(IT) control register, IT_PSGS[3:0]. Wait state can be turned on for saving operation power. The FLG_PSGS_DR bit shall be asserted every ADC conversion cycle complete and shall be cleared automatically after the DATA_PS[15:0] is be read out through I^2C.

IRDR_LED[1:0] and LED_DIV2 is used to choose different LED constant driving current. STK3420 has 3 different LED current levels 50/100/150mA.



6.4.2 PS Run-Once State

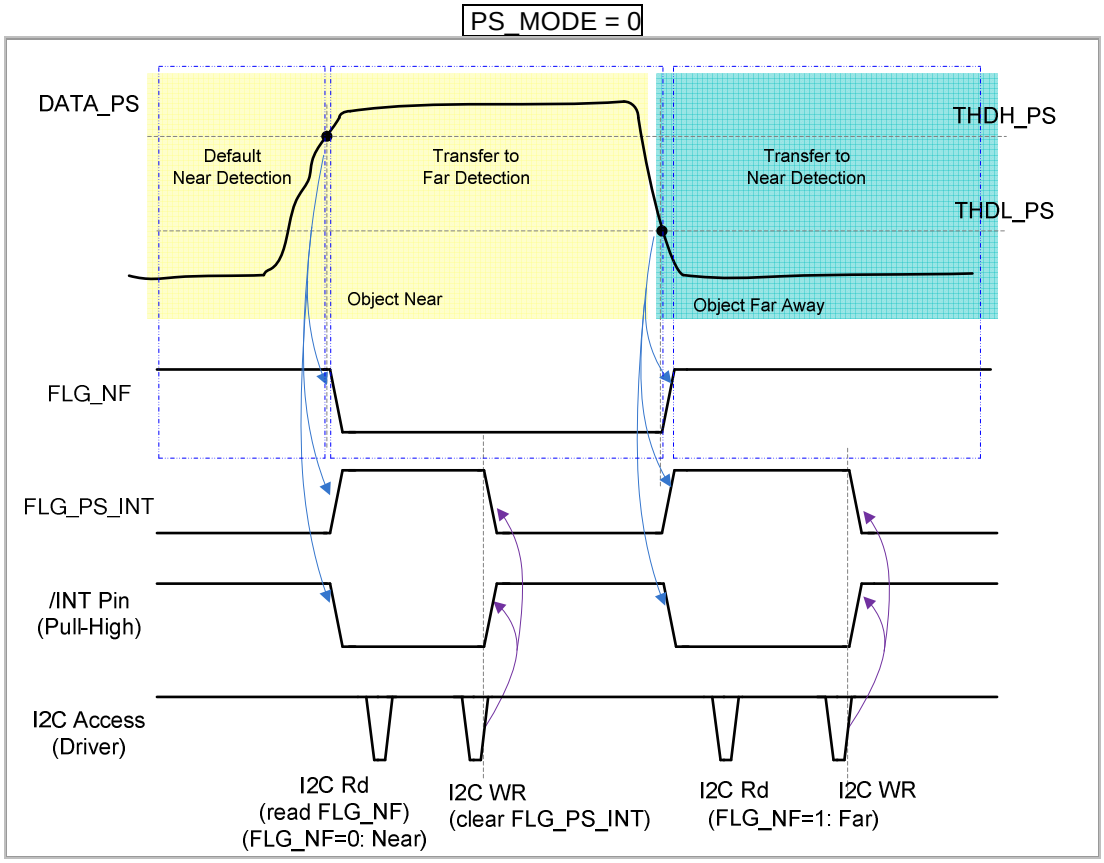
STK3420 provides the PS run-once function for saving the system power. The run-once function can only be effective when the PS function is turn on. The EN_PS_RO shall be set to 1 before EN_PS is set in order to enable the run-once function. Once the ALS run-once function is enabled, the STK3420 shall perform the whole PS operation state once, then stay in the *PS_Standby* state. Keep the EN_PS_RO = 1 and toggle the EN_PS bit from 0 to 1 will enable the run-once function again. The PS run-once function will not be effective if Gesture function is enabled.

6.4.3 PS Interrupt Description

If EN_PS_INT is set to 1, the PS_MODE signal is used to select how STK3420 report the object near/far state to application. PS_MODE is default 0 and the interrupt mode for near/far state change is used.

PS Near/Far Interrupt Mode (PS_MODE = 0)

The /INT pin is treated as interrupt signal. The FLG_NF is used to indicate whether the object is in near or far state. The STK3420 is default in object far state and the FLG_NF = 1. Once the object moving close to the STK3420 and PS code exceed the high threshold THDH_PS, STK3420 will switch to object near state and the FLG_NF is cleared to 0. If PS_MODE = 0 and EN_PS_INT = 1, STK3420 will issue a PS interrupt to inform the object near/far state changed and also set the FLG_PS_INT to 1. If the object move far away from the STK3420 and PS code lower than the low threshold THDL_PS, STK3420 will switch to object far state and the FLG_NF is set to 1. STK3420 will also issue a PS interrupt to inform and set FLG_PS_INT. The FLG_PS_INT shall be cleared by write the bit 0 and shall be reset to 0 if POR/SWRst or EN_PS = 0. The FLG_NF shall be reset to 1 if POR/SWRst or EN_PS = 0. Clear the EN_PS_INT will clear the FLG_PS_INT to 0, but keep the current PS code and FLG_NF state.

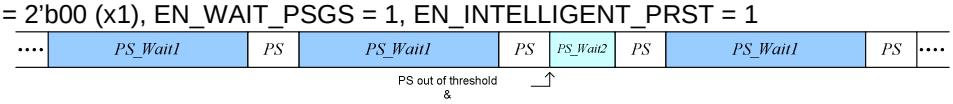


PS persistence numbers PRST_PS[1:0] is used to avoid the false alarm of PS interrupt event due to environment noise. If PS persistence is set larger than 1, then the PS interrupt will not be issued until continuous persistence numbers of ADC conversion results meet the interrupt condition describe above.

The STK3420 also provides intelligent persistence and can be enabled by set EN_INTELLIGENT_PRST to 1. Once the PS signal is exceed the high threshold when object in far state or lower than low threshold when in near state, EN_WAIT_PS = 1 and the PS persistence number PRST_PS[1:0] large than 1, the STK3420 will switch the wait time from a longer period WAIT1_PSGS[7:0] to a shorter one WAIT2_PS[6:0] in order to increase the PS response time and also avoid the flicker noise influence when choosing the appropriate wait2 period. The STK3420 shall switch back to the longer wait1 period no matter what PS persistence success or fail.

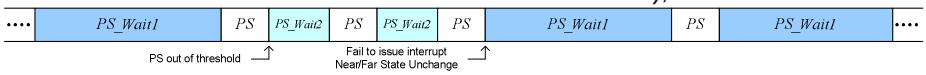
For example:

PRST_PS[1:0] = 2'b00 (x1), EN_WAIT_PSGS = 1, EN_INTELLIGENT_PRST = 1



PRST_PS[1:0] = 2'b10 (x4), EN_WAIT_PSGS = 1, , EN_INTELLIGENT_PRST = 1

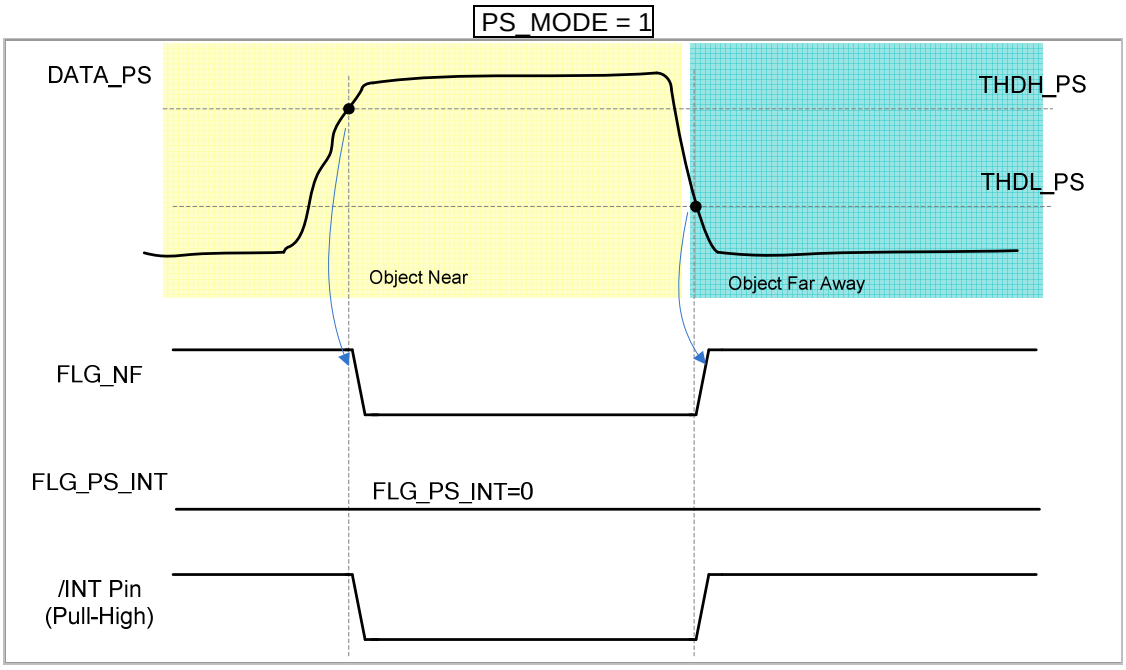
PRST_PS[1:0] = 2'b10 (x4), EN_WAIT_PSGS = 1, , EN_INTELLIGENT_PRST = 1 and fail to issue interrupt event (no continue persistence numbers of ADC conversion results out of threshold),



The intelligent persistence will not be effective if Gesture function is enabled. Only wait 1 period is used when gesture function enabled.

PS Near/Far Flag Mode (PS_MODE = 1)

If PS_MODE is set to 1, then the polling mode is used and the /INT pin is treated as a near/far flag signal, not an interrupt signal. In this mode, the /INT output level is same with the FLG_NF signal level and the FLG_PS_INT will never be asserted. The application simply polls the /INT level (high or low) to check the object in near or far state.



6.5 Gesture Operation

6.5.1 GS General Operation State

The related GS control bits are summarized below.

GS Control Bits

General Control	
EN_GSEW	Enable GS EW gesture function
EN_GSNS	Enable GS NS gesture function
EN_WAIT_PSGS	Enable GS wait state
IT_PSGS[3:0]	GS integration time
WAIT1_PSGS[7:0]	GS wait period
LED Control	
IRDR_LED[1:0]	Choose LED driving current
LED_DIV2	LED current control
GS FIFO Control	
EN_GS_INT	Enable GS FIFO interrupt
GS_FIFO_LEN[4:0]	Specify the GS unit-data length in FIFO
GS_FIFO_THD[3:0]	Specify the GS unit-data length threshold in FIFO

GS Data/Status Bits

Data	
DATA_GSE/W/N/S[15:0]	16-bits GSE/W/N/S raw data
Status	

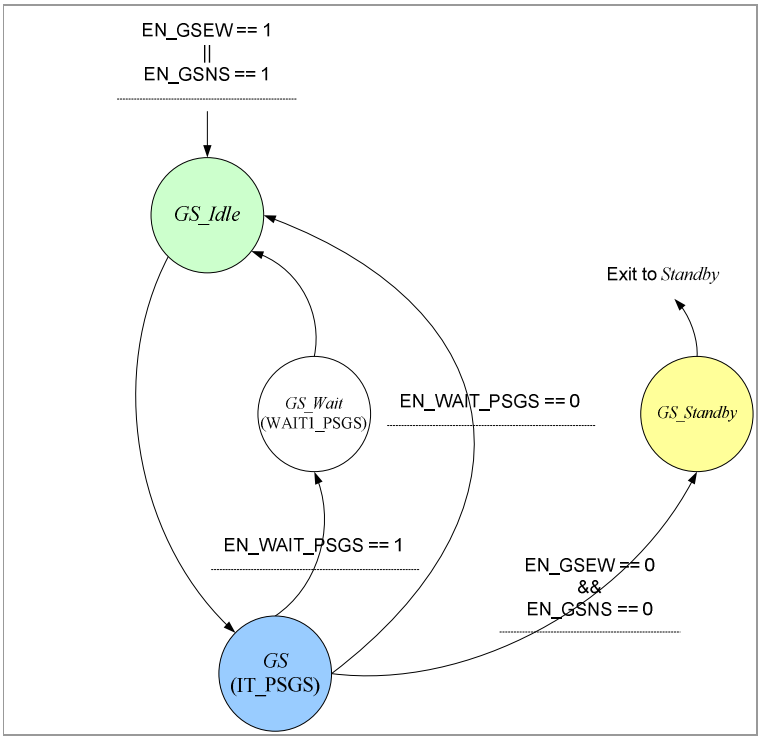
FLG_GS_INT	Indicate the GS FIFO with data
FLG_GS_FIFO_OV	Indicate the GS FIFO overflow

STK3420 provides 3D gesture detection, left/right/up/down/near/far. The near/far detection can be achieved by PS function. EN_GSEW enable the up/down gesture detection and EN_GSNS enable the left/right detection. The application can choose which direction they want to detect the gesture.

The Gesture data processing is different with PS function. All E/W/N/S PD outputs are used for gesture detection and the all the GS output are written into a 128 bytes FIFO. The application polls periodically or use interrupt to get the raw data from FIFO and perform the gesture algorithm in the system processor. The FIFO is designed for the application running in a lower speed system processor.

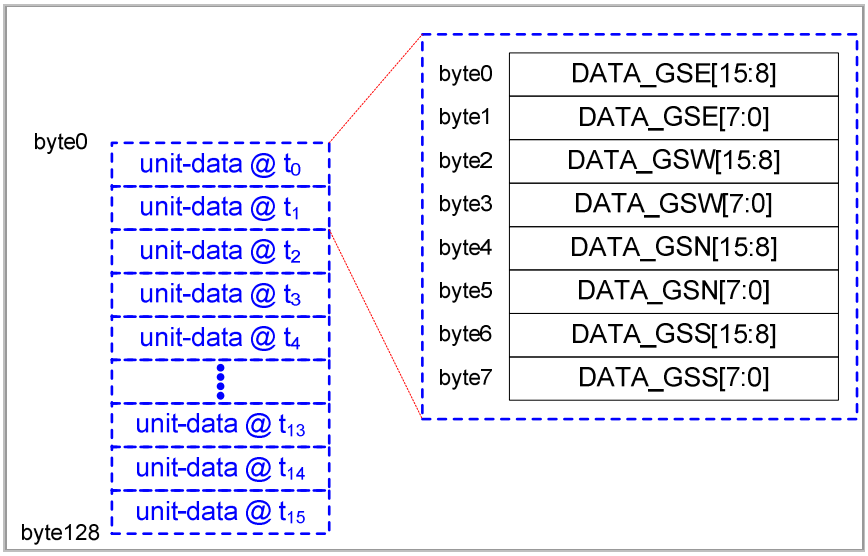
The PS and Gesture function share the same IT period control register, IT_PSGS[3:0]. Wait state (WAIT1_PSGS) can be turned on for saving operation power.

IRDR_LED[1:0] and LED_DIV2 is used to choose different LED constant driving current. STK3420 has 3 different LED current levels 50/100/150mA.



6.5.2 GS FIFO Operation

STK3420 has 128 bytes FIFO used to store 16 gesture unit-data. One gesture unit-data is composed by E/W/N/S word length output data in one ADC conversion cycle. The FIFO layout is shown below.



The GS_FIFO_LEN[4:0] is used to indicate the current unit-data numbers in the FIFO. Once the GS_FIFO_LEN is larger the GS_FIFO_THD and EN_GS_INT = 1, STK3420 will issue an interrupt to inform the application to get the gesture raw data and assert FLG_GS_INT bit. The FLG_GS_INT shall be cleared manually by writing this bit 0.

The FIFO data shall be accessed by DATA_GSE/W/N/S register. The 8 registers contain the oldest gesture unit-data that never being read in the FIFO. If only EN_GSEW is turned on, the next gesture unit-data shall not be uploaded into the DATA_GSE/W/N/S registers until the application readout the DATA_GSW[7:0]. If only EN_GSNS or both EN_GSEW/NS are turned on, the next gesture unit-data shall not be uploaded into the DATA_GSE/W/N/S registers until the application readout the DATA_GSS[7:0].

If FIFO overflow happens, STK3420 will assert the FLG_GS_FIFO_OV and keep the latest gesture unit-data and abandon the oldest one. The FLG_GS_FIFO_OV shall be cleared manually by writing this bit 0.

6.6.3 GS FIFO Access Interrupt Mode / Polling Mode

GS FIFO Access Interrupt Mode

STK3420 will issue GS interrupt and assert FLG_GS_INT to inform the application that there are gesture data in FIFO and the unit-data length exceed the GS_FIFO_THD. The application shall read the GS_FIFO_LEN unit-data through DATA_GSE/W/N/S registers, clear FLG_GS_INT and wait the next interrupt.

GS FIFO Access Polling Mode

The application shall poll GS_FIFO_LEN periodically. If GS_FIFO_LEN is larger than 0, then the application shall read the GS_FIFO_LEN unit-data through DATA_GSE/W/N/S registers and wait for the next polling period.

7. CONTROL REGISTER MAP

ADDR	REG NAME	BIT								Default
		7	6	5	4	3	2	1	0	
0x00	STATE	EN_IRS		EN_ALS_RO	EN_PS_RO	EN_WAIT_ALS	EN_WAIT_PSGS	EN_ALS	EN_PS	0x00
0x01	PS/GSCTRL1	PRST_PS[1:0]				IT_PSGS[3:0]				0x01
0x02	ALSCTRL1	PRST_ALS[1:0]		GAIN_ALS[1:0]		IT_ALS[3:0]				0x34
0x03	LEDCTRL	IRDR_LED[1:0]								0x40
0x04	INT	INT_CTRL			EN_GS_INT	EN_ALS_INT		PS_MODE	EN_PS_INT	0x00
0x05	WAIT1_PSGS	WAIT1_PSGS[7:0]								0x00
0x06	THDH1_PS	THDH_PS[15:8]								0xFF
0x07	THDH2_PS	THDH_PS[7:0]								0xFF
0x08	THDL1_PS	THDL_PS[15:8]								0x00
0x09	THDL2_PS	THDL_PS[7:0]								0x00
0x0A	THDH1_ALS	THDH_ALS[15:8]								0xFF
0x0B	THDH2_ALS	THDH_ALS[7:0]								0xFF
0x0C	THDL1_ALS	THDL_ ALS[15:8]								0x00
0x0D	THDL2_ALS	THDL_ ALS[7:0]								0x00
0x10	FLAG	FLG_ALS_DR	FLG_PS_DR	FLG_ALS_INT	FLG_PS_INT	FLG_GS_INT		FLG_IRS_DR	FLG_NF	0x01
0x11	DATA1_PS	DATA_PS[15:8]								
0x12	DATA2_PS	DATA_PS[7:0]								
0x13	DATA1_ALS	DATA_ALS[15:8]								
0x14	DATA2_ALS	DATA_ALS[7:0]								
0x17	DATA1_IRS	DATA_IRS[15:8]								
0x18	DATA2_IRS	DATA_ IRS[7:0]								
0x19	ALSCTRL2	ITER_IRS[1:0]		GAIN_IRS[1:0]		IT_IRS[3:0]				0x74
0x1B	WAIT_ALS	WAIT_ALS[7:0]								0x00
0x1C	WAIT2_PS		WAIT2_PS[6:0]							0x00
0x1D	PS/GSCTRL2		EN_INTELLIGENT_PRST					EN_GSNS	EN_GSEW	0xF0
0x1E	GSFLAG	FLG_GS_FIFO_OV			GS_FIFO_LEN[4:0]					
0x1F	GSFIFOCTRL					GS_FIFO_THD[3:0]				0x08
0x20	DATA1_GSE	DATA_GSE[15:8]								
0x21	DATA2_GSE	DATA_GSE[7:0]								
0x22	DATA1_GSW	DATA_GSW[15:8]								
0x23	DATA2_GSW	DATA_GSW[7:0]								
0x24	DATA1_GSN	DATA_GSN[15:8]								
0x25	DATA2_GSN	DATA_GSN[7:0]								
0x26	DATA1_GSS	DATA_GSS[15:8]								
0x27	DATA2_GSS	DATA_GSS[7:0]								
0x3E	PDT_ID	PDT_ID[7:0]								0x50
0x3F	Reserved	Reserved								
0x80	SOFT_RESET	Write any to soft reset								
0x94	MISC1						LED_DIV2			0xC3

STATE Register (0x00)

Bit	7	6	5	4	3	2	1	0
ITEM	EN_IRS		EN_ALS_RO	EN_PS_RO	EN_WAIT_ALS	EN_WAIT_PSGS	EN_ALS	EN_PS
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Default	0		0	0	0	0	0	0

Bit	ITEM	Description
0	EN_PS	Enable the PS function. 0: Disable 1: Enable
1	EN_ALS	Enable the ALS function. 0: Disable 1: Enable
2	EN_WAIT_PSGS	Enable the PS/GS wait state. 0: Disable 1: Enable
3	EN_WAIT_ALS	Enable the ALS wait state. 0: Disable 1: Enable
4	EN_PS_RO	Enable the PS run-once mode. 0: Disable 1: Enable
5	EN_ALS_RO	Enable the ALS run-once mode. 0: Disable 1: Enable
7	EN_IRS	Enable the ALS IR-Sensing mode. 0: Disable 1: Enable

PS/GSCTRL1 Register (0x01)

Bit	7	6	5	4	3	2	1	0
ITEM	PRST_PS[1:0]				IT_PSGS[3:0]			
Access	R/W				RW			
Default	2'b00				4'b0001			

Bit	ITEM	Description
3:0	IT_PSGS[3:0]	PS/GS refresh time. The refresh time of PS/GS can be tuned by IT_PSGS[3:0]. Through setting IT_PSGS[3:0], user could achieve very wide range flexibly in choosing refresh time for different application demand. 4'b0000 — 97 us 4'b0001 — 195 us 4'b0010 — 390 us 4'b0011 — 780 us 4'b0100 — 1.56 ms 4'b0101 — 3.12 ms 4'b0110 — 6.25 ms others — Reserved
5:4	Reserved	
7:6	PRST_PS[1:0]	PS persistence setting. The PS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-threshold PS occurrences before an interrupt is triggered.

2'b00	x 1 times		
2'b01	x 2 times		
2'b10	x 4 times		
2'b11	x 8 times		

ALSCTRL1 Register **(0x02)**

Bit	7	6	5	4	3	2	1	0
ITEM	PRST_ALS[1:0]		GAIN_ALS[1:0]		IT_ALS[3:0]			
Access	R/W		R/W		RW			
Default	2'b00		2'b11		4'b0100			

Bit	ITEM	Description
3:0	IT_ALS[3:0]	ALS refresh time. The refresh time of ALS can be tuned by IT_ALS[3:0]. Through setting IT_ALS[3:0], user could achieve very wide range flexibly in choosing refresh time for different application demand. 4'b0000 — 12.5 ms 4'b0001 — 25 ms 4'b0010 — 50 ms 4'b0011 — 100 ms others — Reserved
5:4	GAIN_ALS[1:0]	ALS gain setting. 2'b00 — x 1 2'b01 — x 2 2'b10 — x 4 2'b11 — Reserved
7:6	PRST_ALS[1:0]	ALS persistence setting. The ALS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-windows ALS occurrences before an interrupt is triggered. 2'b00 — x 1 times 2'b01 — x 2 times 2'b10 — x 4 times 2'b11 — x 8 times

LEDCTRL Register **(0x03)**

Bit	7	6	5	4	3	2	1	0
ITEM	IRDR_LED[1:0]							
Access	R/W							
Default	2'b01							

Bit	ITEM	Description
7:6	IRDR_LED[1:0]	LED constant current setting. The STK3420 provides different driving ability for IRLED through setting IRDR. 2'b00 — 50 mA current sink 2'b01 — 100 mA current sink 2'b10 — Reserved 2'b11 — 150 mA current sink and the LED_DIV2 bit should be set to 1.

INT Register **(0x04)**

Bit	7	6	5	4	3	2	1	0
ITEM	INT_CTRL			EN_GS_INT	EN_ALS_INT		PS_MODE	EN_PS_INT
Access	R/W			R/W	R/W		R/W	R/W
Default	0			0	0		0	0

Bit	ITEM	Description
0	EN_PS_INT	Enable the PS interrupt. 0: Disable 1: Enable
1	PS_MODE	Select the /INT pin type when EN_PS_INT = 1. 0: Normal interrupt mode, /INT is treated as interrupt signal. 1: Near/Far flag polling mode, /INT is treated as near/far flag signal and the pin level definition is same with FLG_NF bit.
3	EN_ALS_INT	Enable the ALS out-of-windows interrupt. 0: Disable 1: Enable
4	EN_GS_INT	Enable the GS interrupt. Once the number of GS unit-data stored in FIFO exceed the threshold and EN_GS_INT = 1, then STK3420 shall issue a interrupt to inform the application. 0: Disable 1: Enable
7	INT_CTRL	0: Set /INT pin low if FLG_ALS_INT or FLG_ALS_DR or FLG_PS_INT or FLG_PSGS_DR or FLG_GS_INT high (logical OR) 1: Set /INT pin low if FLG_ALS_INT and FLG_ALS_DR and FLG_PS_INT and FLG_PSGS_DR and FLG_GS_INT high (logical AND)

WAIT1_PSGS Register **(0x05)**

Bit	7	6	5	4	3	2	1	0
ITEM	WAIT1_PSGS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
7:0	WAIT1_PSGS[7:0]	PS/GS wait state period. wait period = (WAIT1_PSGS[7:0] + 1) * 780us

THDH1_PS Register **(0x06)**

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_PS[15:8]							
Access	R/W							
Default	8'b11111111							

THDH2_PS Register **(0x07)**

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_PS[7:0]							
Access	R/W							
Default	8'b11111111							

THDL1_PS Register (0x08)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_PS[15:8]							
Access	R/W							
Default	8'b00000000							

THDL2_PS Register (0x09)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_PS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
15:0	THDH_PS[15:0]	PS high threshold.
15:0	THDL_PS[15:0]	PS low threshold.

THDH1_ALS Register (0x0A)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[15:8]							
Access	R/W							
Default	8'b11111111							

THDH2_ALS Register (0x0B)

Bit	7	6	5	4	3	2	1	0
ITEM	THDH_ALS[7:0]							
Access	R/W							
Default	8'b11111111							

THDL1_ALS Register (0x0C)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[15:8]							
Access	R/W							
Default	8'b00000000							

THDL2_ALS Register (0x0D)

Bit	7	6	5	4	3	2	1	0
ITEM	THDL_ALS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
15:0	THDH_ALS[15:0]	ALS high threshold.
15:0	THDL_ALS[15:0]	ALS low threshold.

FLAG Register **(0x10)**

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_ALS_DR	FLG_PS_DR	FLG_ALS_INT	FLG_PS_INT	FLG_GS_INT		FLG_IRS_DR	FLG_NF
Access	R/W	R/W	R/W	R/W	R/W		RO	RO
Default	0	0	0	0	0		0	1

Bit	ITEM	Description
0	FLG_NF	Object near/far flag. Default FLG_NF = 1, object in far state. 0: Object in near state 1: Object in far state
1	FLG_IRS_DR	Indicate IRS conversion complete. The FLG_IRS_DR bit shall be asserted once the *IRS* state complete and shall be cleared automatically after the DATA_IRS[15:0] is be read out through I^2C. 0: Not yet complete and data in DATA_IRS is not valid 1: IRS complete and data in DATA_IRS is valid
3	FLG_GS_INT	Indicate if interrupt event is related to GS_INT. Write bit 0 to clear. 0: No GS_INT event 1: GS_INT event
4	FLG_PS_INT	Indicate if interrupt event is related to PS_INT. Write bit 0 to clear. 0: No PS_INT event 1: PS_INT event
5	FLG_ALS_INT	Indicate if interrupt event is related to ALS_INT. Write bit 0 to clear. 0: No ALS_INT event 1: ALS_INT event
6	FLG_PS_DR	Indicate PS data conversion complete. Automatically cleared after DATA_PS[15:0] is read. 0: PS data is not ready 1: PS data is ready
7	FLG_ALS_DR	Indicate ALS data conversion complete. Automatically cleared after DATA_ALS[15:0] is read. 0: ALS data is not ready 1: ALS data is ready

DATA1_PS Register **(0x11)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS[15:8]							
Access	RO							
Default								

DATA2_PS Register **(0x12)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_PS[7:0]							
Access	RO							
Default								

The STK3420 has two 8-bit read-only registers to hold the data from ADC of PS. The most significant bit (MSB) is accessed at register 0x11, and the least significant bit (LSB) is accessed at register 0x12. For 16-bit resolution, the data is from DATA_PS[15:0]. The registers are updated for every PS refresh time (conversion cycle).

DATA1_ALS Register **(0x13)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS[15:8]							
Access	RO							
Default								

DATA2_ALS Register **(0x14)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_ALS[7:0]							
Access	RO							
Default								

The STK3420 has two 8-bit read-only registers to hold the data from ADC of ALS. The most significant bit (MSB) is accessed at register 0x13, and the least significant bit (LSB) is accessed at register 0x14. For 16-bit resolution, the data is from DATA_ALS[15:0]. The registers are updated for every ALS refresh time (conversion cycle).

DATA1_IRS Register **(0x17)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_IRS[15:8]							
Access	RO							
Default								

DATA2_IRS Register **(0x18)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_IRS[7:0]							
Access	RO							
Default								

The STK3420 has two 8-bit read-only registers to hold the data from ADC of IRS. The most significant bit (MSB) is accessed at register 0x17, and the least significant bit (LSB) is accessed at register 0x18. For 16-bit resolution, the data is from DATA_IRS[15:0]. The registers are updated for every IRS refresh time (conversion cycle).

ALSCTRL2 Register **(0x19)**

Bit	7	6	5	4	3	2	1	0
ITEM	ITER_IRS[1:0]		GAIN_IRS[1:0]		IT_IRS[3:0]			
Access	R/W		R/W		RW			
Default	2'b01		2'b11		4'b0100			

Bit	ITEM	Description
3:0	IT_IRS[3:0]	IRS refresh time. The refresh time of IRS can be tuned by IT_IRS[3:0]. Through setting IT_IRS[3:0], user could achieve very wide range flexibly in choosing refresh time for different application demand.

4'b0000	6.25 ms
4'b0001	12.5 ms
4'b0010	25 ms
4'b0011	50 ms
4'b0100	100 ms
4'b0101	200 ms

		4'b0110	400 ms
		others	Reserved
5:4	GAIN_IRS[1:0]	IRS gain setting.	
		2'b00	x 1
		2'b01	x 2
		2'b10	x 4
		2'b11	x 8
7:6	ITER_IRS[1:0]	IRS iteration numbers. The ITER_IRS is used to reduce the overhead of IRS signal acquisition in the whole ALS operation.	
		2'b00	x 4 times
		2'b01	x 8 times
		2'b10	x 16 times
		2'b11	x 32 times

WAIT_ALS Register **(0x1B)**

Bit	7	6	5	4	3	2	1	0
ITEM	WAIT_ALS[7:0]							
Access	R/W							
Default	8'b00000000							

Bit	ITEM	Description
7:0	WAIT_ALS[7:0]	ALSS wait state period. wait period = (WAIT_ALS[7:0] + 1) * 5.7ms

WAIT2_PS Register **(0x1C)**

Bit	7	6	5	4	3	2	1	0
ITEM		WAIT2_PS[6:0]						
Access	R/W							
Default	7'b0000000							

Bit	ITEM	Description
6:0	WAIT2_PS[6:0]	PS wait state period for intelligent persistence. wait period = (WAIT2_PS[6:0] + 1) * 195us

PS/GSCTRL2 Register **(0x1D)**

Bit	7	6	5	4	3	2	1	0
ITEM		EN_INTELLIGENT_PRST					EN_GSNS	EN_GSEW
Access		R/W					R/W	R/W
Default		1					0	0

Bit	ITEM	Description
0	EN_GSEW	Enable the EW direction gesture detection. 0: Disable 1: Enable
1	EN_GSNS	Enable the NS direction gesture detection. 0: Disable 1: Enable
6	EN_INTELLIGENT_PRST	Enable the PS intelligent persistence. The PS will always use WAIT1 period if EN_INTELLIGENT_PRST = 0.

		0: Disable 1: Enable

GSFLAG Register **(0x1E)**

Bit	7	6	5	4	3	2	1	0
ITEM	FLG_GS_FIFO_OV			GS_FIFO_LEN[4:0]				
Access	R/W			RO				
Default	0							

Bit	ITEM	Description
4:0	GS_FIFO_LEN[4:0]	Indicate the unit-data length in current GS FIFO. Each unit-data is 8 byte long. Number 0~16 is valid.
7	FLG_GS_FIFO_OV	Indicate if GS FIFO overflow. Write bit 0 to clear. 0: No FIFO overflow 1: FIFO overflow

GSFIFOCTRL Register **(0x1F)**

Bit	7	6	5	4	3	2	1	0
ITEM					GS_FIFO_THD[3:0]			
Access					R/W			
Default					4'b1000			

Bit	ITEM	Description
3:0	GS_FIFO_THD[3:0]	Gesture FIFO unit-data number threshold. FIFO threshold = GS_FIFO_THD[3:0]

DATA1_GSE Register **(0x20)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSE[15:8]							
Access	RO							
Default								

DATA2_GSE Register **(0x21)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSE[7:0]							
Access	RO							
Default								

DATA1_GSW Register **(0x22)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSW[15:8]							
Access	RO							
Default								

DATA2_GSW Register **(0x23)**

Bit	7	6	5	4	3	2	1	0

ITEM	DATA_GSW[7:0]
Access	RO
Default	

DATA1_GSN Register **(0x24)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSN[15:8]							
Access	RO							
Default								

DATA2_GSN Register **(0x25)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSN[7:0]							
Access	RO							
Default								

DATA1_GSS Register **(0x26)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSS[15:8]							
Access	RO							
Default								

DATA2_GSS Register **(0x27)**

Bit	7	6	5	4	3	2	1	0
ITEM	DATA_GSE[7:0]							
Access	RO							
Default								

GS FIFO data access registers.

Product ID **(0x3E)**

Read Only; PDT_ID = Product ID to indicate the product information.

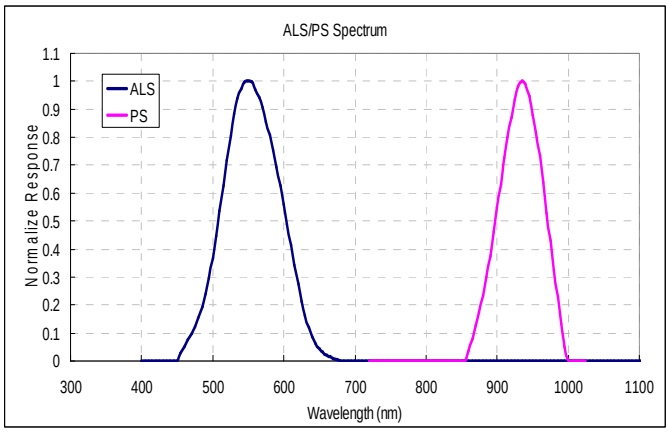
Reserved **(0x3F)**

Read Only; RSRVD = Reserved for engineering mode.

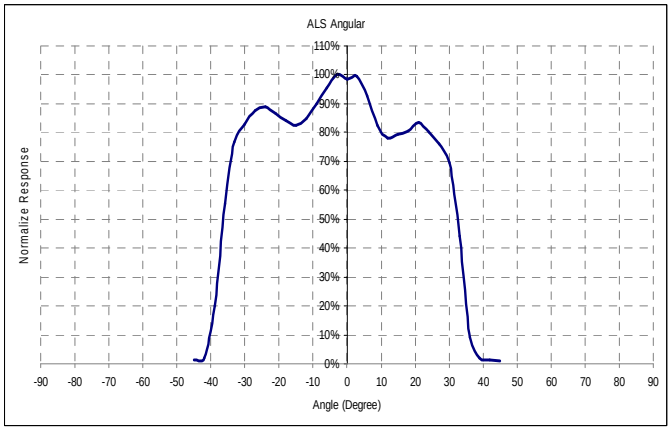
Soft reset **(0x80)**

Write any data to this register will reset the chip.

8. TYPICAL PERFORMANCE CHARACTERISTICS

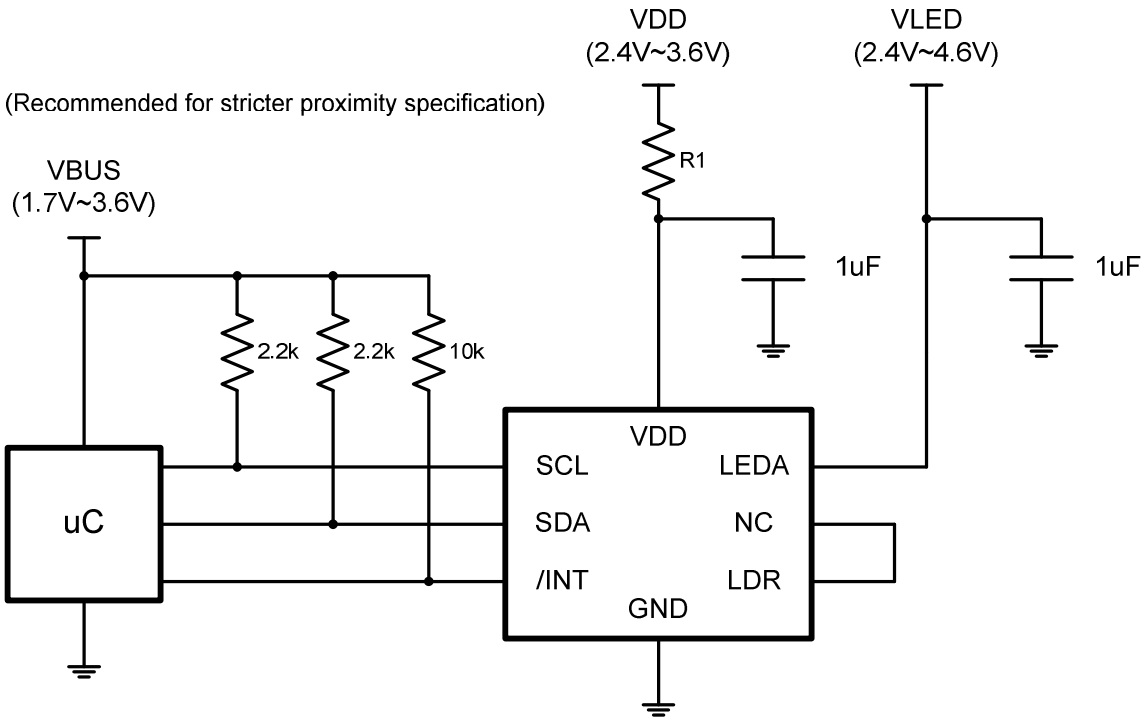


ALS& PS Spectral Response

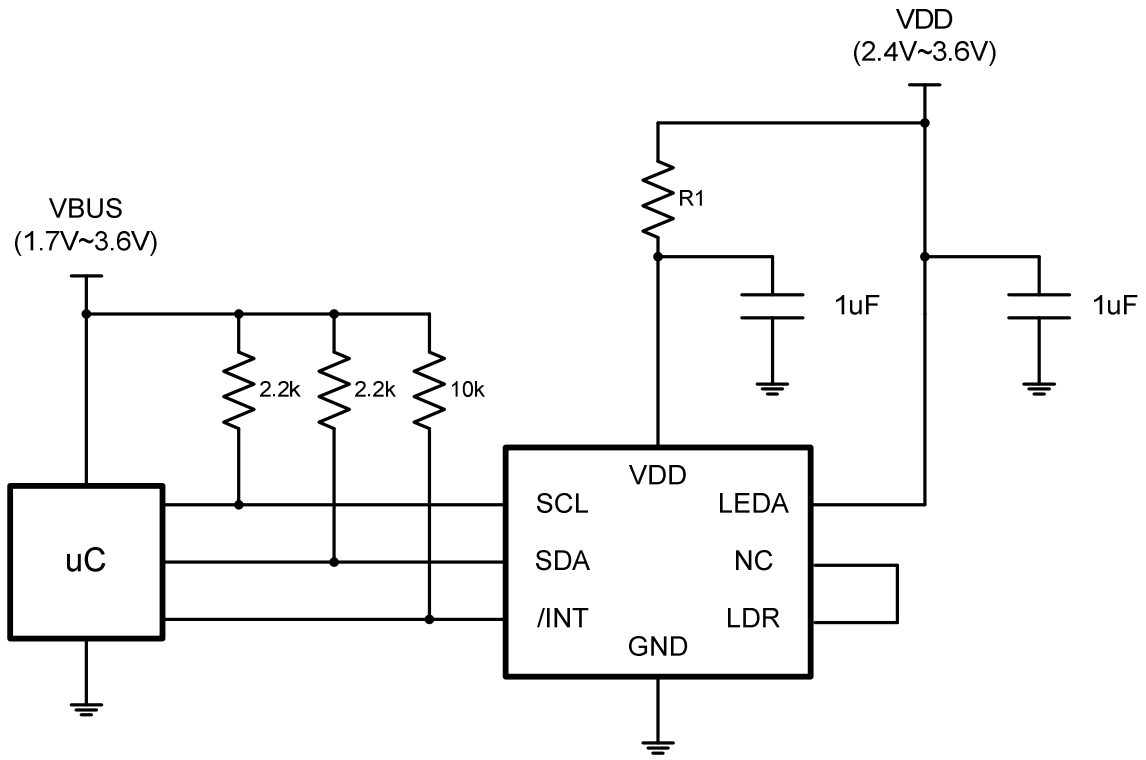


ALS View Angle

9. APPLICATION INFORMATION



STK3420 Typical Application Circuit with Independent VDD and VLED Supply Voltage



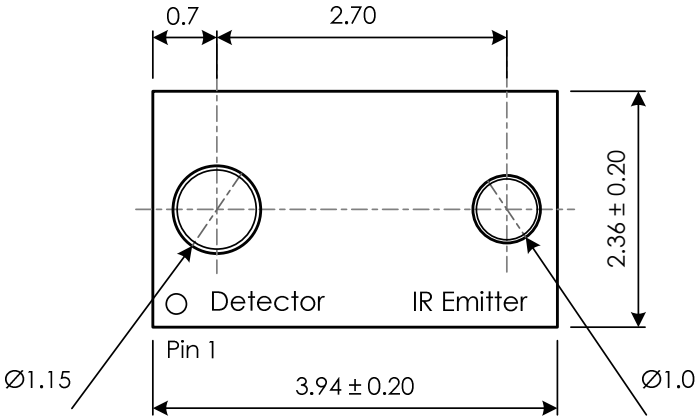
STK3420 Typical Application Circuit with Only One Supply Voltage

9.1 Power Noise Consideration

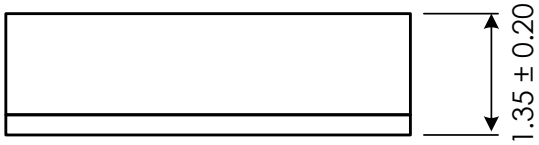
In order to reduce the switching noise come from the VLED, it is suggested that IC power and VLED comes from individual source to get the best performance of STK3420. The R1 series in the VDD path is strongly recommended that used to filter out the poor system power noise and the recommended value is 22 Ohm.

10. PACKAGE OUTLINE

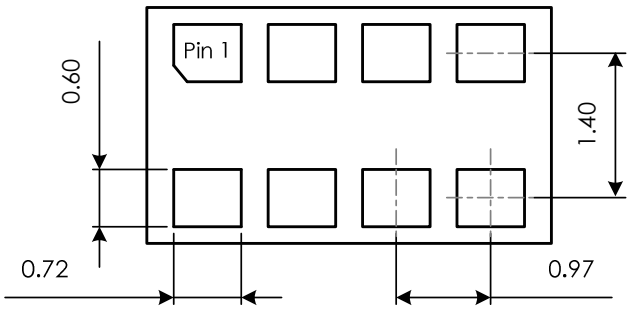
Top View



Side View



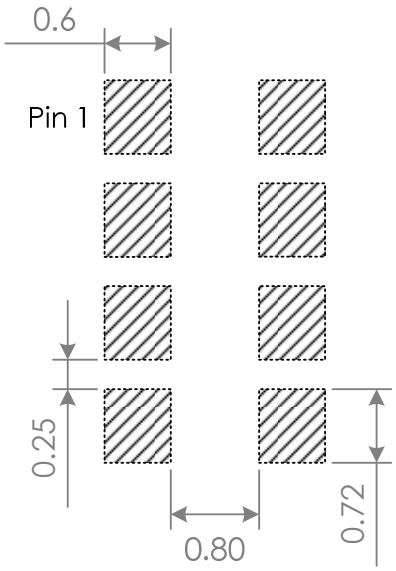
Bottom View



Dimension in Millimeters (mm)

PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown below.

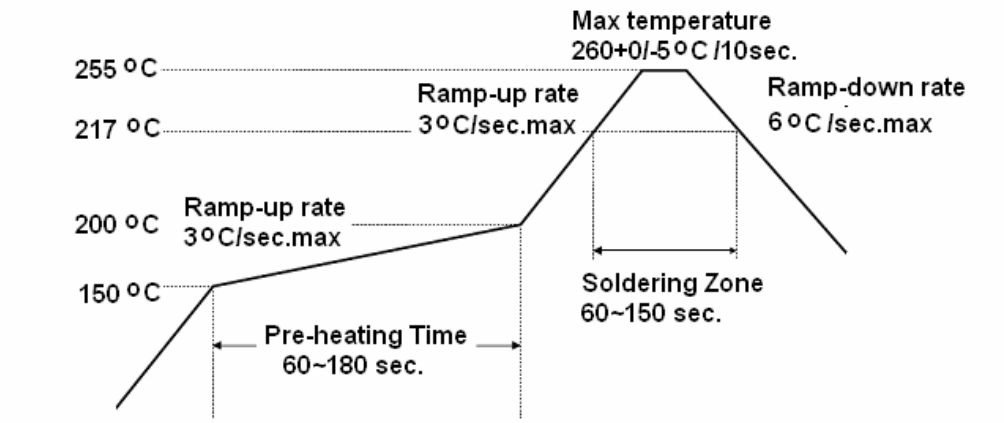


Notes: all linear dimensions are in mm.

11. SOLDERING INFORMATION

11.1 Soldering Condition

1. Pb-free solder temperature profile



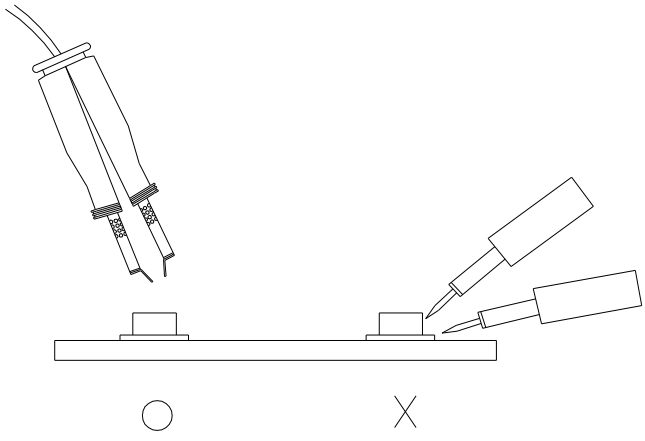
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350℃ for 3 seconds within o nce in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

Revision History

Date	Version	Modified Items
2015/02/01	1.0	Initial release.

