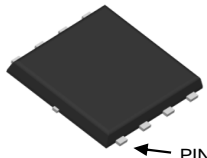
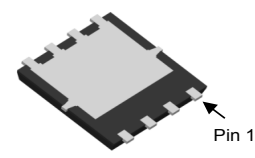
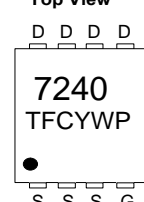
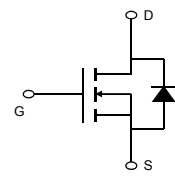


<p>40V N-Channel MOSFET</p> <p>PRODUCT SUMMARY</p> <p>V_{DS} 40V I_D (at $V_{GS}=10V$) 40A $R_{DS(ON)}$ (at $V_{GS}=10V$) < 5.5mΩ $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 7mΩ</p> <p>100% UIS Tested 100% R_g Tested</p> <ul style="list-style-type: none"> • Trench Power MOS Technology • Low $R_{DS(ON)}$ • Low Gate Charge • High Current Capability • RoHS and Halogen-Free Compliant <p>Applications</p> <ul style="list-style-type: none"> • DC/DC Converters in Computing • Isolated DC/DC Converters in Telecom and Industrial 	<p>PDFN5X6-8L</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Top View</p>  <p>PIN1</p> </div> <div style="text-align: center;"> <p>Bottom View</p>  <p>Pin 1</p> </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 20px;"> <div style="text-align: center;"> <p>Top View</p>  <p>D D D D 7240 TFCYWP S S S G</p> </div> <div style="text-align: center;"> <p>Equivalent Circuit</p>  </div> </div> <p>Y :year code W :week code</p>
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Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	I_D	40	A
		I_{DM}	144	
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_{DSM}	19	A
Avalanche Current ^C		I_{AS}, I_{AR}	40	A
Avalanche energy $L=0.1\text{mH}$ ^C		E_{AS}, E_{AR}	80	mJ
Power Dissipation ^B	$T_C=25^\circ\text{C}$	P_D	36.7	W
Power Dissipation ^A	$T_A=25^\circ\text{C}$	P_{DSM}	3.1	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	30	40	$^\circ\text{C/W}$
	Steady-State		60	75	
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.8	3.4	$^\circ\text{C/W}$



SHENZHEN TUOFENG SEMICONDUCTOR TECHNOLOGY CO.,LTD
N-Channel Enhancement Mode Power MOSFET

7240

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.9	2.4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	144			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A		4.2	5.5	mΩ
		V _{GS} =4.5V, I _D =15A		5.6	7	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		67		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				40	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz	1460	1830	2200	pF
C _{oss}	Output Capacitance		365	521	680	pF
C _{rss}	Reverse Transfer Capacitance		20	43	73	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	22	27.8	35	nC
Q _{g(4.5V)}	Total Gate Charge		10	12.8	15	nC
Q _{gs}	Gate Source Charge		3	3.9	5	nC
Q _{gd}	Gate Drain Charge		2	6	10	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1Ω, R _{GEN} =3Ω		7.2		ns
t _r	Turn-On Rise Time			3		ns
t _{D(off)}	Turn-Off DelayTime			23		ns
t _f	Turn-Off Fall Time			3.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	11	16.5	21	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	28	40	52	nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
- B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating g.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

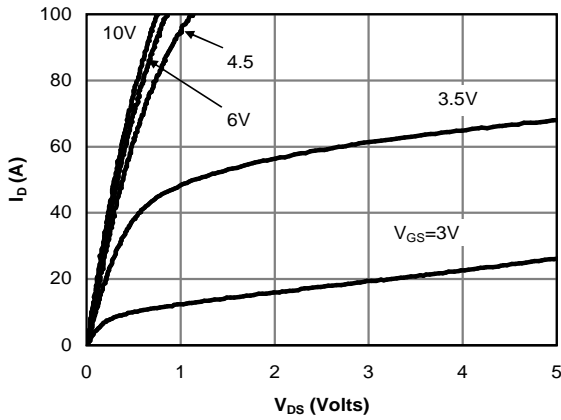


Fig 1: On-Region Characteristics (Note E)

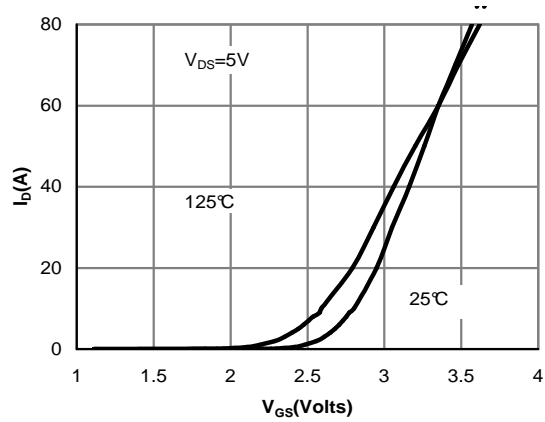


Figure 2: Transfer Characteristics (Note E)

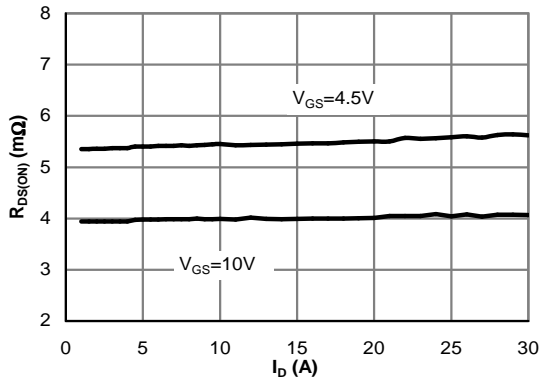


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

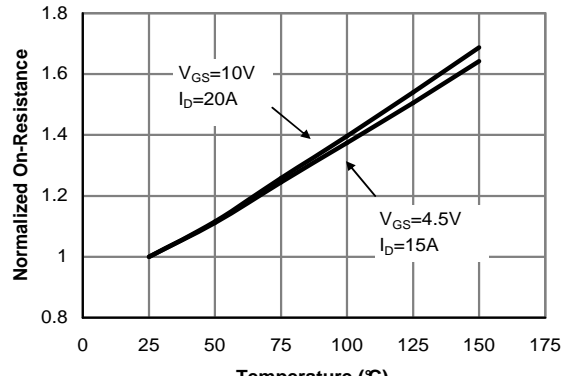


Figure 4: On-Resistance vs. Junction Temperature (Note E)

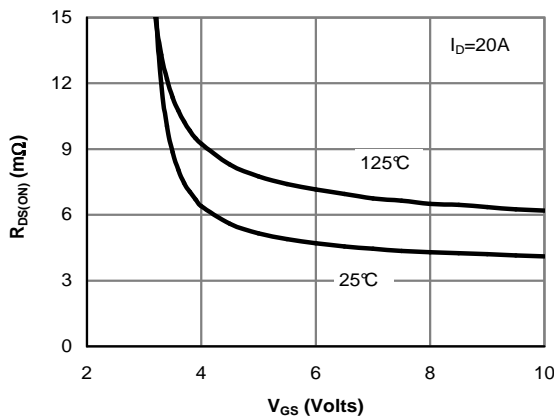


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

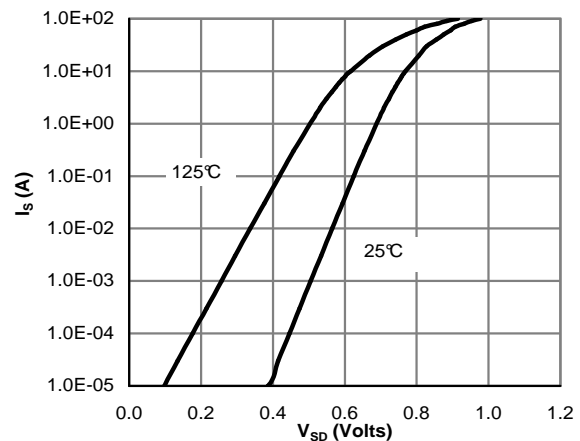


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

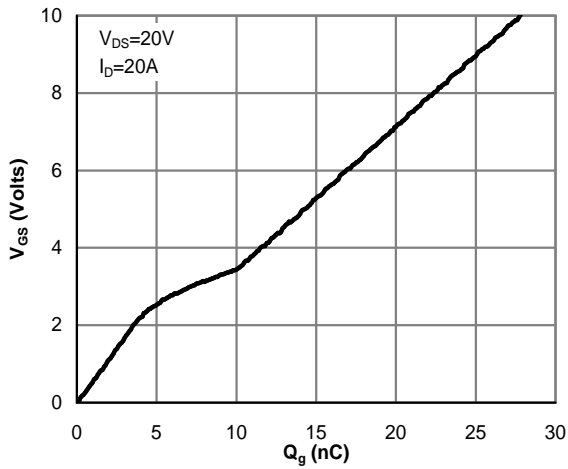


Figure 7: Gate-Charge Characteristics

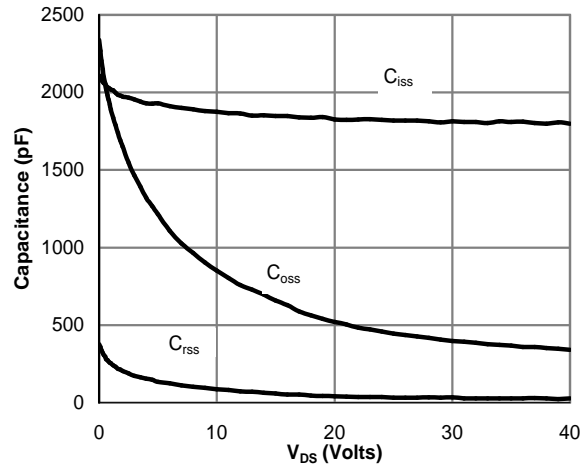


Figure 8: Capacitance Characteristics

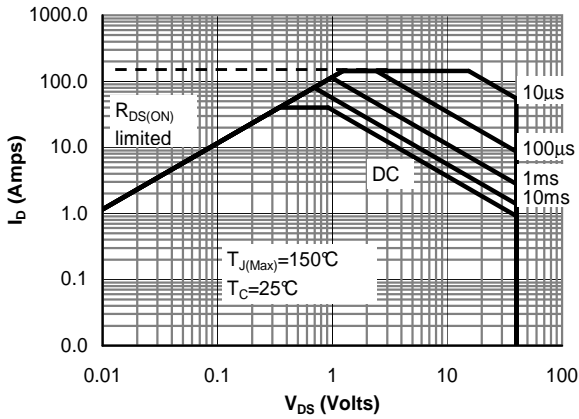


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

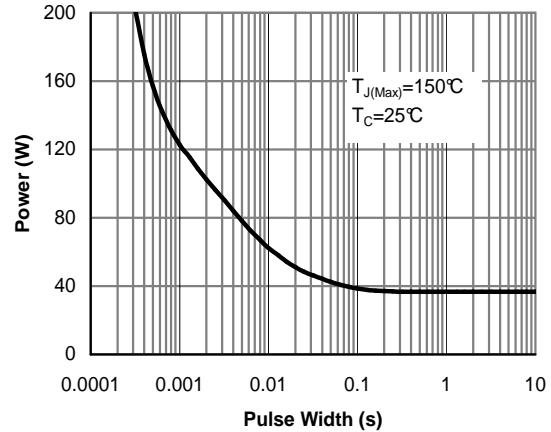


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

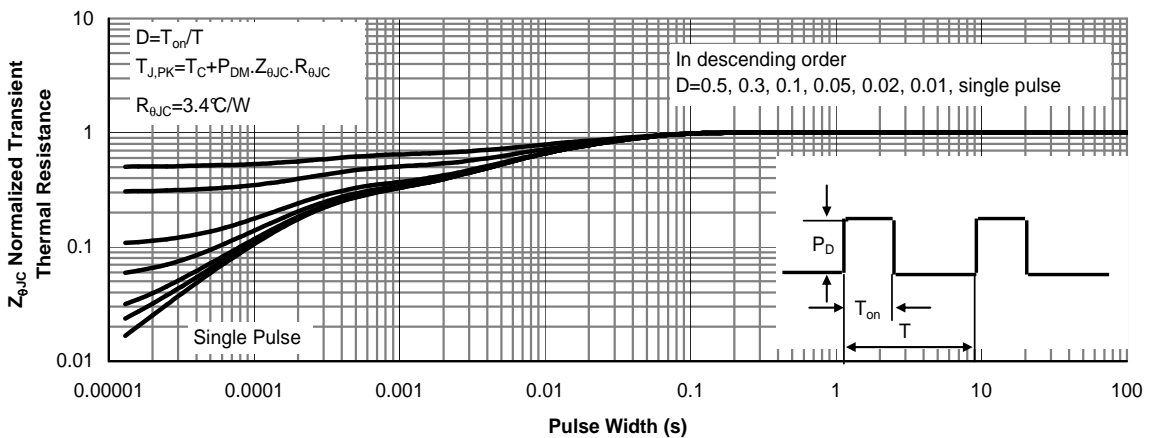


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

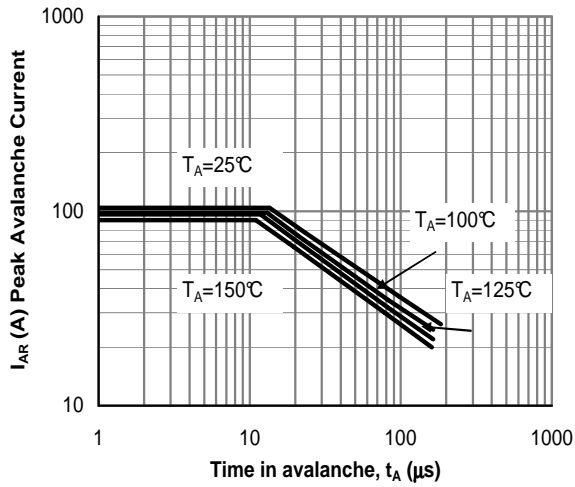


Figure 12: Single Pulse Avalanche capability (Note C)

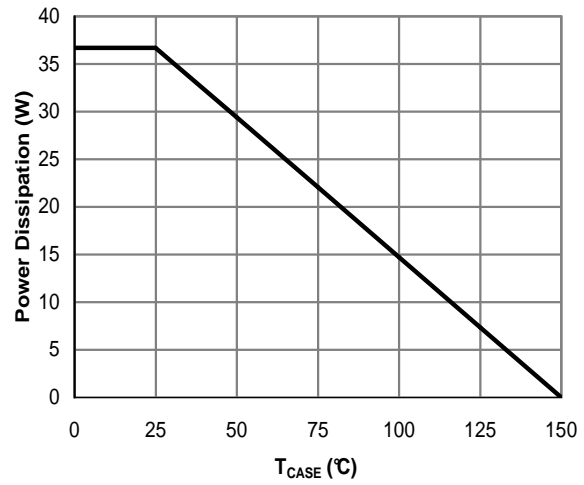


Figure 13: Power De-rating (Note F)

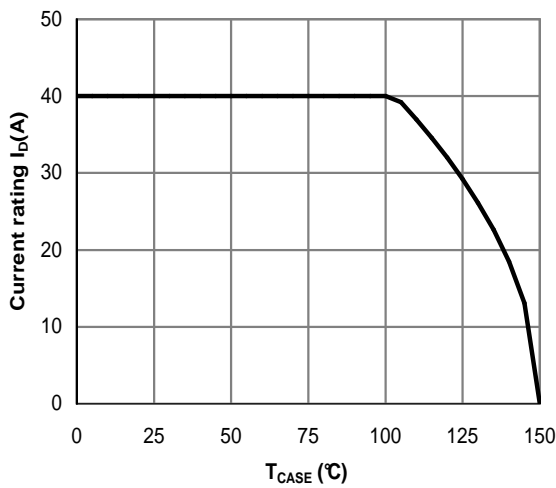


Figure 14: Current De-rating (Note F)

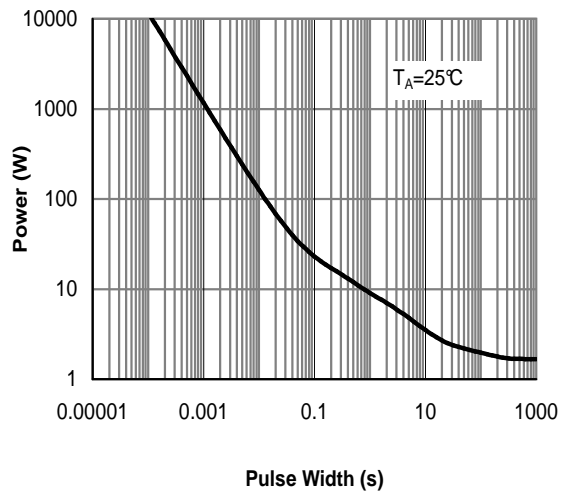


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

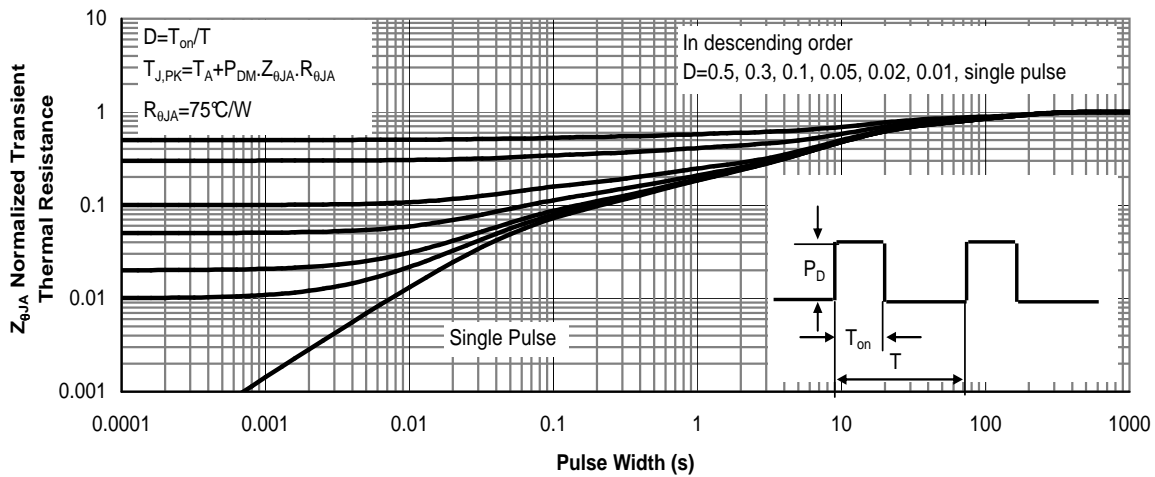
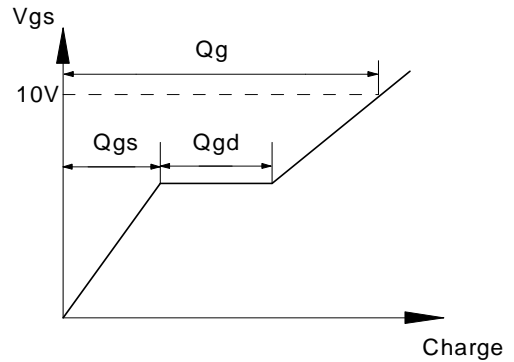
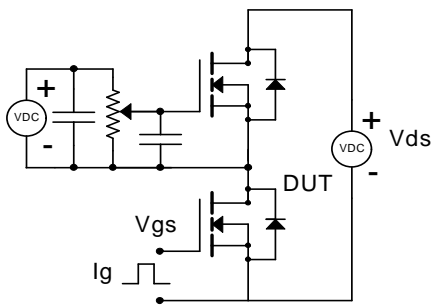
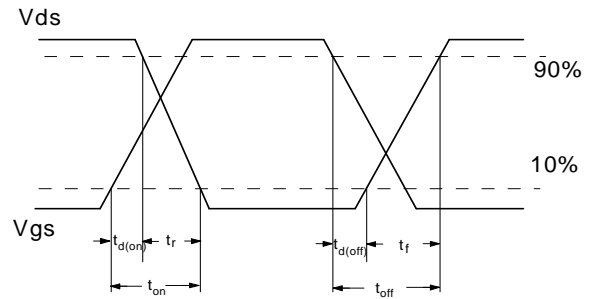
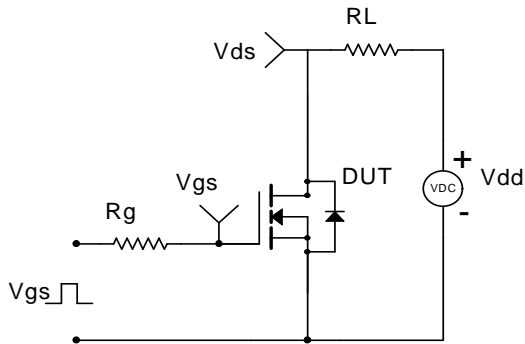


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

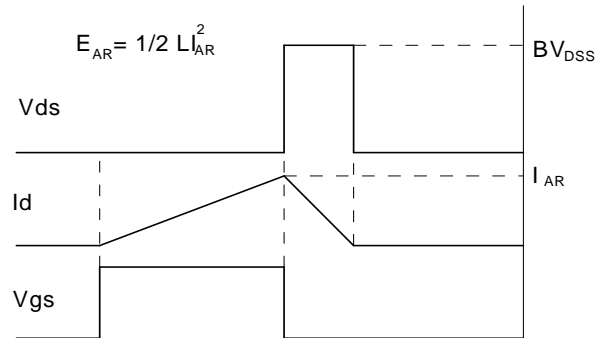
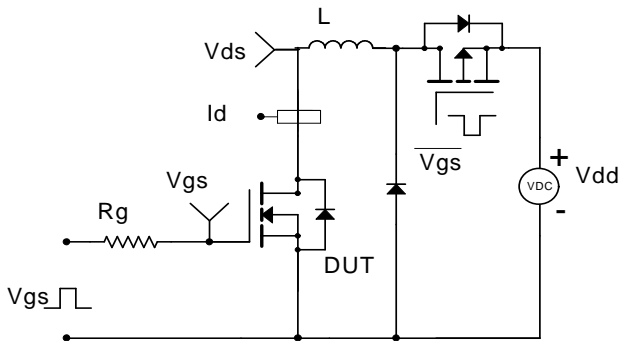
Gate Charge Test Circuit & Waveform



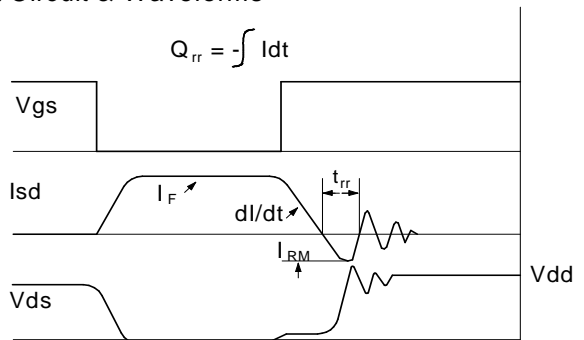
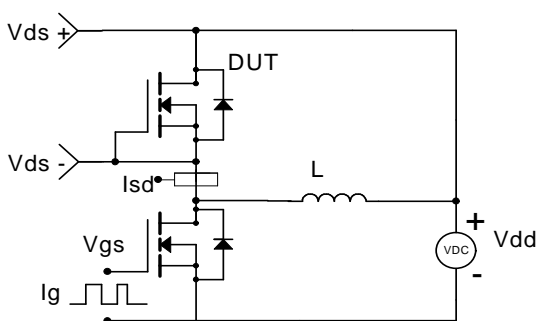
Resistive Switching Test Circuit & Waveforms



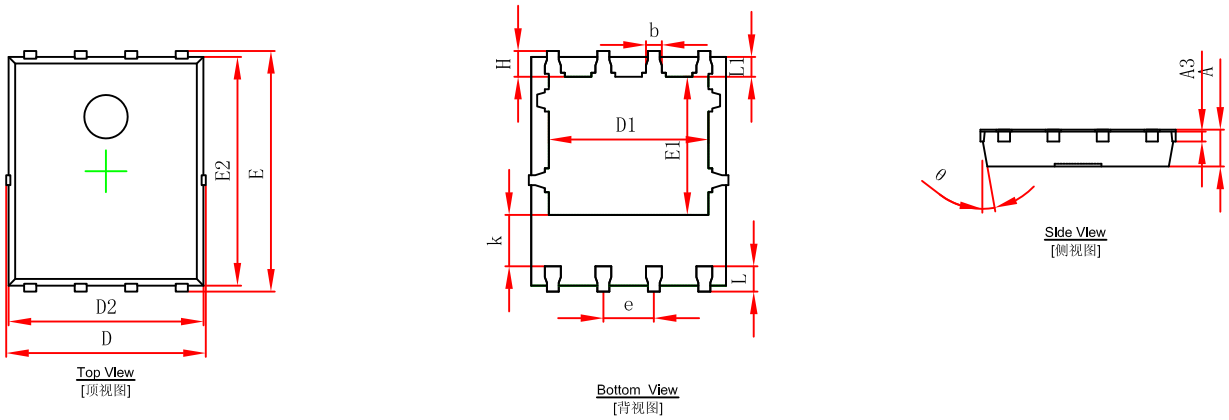
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

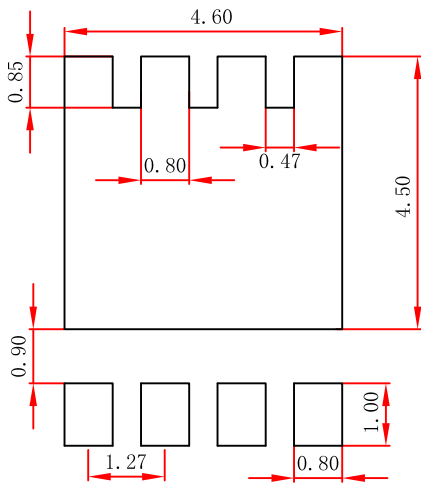


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.