

FEATURES

High performance

- High relative accuracy (INL): ± 4 LSB maximum at 16 bits
- TUE: $\pm 0.14\%$ of FSR maximum
- Offset error: ± 1.5 mV maximum
- Gain error: $\pm 0.06\%$ of FSR maximum
- Low drift 2.5 V voltage reference temperature coefficient: 2 ppm/°C typical

40 mA short-circuit current

Wide operating ranges

- -40°C to $+125^{\circ}\text{C}$ temperature range
- 2.7 V to 5.5 V power supply range

Simplified implementation

- User selectable gain of 1 or 2 (GAIN pin)
- 1.8 V logic compatibility

50 MHz SPI with readback or daisy chain

28-lead, 4 mm \times 4 mm, RoHS compliant LFCSP

APPLICATIONS

Optical transceivers

Base station power amplifiers

Process control (programmable logic controller (PLC)

input/output cards)

Industrial automation

Data acquisition systems

Table 1. Octal and 16-Channel *nanoDAC+*® Devices

No. of Channels	Interface	Reference	16-Bit	12-Bit
8	SPI ¹	Internal	AD5676R	AD5672R
		External	AD5676	Not applicable
8	I ² C	Internal	AD5675R	AD5671R
16	SPI	Internal	AD5679R	

¹ SPI = serial peripheral interface.

PRODUCT HIGHLIGHTS

- High channel density
16 channels in 4 mm \times 4 mm LFCSP
- High relative accuracy (integral nonlinearity (INL))
 ± 4 LSB maximum
- Low drift, 2.5 V, on-chip reference

FUNCTIONAL BLOCK DIAGRAM

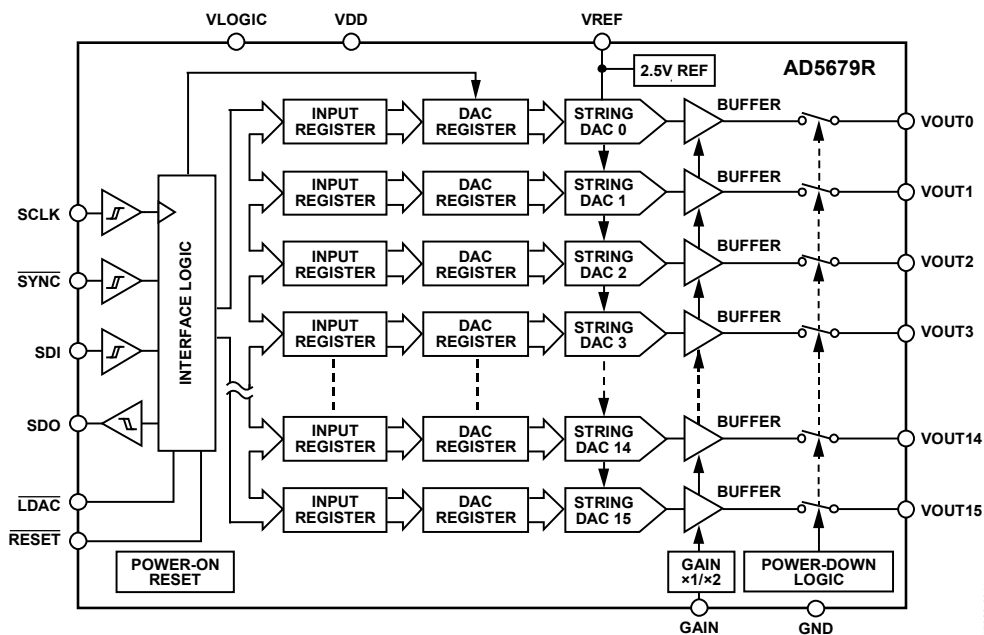


Figure 1.

Rev. 0

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REVISION HISTORY

8/2019—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5679R is a low power, 16-channel, 16-bit, buffered voltage output, digital-to-analog converter (DAC) that includes a 2.5 V, 2 ppm/°C internal reference (enabled by default), and a gain select pin, resulting in a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single, 2.7 V to 5.5 V supply range and is guaranteed monotonic by design. The

AD5679R is available in a 28-lead lead frame chip scale package (LFCSP) and incorporates a power-on reset (POR) circuit that ensures that the DAC outputs power up to and remains at zero-scale until a valid write. The AD5679R contains a power-down mode that reduces the current consumption to 2 μ A typical when in power-down mode.

SPECIFICATIONS

V_{DD} pin voltage (V_{DD}) = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} pin voltage (V_{LOGIC}) ≤ 5.5 V, load resistance (R_L) = 2 kΩ, load capacitance (C_L) = 200 pF, all specifications are T_J = −40°C to +125°C, typical at T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE¹					
Resolution	16			Bits	
INL		±1.8	±4	LSB	Gain = 1
		±1.7	±4	LSB	Gain = 2
Differential Nonlinearity (DNL)		±0.7	±1	LSB	Gain = 1
		±0.5	±1	LSB	Gain = 2
Zero Code Error		0.8	1.6	mV	Gain = 1 or gain = 2
Offset Error		−0.75	±2	mV	Gain = 1
		−0.1	±1.5	mV	Gain = 2
Full-Scale Error		−0.018	±0.14	% of FSR	Gain = 1
		−0.013	±0.07	% of FSR	Gain = 2, V _{DD} = 5.5 V
Gain Error		+0.04	±0.12	% of FSR	Gain = 1
		−0.02	±0.06	% of FSR	Gain = 2
Total Unadjusted Error (TUE)		±0.03	±0.18	% of FSR	Gain = 1
		±0.006	±0.14	% of FSR	Gain = 2
Offset Error Drift		±2		μV/°C	Gain = 1
DC Power Supply Rejection Ratio (PSRR)		0.25		mV/V	DAC code = midscale, V _{DD} = 5 V ± 10%
DC Crosstalk		±2		μV	Due to single channel, full-scale output change, internal reference, gain = 1
		±3		μV/mA	Due to load current change, external reference, gain = 2
		±2		μV	Due to powering down (per channel), internal reference, gain = 1
OUTPUT CHARACTERISTICS					
Output Power-Up Voltage		0		V	Gain = 1, AD5679R-1
		0		V	Gain = 2, AD5679R-1
Output Voltage Range	0		2.5	V	Gain = 1
	0		5	V	Gain = 2
Capacitive Load Stability		2		nF	R _L = ∞
		10		nF	R _L = 1 kΩ
Load Regulation		183		μV/mA	V _{DD} = 5 V ± 10%, DAC code = midscale, −30 mA ≤ output current (I _{OUT}) ≤ +30 mA
		177		μV/mA	V _{DD} = 3 V ± 10%, DAC code = midscale, −20 mA ≤ I _{OUT} ≤ +20 mA
Short-Circuit Current ²		40		mA	
Load Impedance at Rails ³		25		Ω	
Power-Up Time ⁴		3		μs	Exiting power-down mode, V _{DD} = 5 V
REFERENCE INPUT					
Reference Input Current		0.8		mA	Reference voltage (V _{REF}) = V _{DD} = V _{LOGIC} = 5.5 V, gain = 1
		1.6		mA	V _{REF} = V _{DD} = V _{LOGIC} = 5.5 V, gain = 2
Reference Input Range	1		V _{DD}	V	Gain = 1
	1		V _{DD} /2	V	Gain = 2
Reference Input Impedance		7		kΩ	Gain = 1
		3.5		kΩ	Gain = 2
REFERENCE OUTPUT					
Output Voltage ⁵	2.4975		2.5025	V	
Voltage Reference Temperature Coefficient (TC) ^{6,7}		2	5	ppm/°C	See the Terminology section
Output Impedance		0.04		Ω	
Output Voltage Noise		13		μV p-p	0.1 Hz to 10 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Noise Density		240		nV/ $\sqrt{\text{Hz}}$	At ambient temperature (T_A), $f = 10 \text{ kHz}$, $C_L = 10 \text{ nF}$, gain = 1 or 2
Load Regulation Sourcing		29		$\mu\text{V}/\text{mA}$	At ambient temperature
Load Regulation Sinking		74		$\mu\text{V}/\text{mA}$	At ambient temperature
Output Current Load Capability		± 20		mA	$V_{DD} \geq 3 \text{ V}$
Line Regulation		43		$\mu\text{V}/\text{V}$	At ambient temperature
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles
LOGIC INPUTS					
Input Current			± 1	μA	Per pin
Input Voltage (V_{IN})					
Low (V_{INL})			$0.3 \times V_{LOGIC}$	V	
High (V_{INH})	$0.7 \times V_{LOGIC}$			V	
Pin Capacitance		4		pF	
LOGIC OUTPUTS (SDO)					
Output Voltage (V_{OUT})					
Low (V_{OL})			0.4	V	Sink current (I_{SINK}) = 200 μA
High (V_{OH})	$V_{LOGIC} - 0.4$			V	Source current (I_{SOURCE}) = 200 μA
Floating State Output Capacitance		9		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.62		5.5	V	
I_{LOGIC}			1	μA	Power-on, -40°C to $+105^\circ\text{C}$
			1.3	μA	Power-on, -40°C to $+125^\circ\text{C}$
			0.5	μA	Power-down, -40°C to $+105^\circ\text{C}$
			1.3	μA	Power-down, -40°C to $+125^\circ\text{C}$
V_{DD}	2.7		5.5	V	Gain = 1
	$V_{REF} + 1.5$		5.5	V	Gain = 2
Supply Current (I_{DD})					$V_{INH} = V_{DD}$, $V_{INL} = \text{GND}$, $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$
Normal Mode ⁸		2.3	2.53	mA	Internal reference off, -40°C to $+85^\circ\text{C}$
		3.4	3.8	mA	Internal reference on, -40°C to $+85^\circ\text{C}$
		2.3	2.6	mA	Internal reference off
		3.4	4.2	mA	Internal reference on
All Power-Down Modes ⁹		2	3.4	μA	Power-down to 1 k Ω , -40°C to $+85^\circ\text{C}$
		2	5	μA	Power-down to 1 k Ω , -40°C to $+105^\circ\text{C}$
		2	11	μA	Power-down to 1 k Ω , -40°C to $+125^\circ\text{C}$

¹ DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when $V_{REF} = V_{DD}$ with gain = 1, or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280.

² $V_{DD} = 5 \text{ V}$. The device includes current limiting intended to protect the devices during temporary overload conditions. Junction temperature (T_J) can be exceeded during current limit. Operation above the specified maximum operation junction temperature can impair device reliability.

³ When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 $\Omega \times 1 \text{ mA} = 25 \text{ mV}$.

⁴ Time to exit power-down to normal mode of operation, $\overline{\text{SYNC}}$ rising edge to 90% of DAC midscale value, with output unloaded.

⁵ Initial accuracy presolder reflow is $\pm 750 \mu\text{V}$. Output voltage includes the effects of preconditioning drift. See the Internal Reference Setup section.

⁶ Reference is trimmed and tested at two temperatures and is characterized from -40°C to $+125^\circ\text{C}$.

⁷ Voltage reference temperature coefficient is calculated as per the box method. See the Terminology section for further information.

⁸ Interface inactive. All DACs active. DAC outputs unloaded.

⁹ All DACs powered down.

AC CHARACTERISTICS

$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$, $1.62\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$, $R_L = 2\text{ k}\Omega$ to GND, $C_L = 200\text{ pF}$ to GND, all specifications are $T_J = -40^\circ\text{C to } +125^\circ\text{C}$, typical at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE SETTling TIME ¹	6	8		μs	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to ± 2 LSB
SLEW RATE		0.8		$\text{V}/\mu\text{s}$	
DIGITAL-TO-ANALOG GLITCH IMPULSE ¹		1.4		$\text{nV}\cdot\text{sec}$	1 LSB change around major carry (internal reference, gain = 1)
DIGITAL FEEDTHROUGH ¹		0.13		$\text{nV}\cdot\text{sec}$	
CROSSTALK ¹					
Digital		0.1		$\text{nV}\cdot\text{sec}$	Internal reference, gain = 2
Analog		-0.25		$\text{nV}\cdot\text{sec}$	
DAC-to-DAC		-1.3		$\text{nV}\cdot\text{sec}$	
DAC-to-DAC		-2.0		$\text{nV}\cdot\text{sec}$	
TOTAL HARMONIC DISTORTION ²		-80		dB	At $T_A = 25^\circ\text{C}$, bandwidth = 20 kHz, $V_{DD} = 5\text{ V}$, output frequency (f_{OUT}) = 1 kHz, internal reference, gain = 2
OUTPUT NOISE SPECTRAL DENSITY ¹		300		$\text{nV}/\sqrt{\text{Hz}}$	DAC code = midscale, 10 kHz, gain = 2
OUTPUT NOISE ¹		6		$\mu\text{V p-p}$	0.1 Hz to 10 Hz, gain = 1
SIGNAL-TO-NOISE RATIO (SNR)		90		dB	At $T_A = 25^\circ\text{C}$, bandwidth = 20 kHz, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$, internal reference
SPURIOUS-FREE DYNAMIC RANGE (SFDR)		83		dB	At $T_A = 25^\circ\text{C}$, bandwidth = 20 kHz, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$, internal reference
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)		80		dB	At $T_A = 25^\circ\text{C}$, bandwidth = 20 kHz, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$, internal reference, gain = 2

¹ See the Terminology section. Measured using internal reference and gain = 1, unless otherwise noted.

² Digitally generated sine wave (f_{OUT}) at 1 kHz.

TIMING CHARACTERISTICS

All input signals are specified with rise time (t_R) = fall time (t_F) = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{INL} + V_{INH})/2$. See Figure 2. $V_{DD} = 2.7\text{ V to } 5.5\text{ V}$, $1.62\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$. $V_{REF} = 2.5\text{ V}$. All specifications are $T_J = -40^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Symbol	$1.62\text{ V} \leq V_{LOGIC} < 2.7\text{ V}$		$2.7\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t_1	20		20		ns
SCLK High Time	t_2	8		8		ns
SCLK Low Time	t_3	10		12		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time	t_4	15		11		ns
Data Setup Time	t_5	2		3		ns
Data Hold Time	t_6	2		2		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	4		4		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	15		12		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{SYNC}}$ Rising Edge (DAC Register Updates)	t_9	870		830		ns
$\overline{\text{SYNC}}$ Falling Edge to SCLK Fall Ignore	t_{10}	4		4		ns
$\overline{\text{LDAC}}$ Pulse Width Low	t_{11}	12		12		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Rising Edge	t_{12}	27		27		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Falling Edge	t_{13}	25		25		ns
$\overline{\text{LDAC}}$ Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_{14}	840		840		ns
Minimum Pulse Width Low	t_{15}	8		10		ns
Pulse Activation Time	t_{16}	115		115		ns

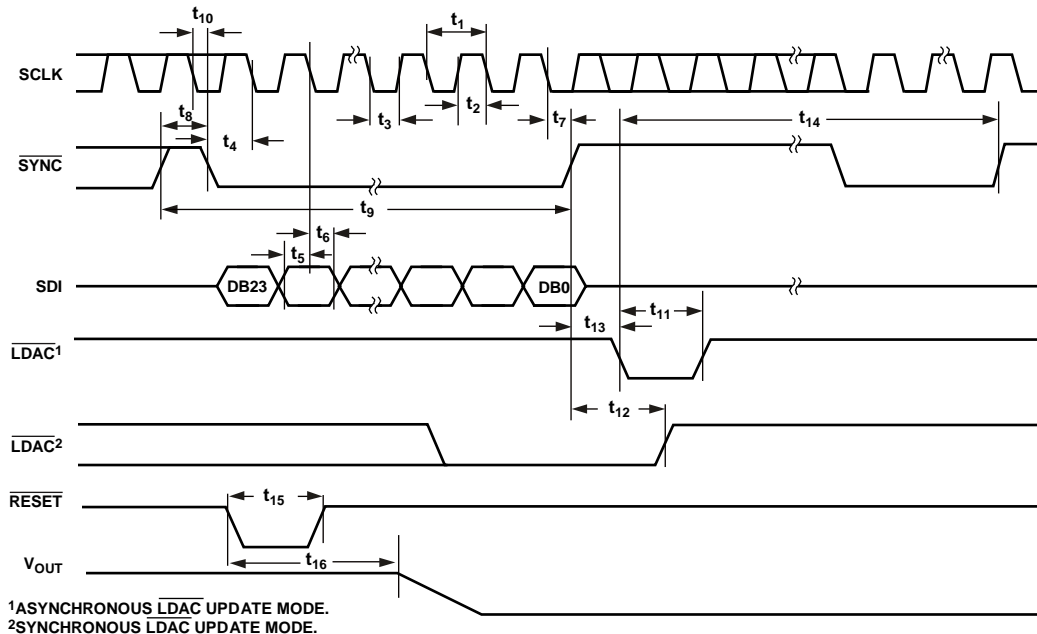


Figure 2. Serial Write Operation

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DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_r = t_f = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{INL} + V_{INH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $1.62 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$. $V_{REF} = 2.5 \text{ V}$. All specifications are $T_j = -40^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted. $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$.

Table 5.

Parameter	Symbol	1.62V ≤ V _{LOGIC} < 2.7V		2.7V ≤ V _{LOGIC} ≤ 5.5V		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t ₁	130		110		ns
SCLK High Time	t ₂	33		23		ns
SCLK Low Time	t ₃	12		7		ns
SYNC to SCLK Falling Edge	t ₄	80		80		ns
Data Setup Time	t ₅	2		2		ns
Data Hold Time	t ₆	2		2		ns
SCLK Falling Edge to SYNC Rising Edge	t ₇	35		10		ns
Minimum SYNC High Time	t ₈	55		32		ns
SDO Data Valid from SCLK Rising Edge	t ₉		130		75	ns
SYNC Rising Edge to SCLK Falling Edge	t ₁₀	15		8		ns
SYNC Rising Edge to SDO Disable	t ₁₁	218		210		ns

Circuit and Timing Diagrams

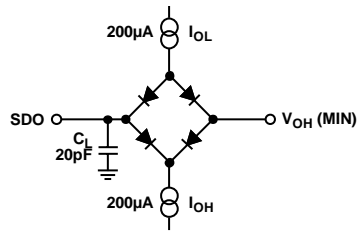


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

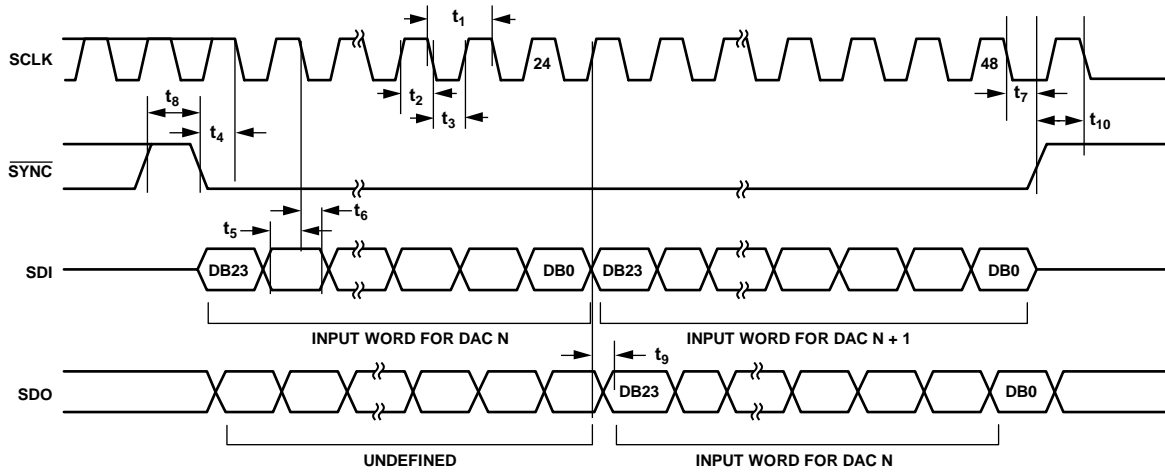


Figure 4. Daisy Chain Timing Diagram

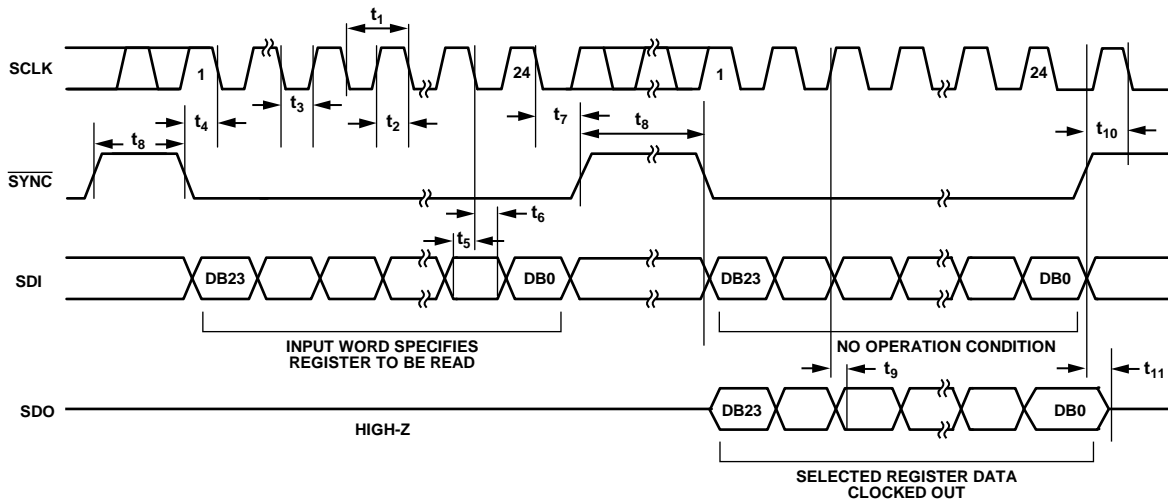


Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	-0.3 V to +7 V
V_{LOGIC} to GND	-0.3 V to +7 V
V_{OUTX} to GND	-0.3 V to $V_{DD} + 0.3$ V
V_{REF} to GND	-0.3 V to $V_{DD} + 0.3$ V
Digital Input Voltage to GND	-0.3 V to $V_{LOGIC} + 0.3$ V
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Absolute Maximum Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
28-Lead LFCSP (CP-28-8) ¹	55.09	24.49	19.14	2.62	23.92	°C/W

¹ Thermal impedance simulated values are based on a JEDEC 252P thermal test board with nine thermal vias. See JEDEC JESD51.

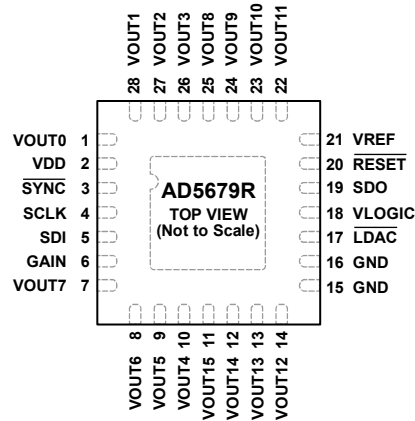
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE TIED TO GND.

17326-006

Figure 6. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT0	Analog Output Voltage from DAC 0. The output amplifier has rail-to-rail operation.
2	VDD	Power Supply Input. These devices operate from 2.7 V to 5.5 V. Decouple the VDD supply with a 10 μ F capacitor in parallel with a 0.1 μ F capacitor to GND.
3	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data transfers in on the falling edges of the next 24 clocks.
4	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data transfers at rates of up to 50 MHz.
5	SDI	Serial Data Input. The AD5679R has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
6	GAIN	Span Set Pin. When this pin is tied to GND, all sixteen DAC outputs have a span from 0 V to VREF. If this pin is tied to VLOGIC, all sixteen DACs output a span of 0 V to $2 \times V_{\text{REF}}$.
7	VOUT7	Analog Output Voltage from DAC 7. The output amplifier has rail-to-rail operation.
8	VOUT6	Analog Output Voltage from DAC 6. The output amplifier has rail-to-rail operation.
9	VOUT5	Analog Output Voltage from DAC 5. The output amplifier has rail-to-rail operation.
10	VOUT4	Analog Output Voltage from DAC 4. The output amplifier has rail-to-rail operation.
11	VOUT15	Analog Output Voltage from DAC 15. The output amplifier has rail-to-rail operation.
12	VOUT14	Analog Output Voltage from DAC 14. The output amplifier has rail-to-rail operation.
13	VOUT13	Analog Output Voltage from DAC 13. The output amplifier has rail-to-rail operation.
14	VOUT12	Analog Output Voltage from DAC 12. The output amplifier has rail-to-rail operation.
15, 16	GND	Ground Reference Point for All Circuitry on the Device.
17	$\overline{\text{LDAC}}$	Load DAC. $\overline{\text{LDAC}}$ operates in two modes: asynchronously and synchronously. Pulsing this pin low updates any or all DAC registers if the input registers have new data, which simultaneously updates all DAC outputs. This pin can also be tied permanently low.
18	VLOGIC	Digital Power Supply. The voltage on this pin is specified in Table 2.
19	SDO	Serial Data Output. This pin can be used to daisy-chain a number of devices together, or it can be used for readback. The serial data transfers on the rising edge of SCLK and is valid on the falling edge.
20	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero-scale.
21	VREF	Reference Output Voltage. When using the internal reference, this is the reference output pin. This pin is the reference output by default.
22	VOUT11	Analog Output Voltage from DAC 11. The output amplifier has rail-to-rail operation.
23	VOUT10	Analog Output Voltage from DAC 10. The output amplifier has rail-to-rail operation.
24	VOUT9	Analog Output Voltage from DAC 9. The output amplifier has rail-to-rail operation.
25	VOUT8	Analog Output Voltage from DAC 8. The output amplifier has rail-to-rail operation.
26	VOUT3	Analog Output Voltage from DAC 3. The output amplifier has rail-to-rail operation.
27	VOUT2	Analog Output Voltage from DAC 2. The output amplifier has rail-to-rail operation.
28	VOUT1	Analog Output Voltage from DAC 1. The output amplifier has rail-to-rail operation.
	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

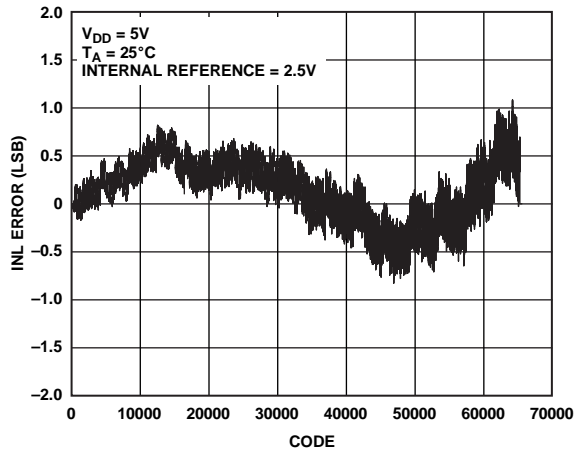


Figure 7. INL Error vs. Code

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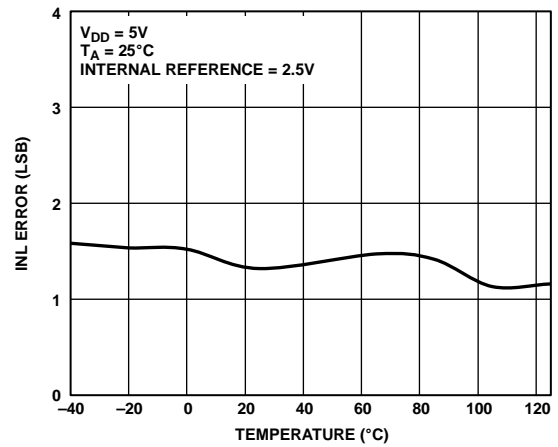


Figure 10. INL Error vs. Temperature

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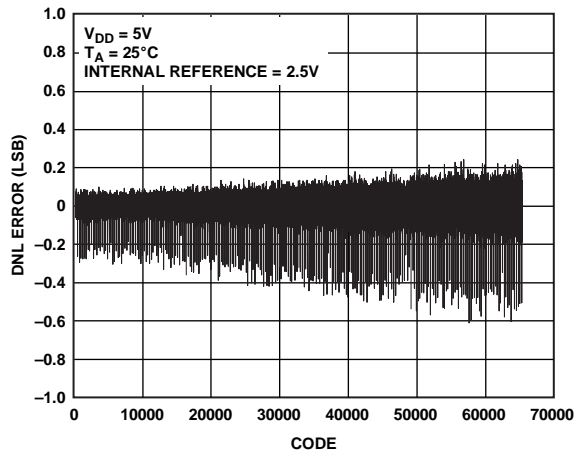


Figure 8. DNL Error vs. Code

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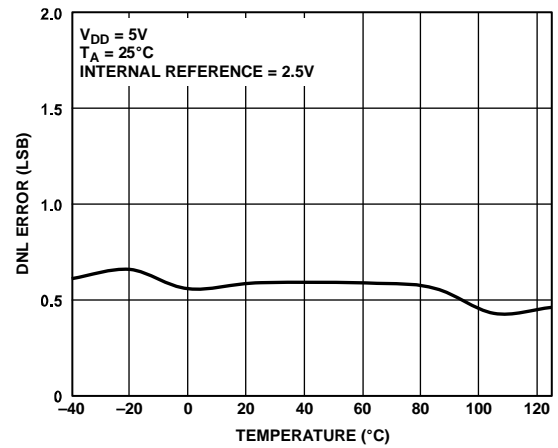


Figure 11. DNL Error vs. Temperature

17326-011

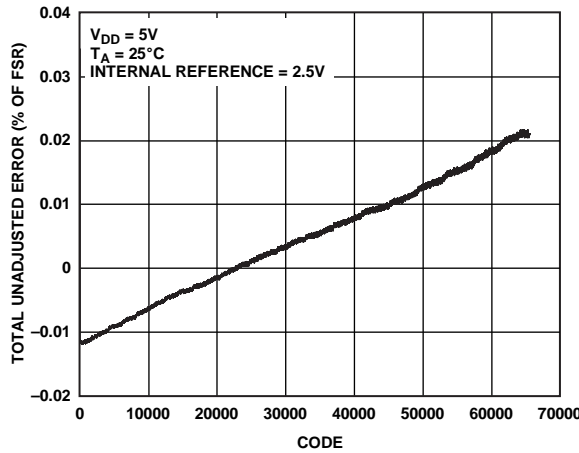


Figure 9. Total Unadjusted Error vs. Code

17326-009

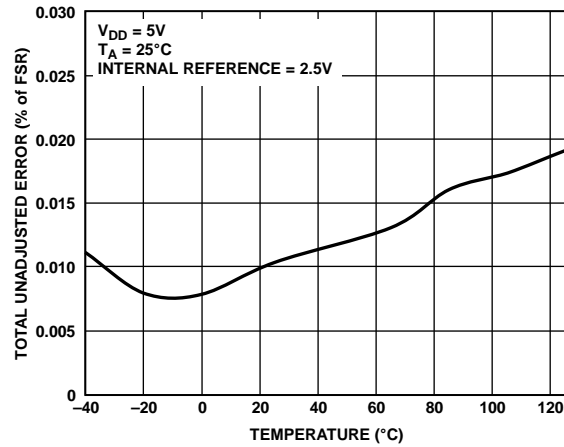


Figure 12. Total Unadjusted Error vs. Temperature

17326-012

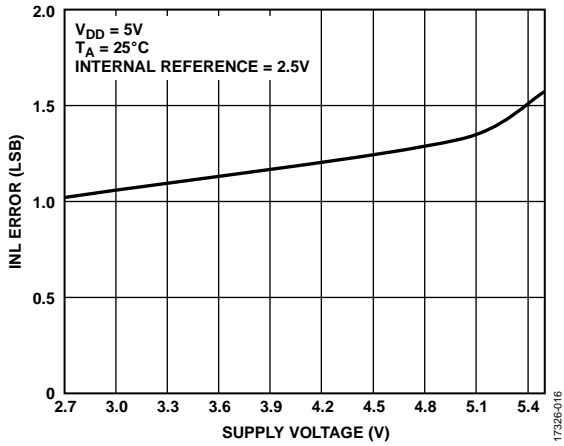


Figure 13. INL Error vs. Supply Voltage

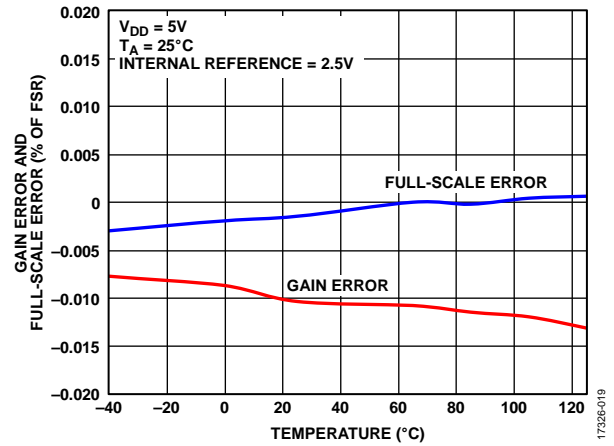


Figure 16. Gain Error and Full-Scale Error vs. Temperature

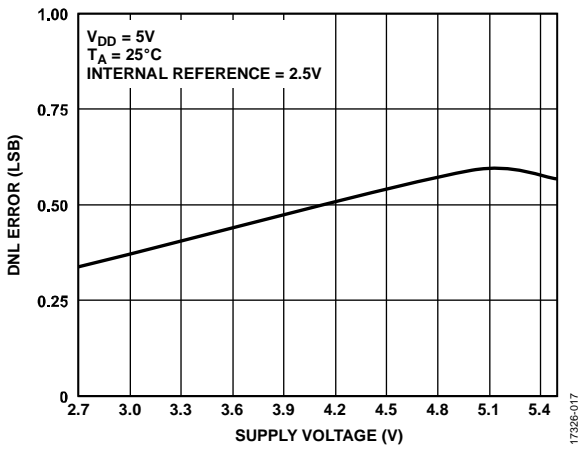


Figure 14. DNL Error vs. Supply Voltage

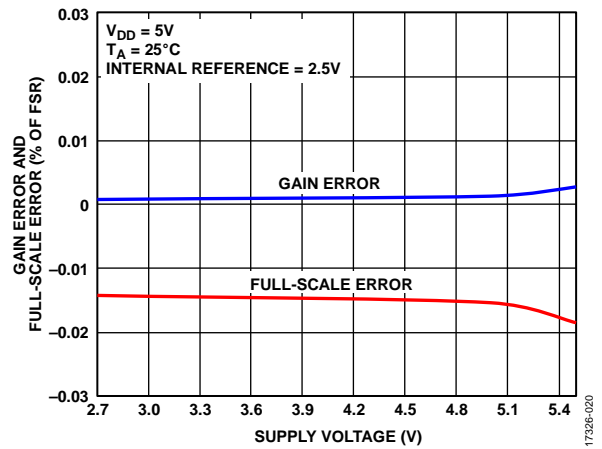


Figure 17. Gain Error and Full-Scale Error vs. Supply Voltage

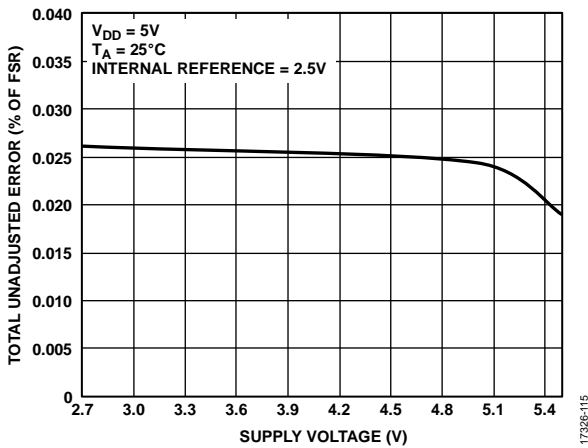


Figure 15. Total Unadjusted Error vs. Supply Voltage

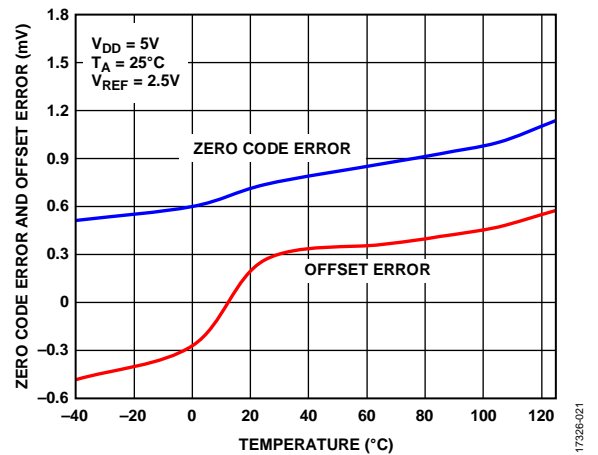


Figure 18. Zero Code Error and Offset Error vs. Temperature

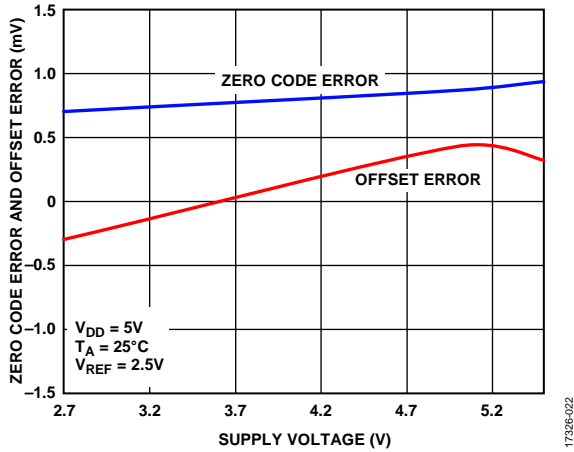


Figure 19. Zero Code Error and Offset Error vs. Supply Voltage

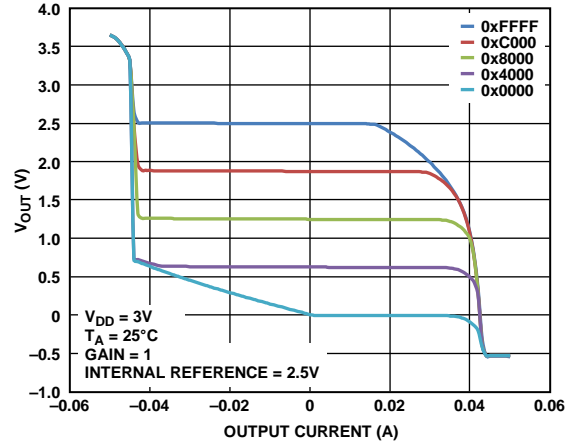


Figure 22. Source and Sink Capability at 3V

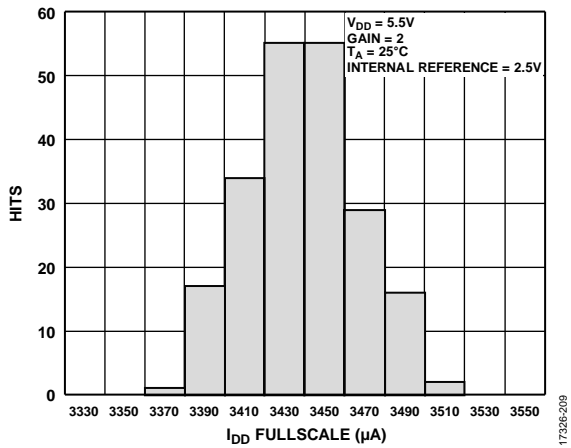


Figure 20. Supply Current (I_{DD}) Histogram with Internal Reference

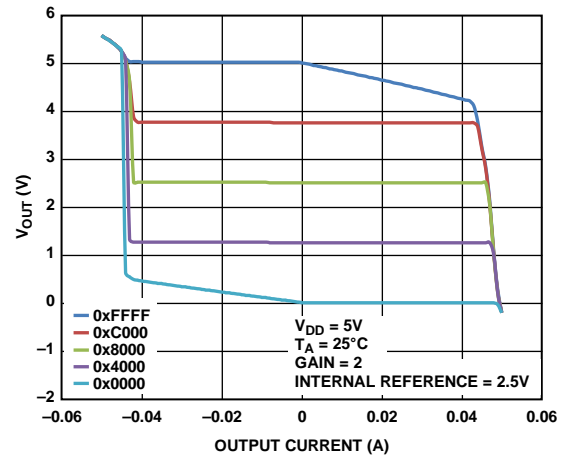


Figure 23. Source and Sink Capability at 5V

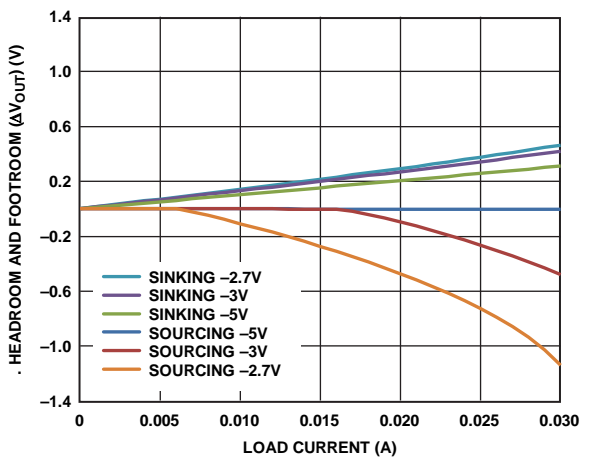


Figure 21. Headroom and Footroom (ΔV_{out}) vs. Load Current

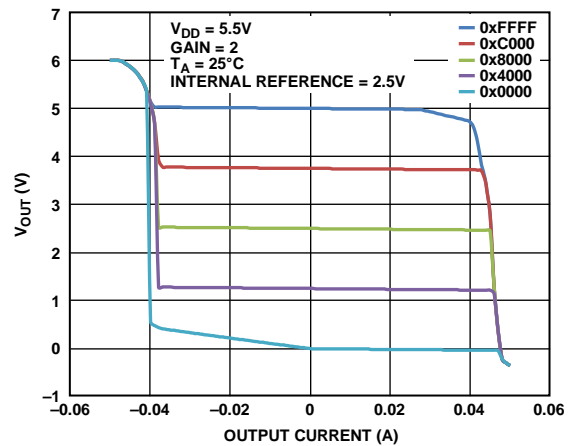


Figure 24. Source and Sink Capability at 5.5V

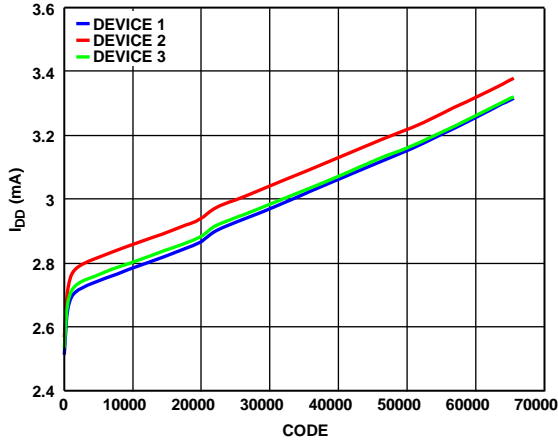


Figure 25. I_{DD} vs. Code

17326-206

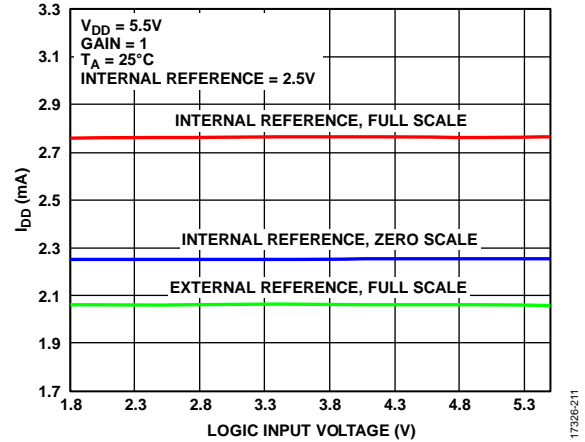


Figure 28. I_{DD} vs. Logic Input Voltage

17326-211

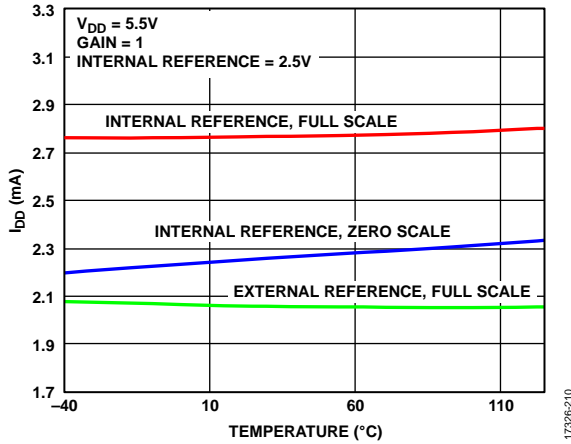


Figure 26. I_{DD} vs. Temperature

17326-210

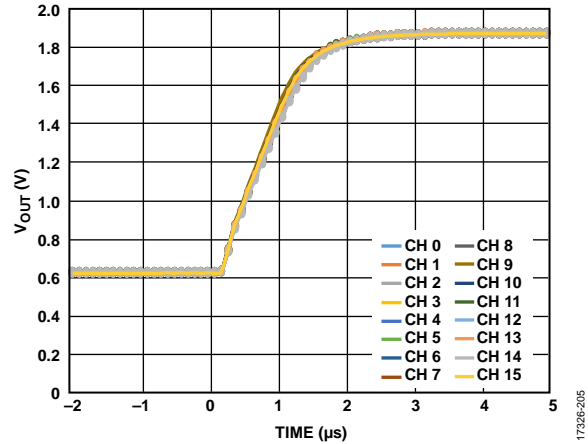


Figure 29. Settling Time

17326-205

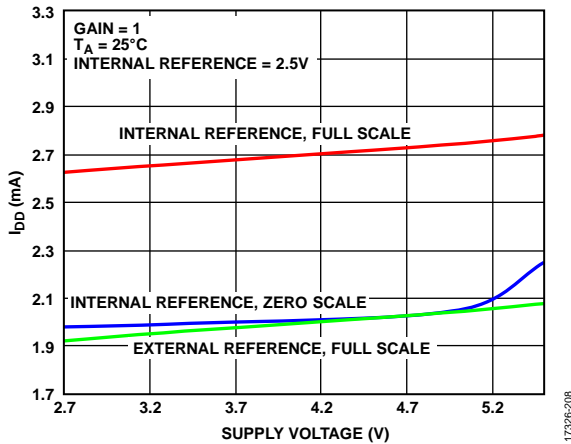


Figure 27. I_{DD} vs. Supply Voltage

17326-208

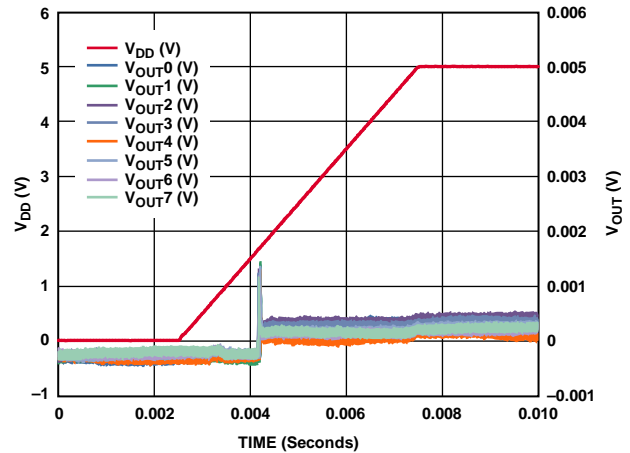


Figure 30. POR to 0 V and Midscale Output

17326-032

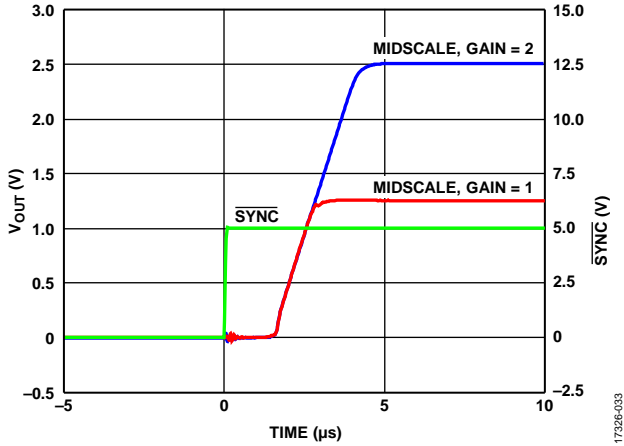


Figure 31. Exiting Power-Down to Midscale

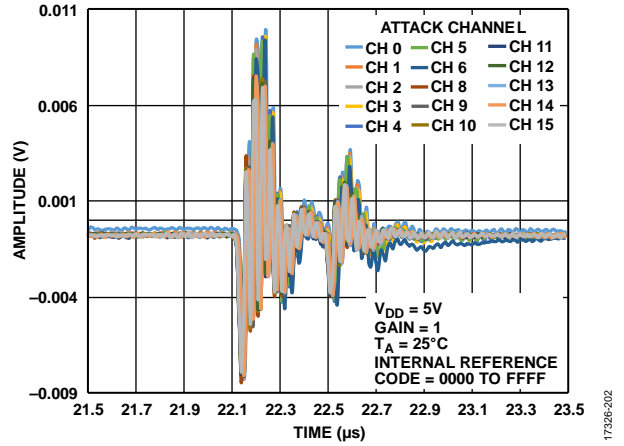


Figure 34. DAC-to-DAC Crosstalk

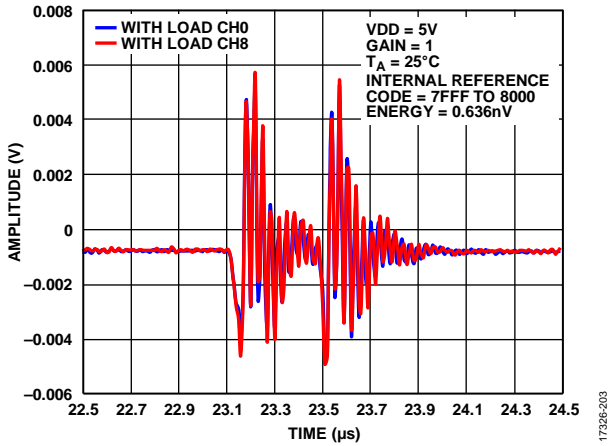


Figure 32. Digital-to-Analog Glitch Impulse

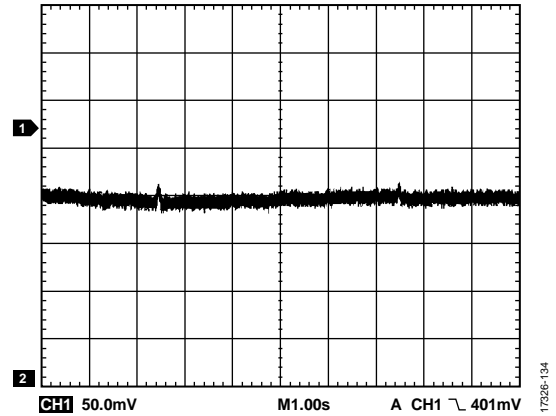


Figure 35. 0.1 Hz to 10 Hz Output Noise

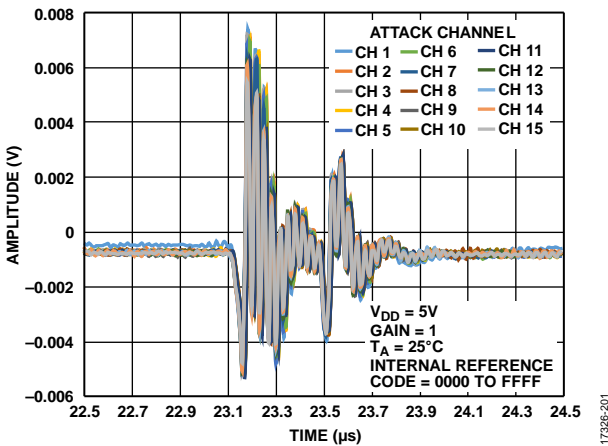


Figure 33. Analog Crosstalk

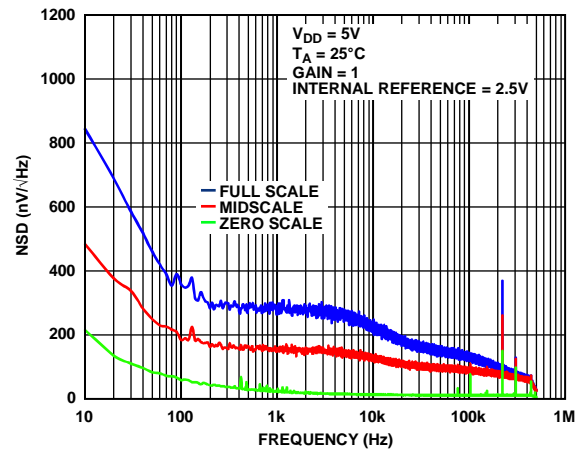


Figure 36. Noise Spectral Density (NSD)

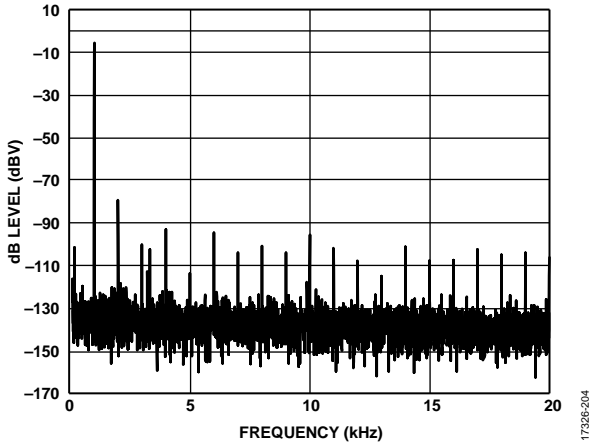


Figure 37. Total Harmonic Distortion (THD) at 1 kHz

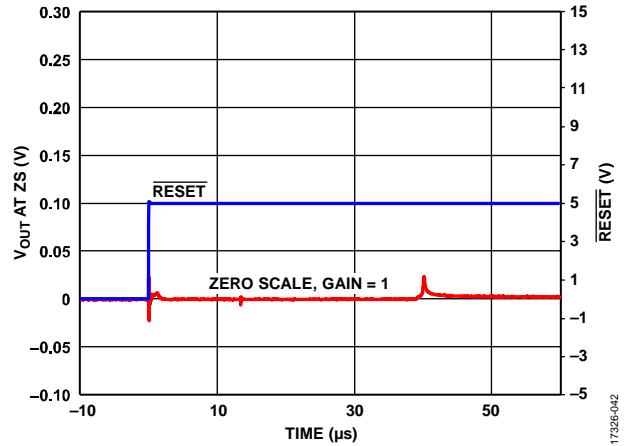


Figure 39. Hardware Reset

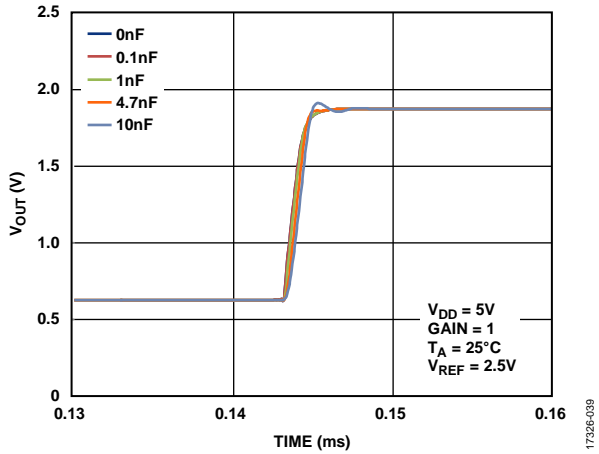


Figure 38. Settling Time at Various Capacitive Loads

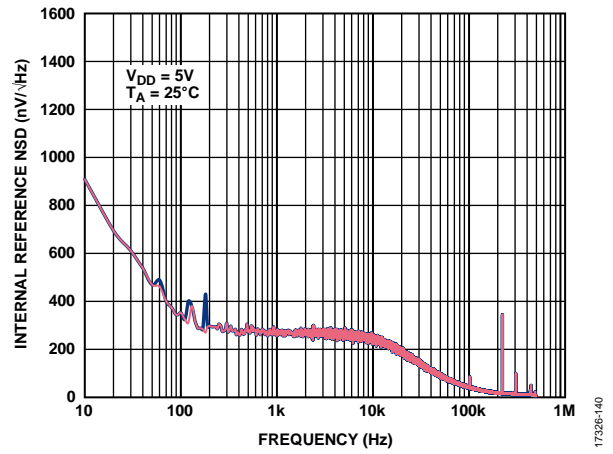


Figure 40. Internal Reference NSD vs. Frequency

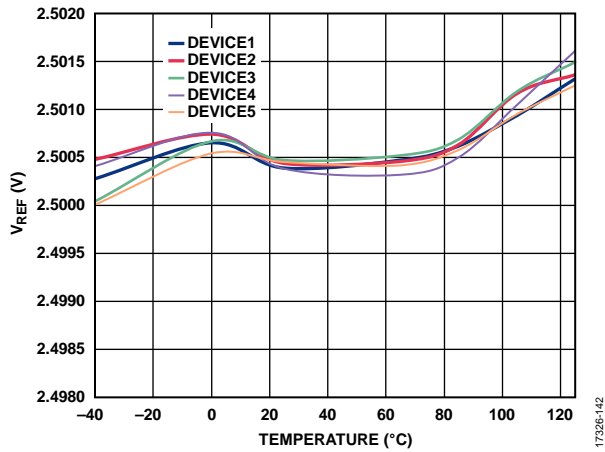


Figure 41. V_{REF} vs. Temperature

17326-142

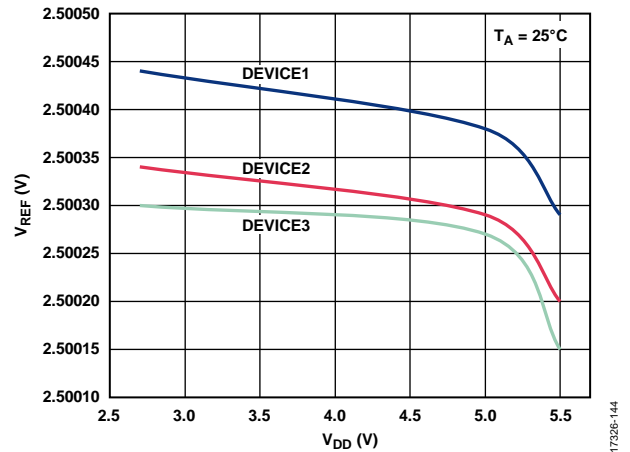


Figure 43. V_{REF} vs. V_{DD}

17326-144

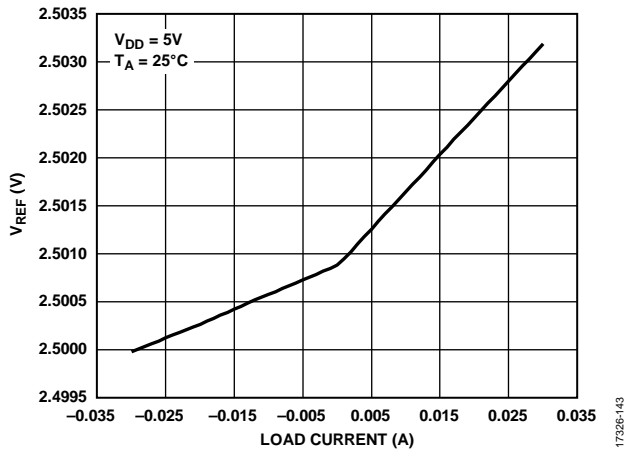


Figure 42. V_{REF} vs. Load Current

17326-143

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. These DACs are guaranteed monotonic by design.

Zero Code Error

Zero code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. The ideal output is 0 V. The zero code error is always positive because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Full-Scale Error

Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. The ideal output is $V_{DD} - 1$ LSB. Full-scale error is expressed in percent of full-scale range (% of FSR).

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. Offset error drift is expressed in $\mu\text{V}/^\circ\text{C}$.

Offset Error

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 256 loaded in the DAC register. Offset error can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)

The dc PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. PSRR is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by $\pm 10\%$.

Output Voltage Settling Time

The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a $\frac{1}{4}$ to $\frac{3}{4}$ full-scale input change and is measured from the rising edge of SYNC.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. Digital-to-analog glitch impulse is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. Digital feedthrough is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. Reference feedthrough is expressed in dB.

Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density ($\text{nV}/\sqrt{\text{Hz}}$). Noise spectral density is measured by loading the DAC to midscale and measuring noise at the output. Noise spectral density is measured in $\text{nV}/\sqrt{\text{Hz}}$.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. DC crosstalk is measured with a full-scale output change on one DAC (or soft power-down and power-up) when monitoring another DAC kept at midscale. DC crosstalk is expressed in μV .

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. DC crosstalk due to load current change is expressed in $\mu\text{V}/\text{mA}$.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. Digital crosstalk is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. Analog crosstalk is measured by first loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then, execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. DAC-to-DAC crosstalk is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands when monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The multiplying bandwidth is a measure of the finite bandwidth of the amplifiers within the DAC. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. THD is measured in dB.

Voltage Reference TC

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range, expressed in ppm/°C, shown in the following equation:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temperature\ Range} \right] \times 10^6$$

where:

$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.

$V_{REF(MIN)}$ is the minimum reference output measured over the total temperature range.

$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V.

Temperature Range is the specified temperature range of -40°C to $+125^{\circ}\text{C}$.

THEORY OF OPERATION

DAC

The AD5679R is a 16-channel, 16-bit, serial input, voltage output DAC with an internal reference. The device operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5679R in a 24-bit word format via a 3-wire serial interface. The AD5679R incorporates a power-on reset circuit to ensure that the DAC output powers up to a known output state. The device also has a software power-down mode that reduces the typical current consumption to 2 μ A.

TRANSFER FUNCTION

The internal reference is on by default.

The gain of the output amplifier can be set to $\times 1$ or $\times 2$ using the span set pin (GAIN). When the GAIN pin is tied to GND, all 16 DAC outputs have a span from 0 V to V_{REF} . When the GAIN pin is tied to VLOGIC, all 16 DACs output a span of 0 V to $2 \times V_{REF}$.

DAC ARCHITECTURE

The AD5679R implements a segmented string DAC architecture with an internal output buffer. Figure 44 shows the internal block diagram.

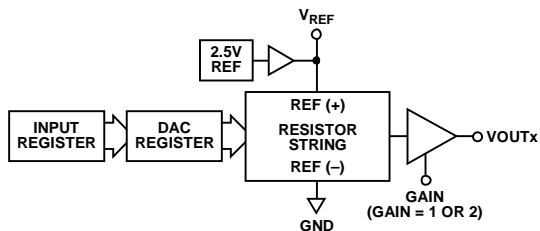


Figure 44. Single DAC Channel Architecture Block Diagram

Figure 45 shows the resistor string structure. The code loaded to the DAC register determines the node on the string where the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches and connecting the string to the amplifier. Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

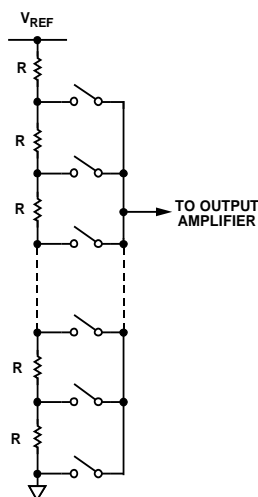


Figure 45. Resistor String Structure

Internal Reference

The AD5679R on-chip reference is enabled at power-up, but can be disabled via a write to the control register. See the Internal Reference Setup section for details.

The AD5679R have a 2.5 V, 2 ppm/ $^{\circ}$ C reference, resulting in a full-scale output of 2.5 V or 5 V, depending on the state of the GAIN pin. The internal reference associated with the device is available at the VREFOUT pin. This buffered reference is capable of driving external loads of up to 15 mA.

Output Amplifiers

The output buffer amplifier generates rail-to-rail voltages on its output. The actual range depends on the value of V_{REF} , the gain setting, the offset error, and the gain error.

The output amplifiers can drive a load of 1 k Ω in parallel with 10 nF to GND. The slew rate is 0.8 V/ μ s, with a typical $\frac{1}{4}$ to $\frac{3}{4}$ scale settling time of 6 μ s.

SERIAL INTERFACE

The AD5679R uses a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDI), compatible with SPI, QSPI[™], and MICROWIRE interface standards, as well as most digital signal processors (DSPs). See Figure 2 for a timing diagram of a typical write sequence. The AD5679R contains an SDO pin to allow the user to daisy-chain multiple devices together (see the Daisy-Chain Operation section) or for readback.

Input Shift Register

The input shift register of the AD5679R is 24 bits wide. Data is loaded MSB first (DB23), and the first four bits are the command bits, C3 to C0 (see Table 9), followed by the 4-bit DAC address bits, A3 to A0 (see Table 10), and finally, the 16-bit data-word.

The data-word comprises 16-bit input code for the AD5679R (see Figure 46). These data bits are transferred to the input register on the 24 falling edges of SCLK and are updated on the rising edge of $\overline{\text{SYNC}}$.

Commands execute on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

Table 9. Command Definitions

Command				Description
C3	C2	C1	C0	
0	0	0	0	No operation
0	0	0	1	Write to Input Register n where n = 1 to 8, depending on the DAC selected from the address bits in Table 10 (dependent on $\overline{\text{LDAC}}$)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up the DAC
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference setup register
1	0	0	0	Set up the daisy-chain enable (DCEN) register
1	0	0	1	Set up the readback register (readback enable)
1	0	1	0	Update all channels of the input register simultaneously with the input data
1	0	1	1	Update all channels of the DAC register and input register simultaneously with the input data
1	1	0	0	Reserved
...	
1	1	1	1	No operation, daisy-chain mode

Table 10. Address Commands

Channel Address[3:0]				Selected Channel
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4
0	1	0	1	DAC 5
0	1	1	0	DAC 6
0	1	1	1	DAC 7
1	0	0	0	DAC 8
1	0	0	1	DAC 9
1	0	1	0	DAC 10
1	0	1	1	DAC 11
1	1	0	0	DAC 12
1	1	0	1	DAC 13
1	1	1	0	DAC 14
1	1	1	1	DAC 15

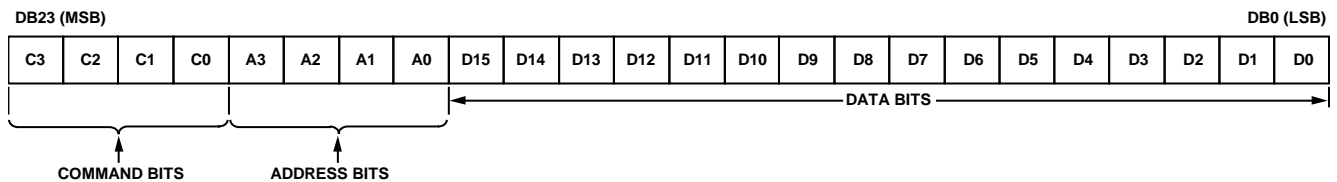


Figure 46. Input Shift Register Content

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STANDALONE OPERATION

Bring the $\overline{\text{SYNC}}$ line low to begin the write sequence. Data from the SDI line is clocked into the 24-bit input shift register on the falling edge of SCLK. After the last of 24 data bits is clocked in, bring $\overline{\text{SYNC}}$ high. The programmed function is then executed, that is, an $\overline{\text{LDAC}}$ dependent change in DAC register contents and/or a change in the mode of operation. If $\overline{\text{SYNC}}$ is brought high at a clock before the 24th clock, it is considered a valid frame, and invalid data is loaded to the DAC. Bring $\overline{\text{SYNC}}$ high for a minimum of 20 ns (single channel, see t_s in Figure 2) before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. Idle $\overline{\text{SYNC}}$ at rails between write sequences for even lower power operation. The $\overline{\text{SYNC}}$ line is kept low for 24 falling edges of SCLK, and the DAC is updated on the rising edge of $\overline{\text{SYNC}}$.

When data is transferred to the input register of the addressed DAC, all DAC registers and outputs update by bringing $\overline{\text{LDAC}}$ low while the $\overline{\text{SYNC}}$ line is high.

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on $\overline{\text{LDAC}}$)

Command 0001 allows the user to write the dedicated input register of each DAC individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent, if not controlled by the $\overline{\text{LDAC}}$ mask register.

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers and outputs with the contents of the input registers selected and updates the DAC outputs directly. Data Bit D15 to Bit D0 determine which DACs have data from the input register transferred to the DAC register. Setting a bit to 1 transfers data from the input register to the appropriate DAC register.

Write to and Update DAC Channel n (Independent of $\overline{\text{LDAC}}$)

Command 0011 allows the user to write to the DAC registers and updates the DAC outputs directly. The address bits are used to select the DAC channel.

DAISY-CHAIN OPERATION

For systems that contain several DACs, the SDO pin can daisy-chain several devices together and is enabled through a software executable DCEN command. Command 1000 is reserved for this DCEN function (see Table 9). The daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The default setting is standalone mode, where DB0 = 0. Table 11 shows how the state of the bit corresponds to the mode of operation of the device.

Table 11. DCEN Register

DB0	Description
0	Standalone mode (default)
1	DCEN mode

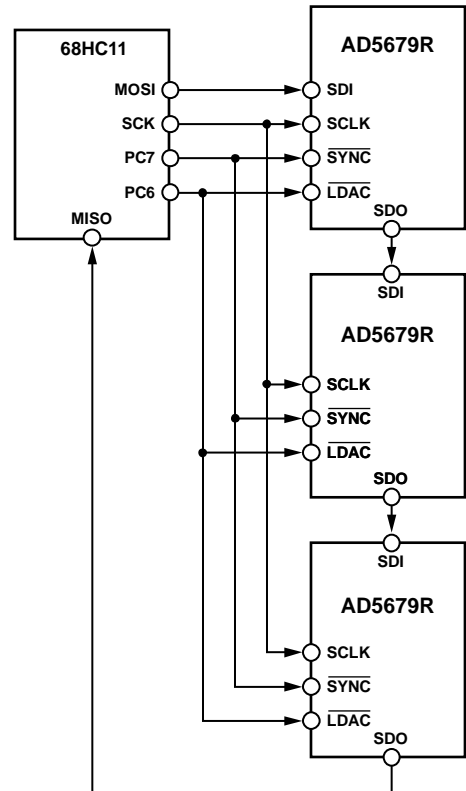


Figure 47. Daisy-Chaining the AD5679R to a Motorola® 68HC11

The SCLK pin is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the SDI input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal $24 \times N$, where N is the total number of devices updated. If $\overline{\text{SYNC}}$ is brought high at a clock that is not a multiple of 24, it is considered a valid frame, and invalid data may be loaded to the DAC. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ goes high, which latches the input data in each device in the daisy-chain and prevents any further data from being clocked into the input shift register. The serial clock can be continuous or a gated clock. If $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles, a continuous SCLK source is used. In gated clock mode, use a burst clock containing the exact number of clock cycles, and bring $\overline{\text{SYNC}}$ high after the final clock to latch the data.

READBACK OPERATION

Readback mode is invoked through a software executable readback command. If the SDO output is disabled via the daisy-chain mode disable bit in the control register, the SDO output is automatically enabled for the duration of the read operation, after which the SDO output is disabled again. Command 1001 is reserved for the readback function. This command, in association with the address bits (A3 to A0), selects the DAC input register to read (see Table 9 and Table 10). During readback, only one input register can be

selected. The remaining data bits in the write sequence are don't care bits. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register.

For example, to read back the DAC register for Channel 0, implement the following sequence:

1. Write 0x900000 to the AD5679R input register. This configures the device for read mode with the DAC register of Channel 0 selected. Note that all data bits, DB15 to DB0, are don't care bits.
2. Follow Step 1 with a second write, a no operation (NOP) condition, 0x000000 or 0xF00000 when in daisy-chain mode. During this write, the data from the register is clocked out on the SDO line. DB23 to DB20 contain undefined data, and the last 20 bits contain the DB19 to DB0 DAC register contents.

When SYNC is high, the SDO pin is driven by a weak latch that holds the last data bit. The SDO pin can be overdriven by the SDO pin of another device. Multiple devices can be read using the same SPI interface.

POWER-DOWN OPERATION

The AD5679R contains two separate power-down modes. Command 0100 is designated for the power-down function (see Table 9). These power-down modes are software programmable by setting 16 bits, Bit DB15 to Bit DB0, in the input shift register. There are two bits associated with each DAC channel. Table 12 shows how the state of the two bits corresponds to the mode of operation of the device.

Any or all DACs (DAC 0 to DAC 15) power down to the selected mode by setting the corresponding bits. See Table 13 and Table 14 for the contents of the input shift register during the power-down/power-up operation.

Table 12. Modes of Operation

Operating Mode	PD1	PD0
Normal Operation	0	0
Power-Down Modes 1 kΩ to GND	0	1

When both Bit PD1 and Bit PD0 in the input shift register are set to 0, the device works normally with a typical power consumption of 2.3 mA at 5 V. However, for the two power-down modes, the supply current typically falls to 2 μA. In addition to this fall, the output stage switches internally from the amplifier output to a resistor network of a known value. Therefore, the DAC channel output impedance is defined when the channel is powered down by internally connecting the output to GND through a 1 kΩ resistor. Figure 48 shows the output stage.

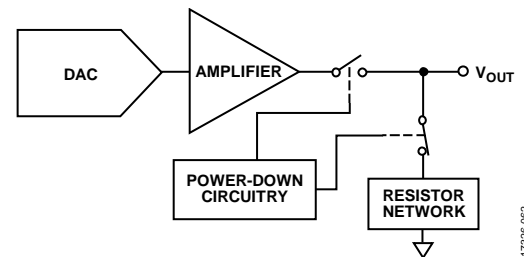


Figure 48. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register updates while the device is in power-down mode. The time required to exit power-down is typically 3 μs for V_{DD} = 5 V.

To reduce the current consumption further, power off the on-chip reference. See the Internal Reference Setup section.

Table 13. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation for Output Channels DAC 7 to DAC 0

[DB23:DB20]	DB19	[DB18:DB16]	DAC 7	DAC 6	DAC 5	DAC 4	DAC 3	DAC 2	DAC 1	DAC 0
			[DB15:DB14]	[DB13:DB12]	[DB11:DB10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	0	XXX ¹	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

¹ X means don't care

Table 14. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation for Output Channels DAC 15 to DAC 8

[DB23:DB20]	DB19	[DB18:DB16]	DAC 15	DAC 14	DAC 13	DAC 12	DAC 11	DAC 10	DAC 9	DAC 8
			[DB15:DB14]	[DB13:DB12]	[DB11:DB10]	[DB9:DB8]	[DB7:DB6]	[DB5:DB4]	[DB3:DB2]	[DB1:DB0]
0100	1	XXX ¹	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]	[PD1:PD0]

¹ X means don't care

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5679R DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the $\overline{\text{LDAC}}$ pin.

Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)

$\overline{\text{LDAC}}$ is held low and data is clocked to the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of $\overline{\text{SYNC}}$, and the output begins to change (see Table 16).

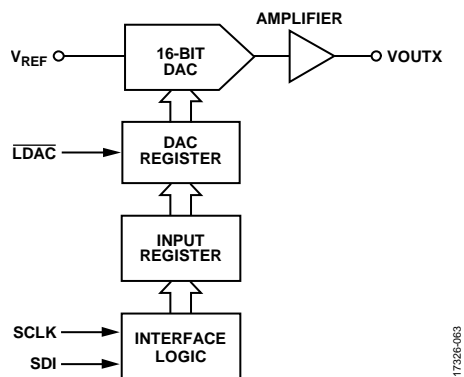


Figure 49. Simplified Diagram of Input Loading Circuitry for a Single DAC

Table 15. $\overline{\text{LDAC}}$ Overwrite Definition

Load $\overline{\text{LDAC}}$ Register		$\overline{\text{LDAC}}$ Operation
$\overline{\text{LDAC}}$ Bits (DB15 to DB0)	$\overline{\text{LDAC}}$ Pin	
0000000000000000	1 or 0	Determined by the $\overline{\text{LDAC}}$ pin.
1111111111111111	X ¹	DAC channels update and override the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 1.

¹ X means don't care.

Table 16. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table¹

Command	Description	Hardware $\overline{\text{LDAC}}$ Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)	VLOGIC GND ²	Data update Data update	No change (no update) Data update
0010	Update DAC Register n with contents of Input Register n	VLOGIC GND	No change No change	Updated with input register contents Updated with input register contents
0011	Write to and update DAC Channel n	VLOGIC GND	Data update Data update	Data update Data update

¹ A high to low hardware $\overline{\text{LDAC}}$ pin transition always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.

² When $\overline{\text{LDAC}}$ is permanently tied low, the $\overline{\text{LDAC}}$ mask bits are ignored.

Deferred DAC Updating ($\overline{\text{LDAC}}$ is Pulsed Low)

$\overline{\text{LDAC}}$ is held high and data is clocked to the input register using Command 0001. All DAC outputs are asynchronously updated by bringing $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is brought high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

$\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for this software $\overline{\text{LDAC}}$ function. Address bits are ignored. Writing to the DAC, using Command 0101, loads the 16-bit $\overline{\text{LDAC}}$ register (DB15 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wants to select which channels respond to the $\overline{\text{LDAC}}$ pin.

The $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 15). Setting the $\overline{\text{LDAC}}$ bits (DB0 to DB15) to 0 for a DAC channel means that this channel update is controlled by the hardware $\overline{\text{LDAC}}$ pin.

HARDWARE RESET (RESET)

The **RESET** pin is an active low reset that allows the outputs to be cleared to zero scale. It is necessary to keep the **RESET** pin low for a minimum time (see Table 4) to complete the operation. When the **RESET** signal is returned high, the output remains at the cleared value until a new value is programmed. When the **RESET** pin is low, the outputs cannot be updated with a new value. Any events on the LDAC pin or **RESET** pin during power-on reset are ignored. If the **RESET** pin is pulled low at power-up, the device does not initialize properly until the pin is released.

POWER-ON RESET INTERNAL CIRCUIT

The AD5679R contains a power-on reset circuit that controls the output voltage during power-up. The AD5679R powers up to zero scale. The output remains powered up at this level until a valid write sequence is made to the DAC.

SOFTWARE RESET

A software executable reset function is also available that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function. The DAC address bits must be set to 0x0 and the data bits set to 0x1234 for the software reset command to execute.

INTERNAL REFERENCE SETUP

The on-chip reference is on at power-up by default. To reduce the supply current, turn off this reference by setting the software programmable bit, DB0, in the control register. Table 17 shows how the state of the bit corresponds to the mode of operation. Command 0111 is reserved for setting up the internal reference (see Table 9 and Table 18).

Table 17. Internal Reference Setup Register

Bit	Description
DB2	Reserved
DB0	Reference enable DB0 = 0: internal reference enabled (default) DB0 = 1: internal reference disabled

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc., performs a reliability test called precondition to mimic the effect of soldering a device to a board. The output voltage specification quoted previously includes the effect of this reliability test.

Figure 50 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

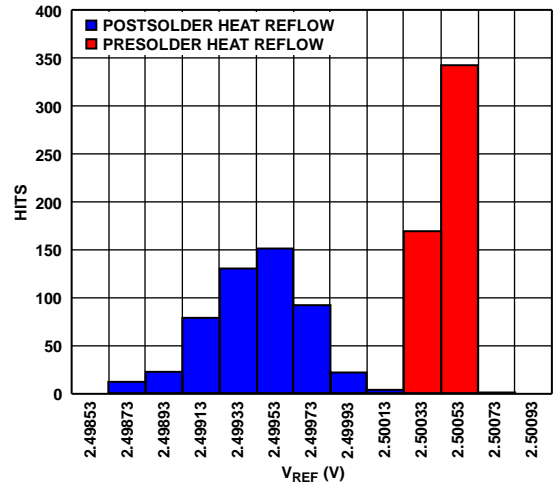


Figure 50. SHR Reference Voltage Shift

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold to hot, and then back to ambient.

Figure 51 shows thermal hysteresis data. Thermal hysteresis is measured by sweeping the temperature from ambient to -40°C, then to +125°C, and returning to ambient. The ΔV_{REF} , shown in blue in Figure 51, is then measured between the two ambient measurements. The same temperature sweep and measurements are immediately repeated and the results are shown in red in Figure 51.

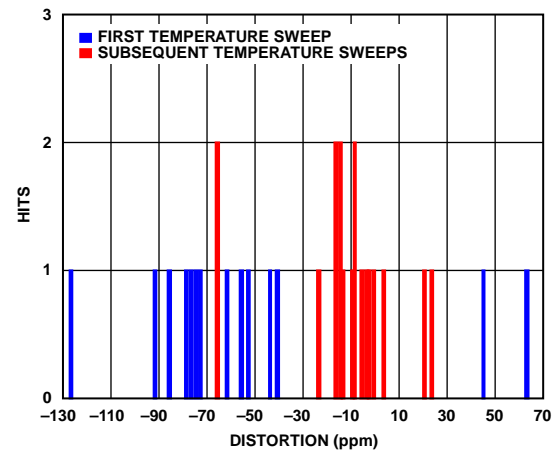


Figure 51. Thermal Hysteresis

Table 18. 24-Bit Input Shift Register Contents for Internal Reference Setup Command

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB3	DB2	DB1	DB0 (LSB)
0	1	1	1	Don't care	Reserved	Reserved, set to 0	Reference enable

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The following supplies typically power the AD5679R: $V_{DD} = 3.3\text{ V}$ and $V_{LOGIC} = 1.8\text{ V}$.

The ADP7118 can be used to power the VDD pin. The ADP160 can be used to power the VLOGIC pin. Figure 52 shows this setup. The ADP7118 can operate from input voltages up to 20 V. The ADP160 can operate from input voltages up to 5.5 V.

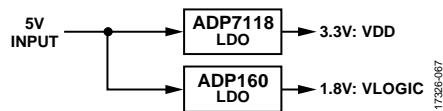


Figure 52. Low Noise Power Solution for the AD5679R

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5679R is performed via a serial bus that uses a standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The device requires a 24-bit data-word with data valid on the rising edge of SYNC.

AD5679R TO ADSP-BF531 INTERFACE

The SPI interface of the AD5679R can connect to industry-standard DSPs and microcontrollers. Figure 53 shows the AD5679R connected to the Analog Devices Blackfin® DSP. The Blackfin has an integrated SPI port that can connect directly to the SPI pins of the AD5679R.

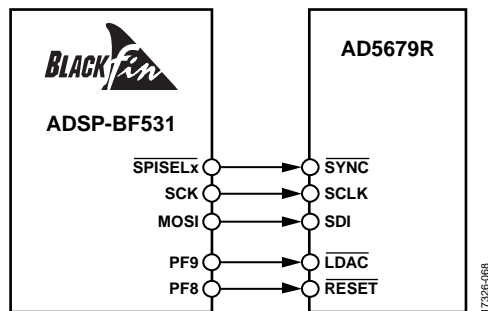


Figure 53. ADSP-BF531 Interface

AD5679R TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT® serial port. Figure 54 shows how a SPORT interface is used to control the AD5679R.

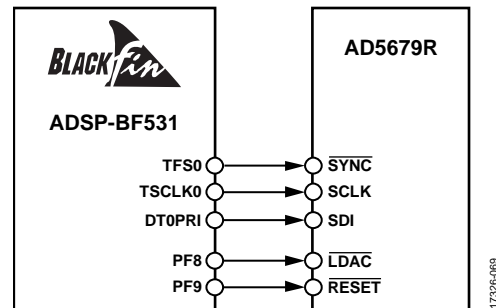


Figure 54. SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5679R is mounted so that the device lies on the analog plane.

The AD5679R must have ample supply bypassing of $10\ \mu\text{F}$ in parallel with $0.1\ \mu\text{F}$ on each supply, located as close to the package as possible, ideally up against the device. The $10\ \mu\text{F}$ capacitors are tantalum bead type. The $0.1\ \mu\text{F}$ capacitors must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The GND plane on the device can be increased (as shown in Figure 55) to provide a natural heat sinking effect.

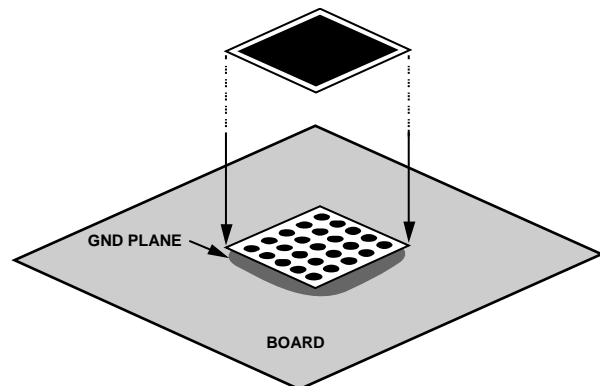
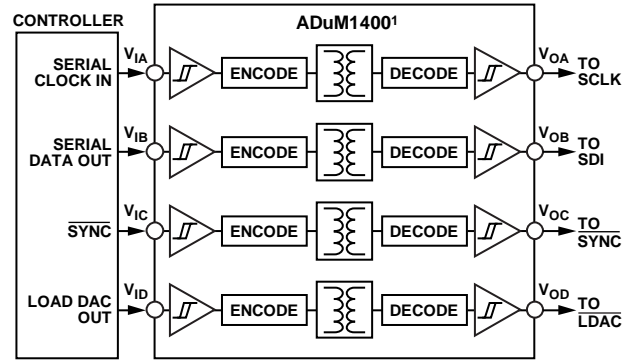


Figure 55. Pad Connection to the Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *iCoupler*® products from Analog Devices may provide voltage isolation greater than 2.5 kV. The serial loading structure of the AD5679R makes the device ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 56 shows a 4-channel isolated interface to the AD5679R using the ADuM1400. For further information, visit www.analog.com/icoupler.

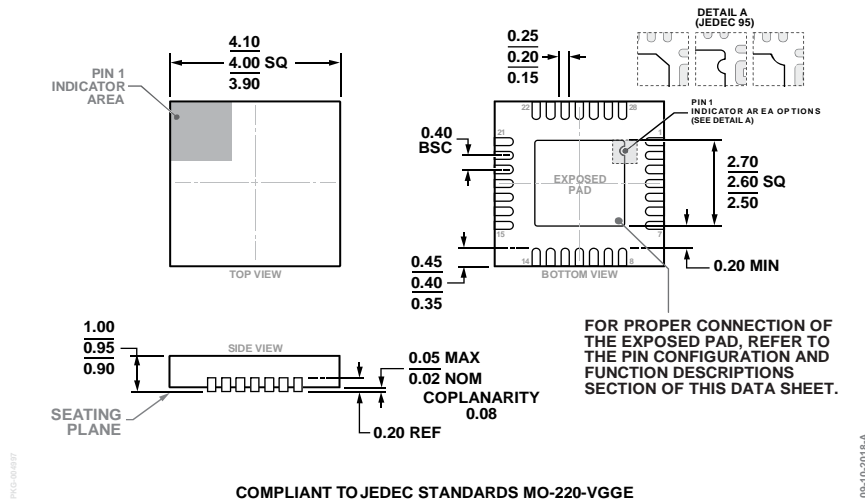


¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 56. Isolated Interface

17526-071

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGE

Figure 57. 28-Lead Lead Frame Chip Scale Package [LFCSPP]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-28-9)

Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1, 2, 3}	Resolution	Temperature Range	Package Description	Package Option
AD5679RBCPZ-1	16 bits	-40°C to +125°C	28-Lead LFCSP	CP-28-9
AD5679RBCPZ-1-RL7	16 bits	-40°C to +125°C	28-Lead LFCSP	CP-28-9
EVAL-AD5679RSDZ			AD5679R Evaluation Board	

¹ Z = RoHS Compliant Part.

² The EVAL-SDP-CB1Z is used in conjunction with the EVAL-AD5679RSDZ.

³ The EVAL-AD5679RSDZ is for the AD5679R DAC.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).