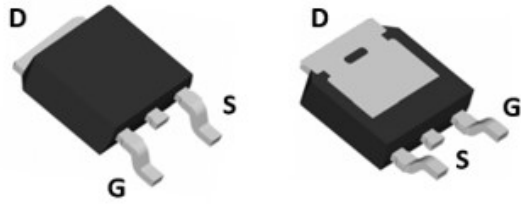
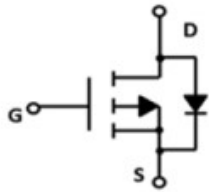


## P-Channel Enhancement Mode Field Effect Transistor



TO-252



### Product Summary

- $V_{DS}$  -30V
- $I_D$  -45A
- $R_{DS(ON)}$ ( at  $V_{GS}=-20V$ ) <7.0mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-10V$ ) <8.0mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ ) <13.0mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	-45
		$T_C=100^\circ\text{C}$	-32
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-175	A
Total Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	75
		$T_C=100^\circ\text{C}$	37
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	145	mJ
Thermal Resistance Junction-to-Case <sup>C</sup>	$R_{\theta JC}$	2.4	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+175	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD45P03A	F1	YJD45P03A	2500	/	25000	13" reel



# YJD45P03A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		-1	μA
			T <sub>J</sub> =55°C		-5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -20V, I <sub>D</sub> =-20A		4.8	7	mΩ
		V <sub>GS</sub> = -10V, I <sub>D</sub> =-15A		5.5	8	
		V <sub>GS</sub> = -6.0V, I <sub>D</sub> =-12A		6.5	12	
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-12A		8	13	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V			-1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-45	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHZ		2152		pF
Output Capacitance	C <sub>oss</sub>			308		
Reverse Transfer Capacitance	C <sub>rss</sub>			242		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-12A		40		nC
Gate-Source Charge	Q <sub>gs</sub>			8.4		
Gate-Drain Charge	Q <sub>gd</sub>			8.6		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-20A, di/dt=-100A/us		7.8		ns
Reverse Recovery Time	t <sub>rr</sub>			18		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-15V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =2.5Ω		8		ns
Turn-on Rise Time	t <sub>r</sub>			19		
Turn-off Delay Time	t <sub>D(off)</sub>			75		
Turn-off fall Time	t <sub>f</sub>			46		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

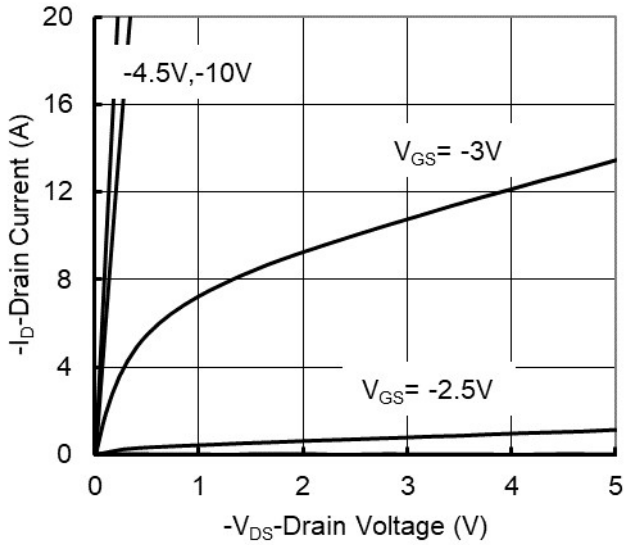


Figure 1. Output Characteristics

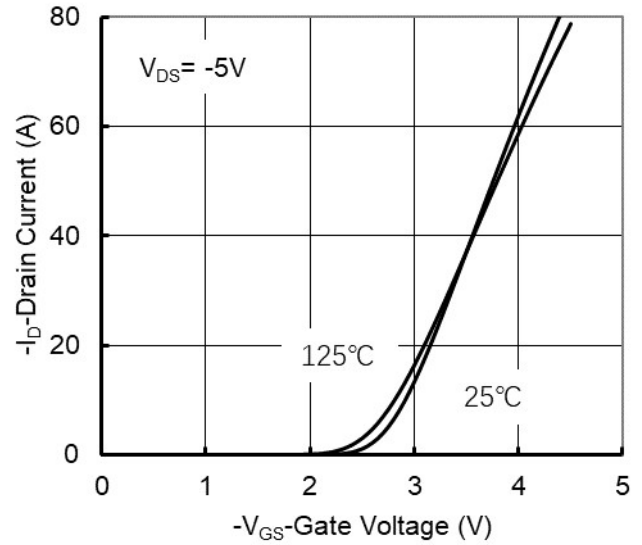


Figure 2. Transfer Characteristics

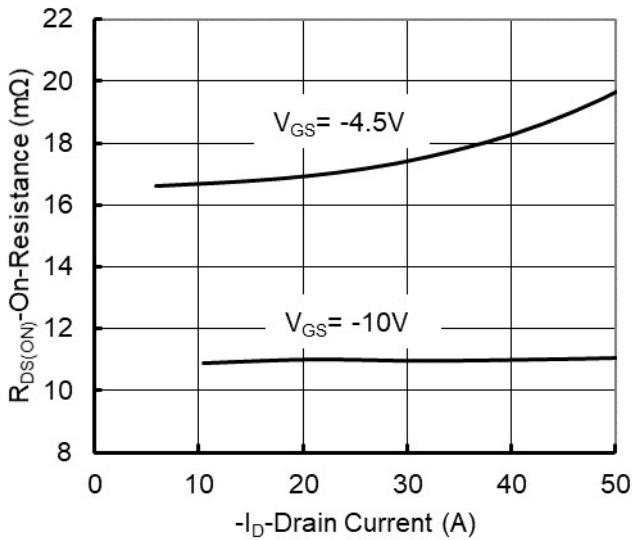


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

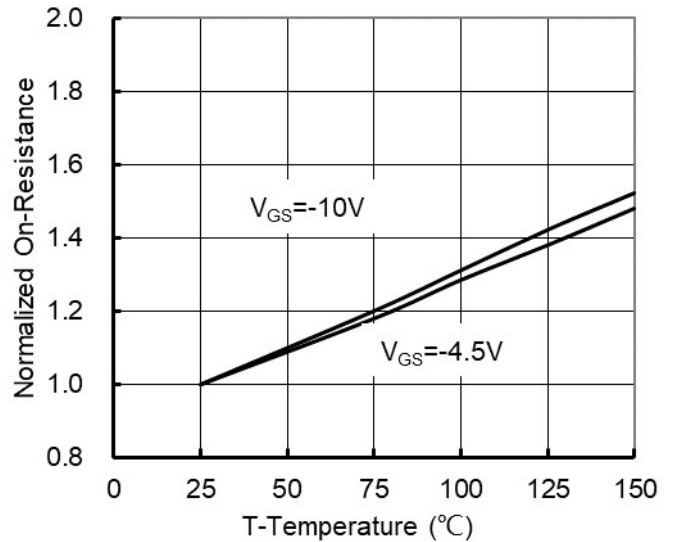


Figure 4. On-Resistance vs. Junction Temperature

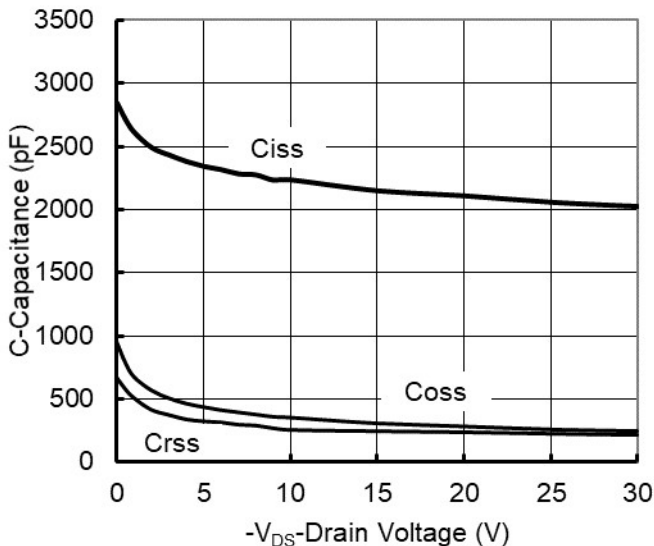


Figure 5. Capacitance Characteristics

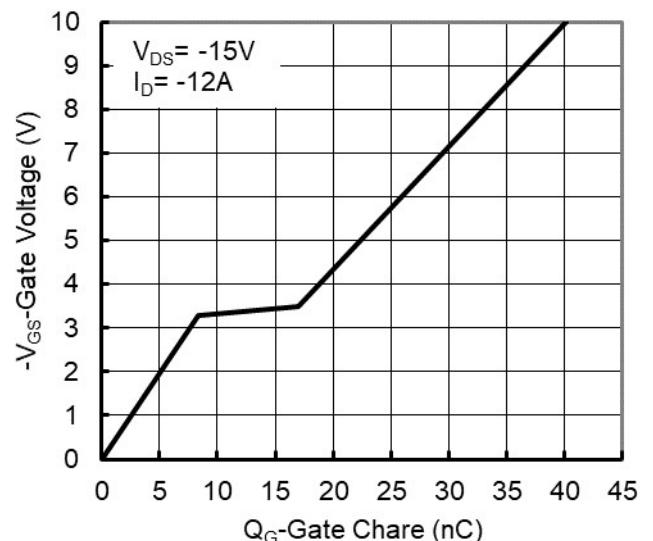


Figure 6. Gate Charge



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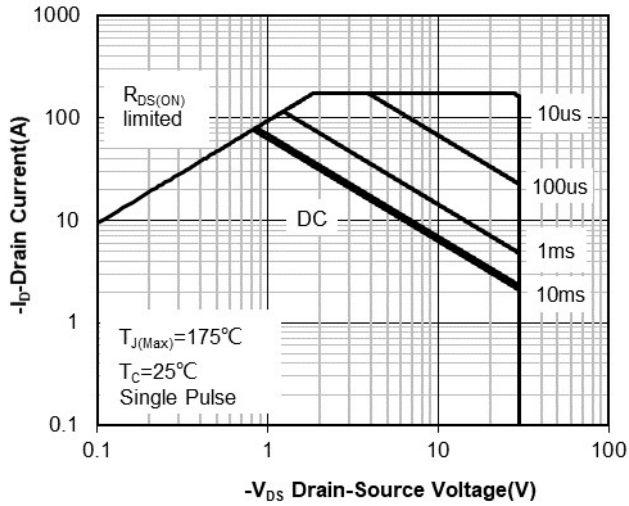


Figure 7. Safe Operation Area

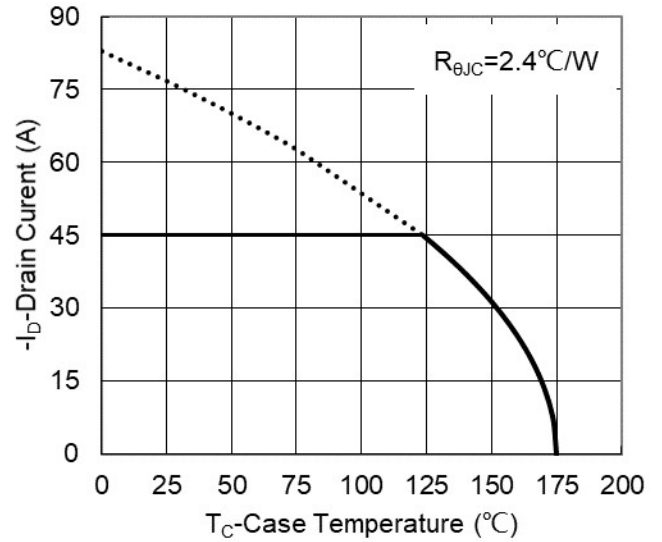


Figure 8. Maximum Continuous Drain Current vs Case Temperature

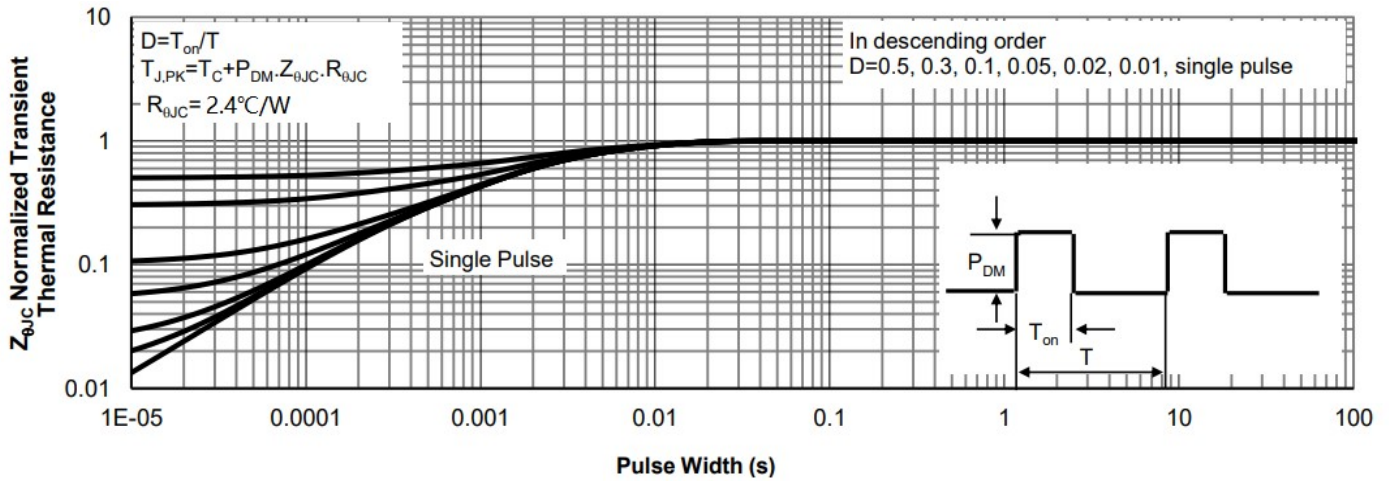


Figure 9. Normalized Maximum Transient Thermal Impedance



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

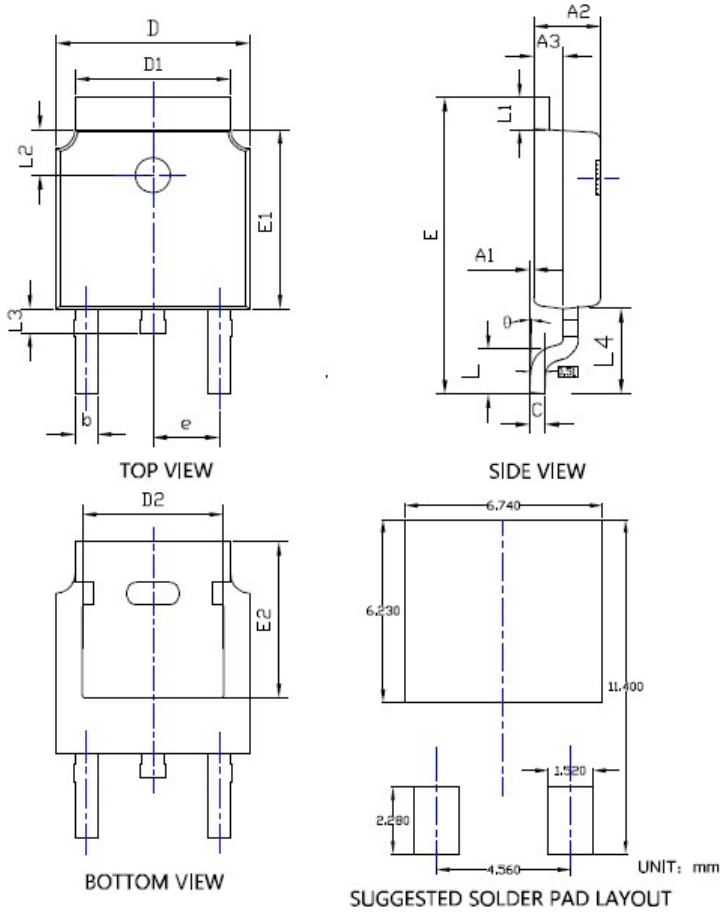


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJD45P03A

## TO-252 Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
e	0°	---	10°	0°	---	10°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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