

WS71441

HD Composite Video Filter Driver with Comparator

Descriptions

The WS71441 is a low power, HD composite video filter and comparator on a single chip. Drawing less than 15mA supply current over the full operating temperature range.

WS71441 integrate high-performance low-cost 54MHz composite video reconstruction filter, it incorporates one high-definition (HD) filter channel. The HD filters can be bypassed to support HDCVI 1080i/720p video.

The WS71441's on-board comparator is high-speed (28ns propagation delay under 2.7~5.5V wide supply range) and low power consumption.

The WS71441 is available in SOP-8L package and MSOP-8L package. Its operation temperature range is from −40°C to +85°C.

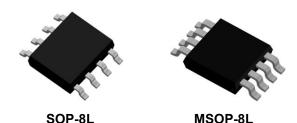
Applications

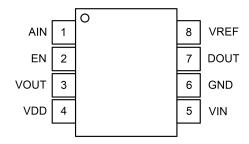
- Video signal amplification
- Set-Top box video driver
- Video buffer for portable or USB-Powered video devices
- HDTV, PV, DVD player video buffer

Features

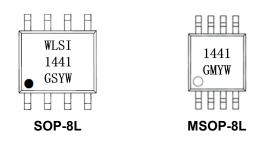
- Wide power supply: +2.7V to +5.5V single supply
- Robust 8kV-HBM and 2kV-CDM ESD rating
- Green product, SOP-8L & MSOP-8L package
- HDTV video filter support Composite 1080p/60
- HD channel: -3dB BW 54MHz
- Provide 80mV level-shift when DC-Coupled
- Very low quiescent current: 12mA (at 3.3V, typical)
- 6dB gain (2V/V), rail to rail output
- AC- or DC-Coupled output driving dual video loads (75Ω)
- Fast response time: 28ns propagation delay
- Offset voltage: ± 3.0mV maximum
- Internal hysteresis ensures clean switching
- Push-Pull, CMOS/TTL compatible output

Http://www.willsemi.com





SOP-8L/MSOP-8L
Pin configuration (Top view)



Marking

1441 = Device code
GS = Special code
GM = Special code
Y = Year code
W = Week code

Order Information

Device	Package	Shipping
WS71441S-8/TR	SOP-8L	4000/Reel &Tape
WS71441M-8/TR	MSOP-8L	4000/Reel &Tape



Pin Descriptions

Pin Number	Symbol	I/O	Descriptions		
1	AIN	1	Input signal pin for comparator		
2	EN	I	The whole chip enable control pin. EN=high, chip work; EN=low, chip shut down		
3	VOUT	0	Video filter output pin		
4	VDD	Power	Power supply (2.7V/5.5V), connect to positive voltage supply		
5	VIN	I	Video signal input pin		
6	GND	Ground	Ground pin, connect to the most negative supply		
7	DOUT	0	Comparator output pin, high voltage level is pulled to VDD low voltage is GND		
8	VREF	I	The DC reference voltage input pin for comparator		

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power Supply, VDD to GND	V_{DD}	6	V
Input Voltage	V _{in}	GND-0.3 ~ VDD+0.3	V
Output Current	Io	150	mA
Maximum Junction Temperature	TJ	150	°C
Operating Temperature Range	T _A	-45 to 85	°C
Storage Temperature Range	T _{STG}	-65 to 150	°C
Lead Temperature (Soldering 10 sec)	T∟	300	°C

Notes:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

- (1) This data was taken with the JEDEC low effective thermal conductivity test board.
- (2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
ПВМ	Human Bady Madal FSD	MIL-STD-883H Method 3015.8	10000	\
HBM	Human Body Model ESD	JEDEC-EIA/JESD22-A114A	±8000	v
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	±2000	V



Electrical Characteristics-Video Filter Part

All test condition is V_{DD} = 3.3V, T_A = +25°C, R_L = 150 Ω to GND, unless otherwise noted.

Paramete	r	Conditions	Min.	Тур.	Max.	Units
Input Electrical Specif	ications					
Supply Voltage Range			2.7		5.5	V
0	lote 1	$V_{DD} = 3.3V$, $V_{IN} = 500$ mV, no load		11.5		mA
Quiescent current (IQ) ^N	iote i	V _{DD} = 5.0V, V _{IN} = 500mV, no load		14.3		mA
Clamp Discharge Curre	nt	V _{IN} =300mV, measure current		1		μA
Clamp Charge Current		V _Y = -0.2V		1		mA
Input Voltage Clamp		I _Y = -100μA		116		mV
Input Impedance		0.5V < V _Y < 1V		36		МΩ
Voltage Cain		V _{IN} =0.5V,1V or 2V		6		٩D
Voltage Gain		R_L =150 Ω to GND		0		dB
Output Level Shift Volta	ge	V _{IN} = 0V, no load, input referred		108		mV
Output Voltage Low Swi	ing	$V_{IN} = -0.3V, R_L = 75\Omega$		0.268		V
Output Valtage Lligh Cu	·i	V_{IN} = 3.3V, R_L =75 Ω to GND		2.05		V
Output Voltage High Sw	ring	(dual load)	2.85			V
Dower Cumply Dejection	Datia	Δ V _{DD} = 3.3V to 3.6V		50		dB
Power Supply Rejection	Rallo	$\Delta V_{DD} = 5.0 V \text{ to } 5.5 V, 50 Hz$		53		dB
Chart singuit augment		V_{IN} = 2V, 10 Ω , output to GND		121		mA
Short-circuit current		V_{IN} =0.1V, output short to V_{DD}		135		mA
Disable Threshold		V _{DD} = 3.0V to 5.5V		0.66		V
Enable Threshold		V _{DD} = 3.0V to 5.5V		1		V
Enable Time		V _{IN} = 500mV, V _{OUT} to 1%		808		ns
Disable Time		V _{IN} = 500mV, V _{OUT} to 1%		147		ns
AC Electrical Specifica	ations					
-1dB Bandwidth	HD Channel	R _L =150Ω		44		MHz
-3dB Bandwidth	HD Channel	R _L =150Ω 54			MHz	
Croup Dolay Variation	UD Charact	f = 100kHz to 27MHz		12.1		ns
Group Delay Variation	HD Channel	f = 100kHz to 54MHz		15.7		ns
Output Impedance		f = 10MHz		0.7		Ω

Note 1:

100% tested at T_A=25°C.



Electrical Characteristics-Comparator Part

All test condition is V_{DD} = 3.3V, T_A = +25°C, V_{IN+} = V_{DD} , V_{IN-} = 1.2V, R_{PU} =10k Ω , C_L =15pF, unless otherwise noted.

Parameter	Conditions	Min.	Тур.	Max.	Units
Supply Voltage		2.7		5.5	V
Input Offset Voltage Note 1	V _{CM} = 1.2V		80		mV
Input Hysteresis Voltage Note 1	V _{CM} = 1.2V		2		mV
Input Bias Current	V _{CM} = 1.2V		10		pА
Input Offset Current			10		pА
Input Resistance		1		GΩ	
Common-mode Input Voltage Range		V _{DD} -0.1		V _{SS} +0.1	V
High-Level Output Voltage	I _{OUT} =1mA		3.22		V
Low-Level Output Voltage	I _{OUT} =-1mA		0.04		V
Output Short-Circuit Current	Sink or source current		27		mA
Rising Time			3.5		ns
Falling Time			4		ns
Propagation Delay (Low-to-High)	Overdrive=100mV, V _{IN-} =1.2V		28		ns
Propagation Delay (High-to-Low)	Overdrive=100mV, V _{IN-} =1.2V		14		ns
Propagation Delay Skew	Overdrive=100mV, V _{IN-} =1.2V		4		ns

Note 1:

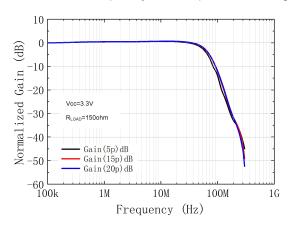
The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.



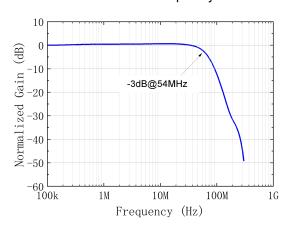
Typical Characteristics-Video Filter Part

All test condition is V_{DD} = 3.3V, T_A = +25°C, R_L = 150 Ω to GND, unless otherwise noted.

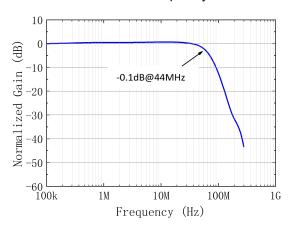
Gain Vs. Frequency With Capacitor Loading



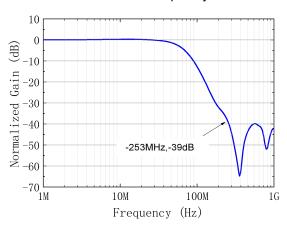
Gain Vs. Frequency



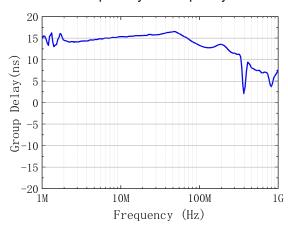
Gain Vs. Frequency



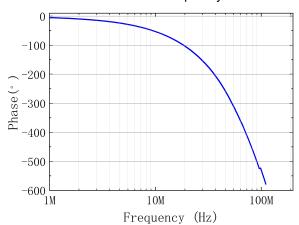
Gain Vs. Frequency



Group Delay vs Frequency



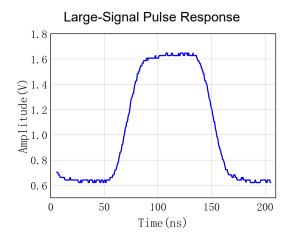
Phase Vs. Frequency

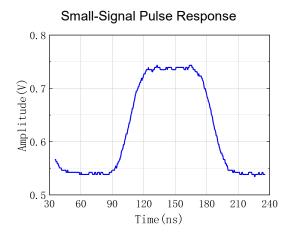




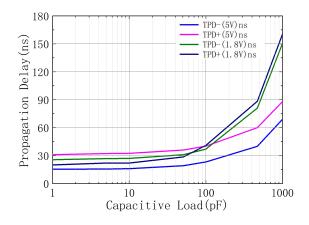
Typical Characteristics-Comparator Part

 T_A =25°C, I_Q =22mA, G_{DIFF} =5V/V, R_F =750 Ω , and R_L Diff=100 Ω , unless otherwise noted.

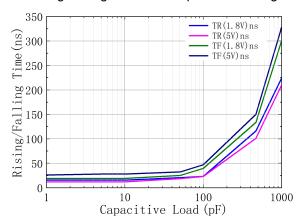




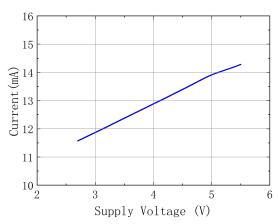
Propagation Delay V.S. Capacitor Loading



Rising/Falling Time V.S. Capacitor Loading



Current Vs. Supply Voltage





Application Information

The WS71441 is targeted for systems that require 1 channel high-definition (HD) video outputs. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the WS71441. The WS71441 incorporates many features not typically found in integrated video parts while consuming very low power.

Internal Sync Clamp

The typical embedded video DAC operates from a ground referenced single supply. This becomes an issue because the lower level of the sync pulse output may be at a 0V reference level to some positive level. The problem is presenting a 0V input to most single supply driven amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degrading the video image. A larger positive reference may offset the input above its positive range.

The WS71441 features an internal sync clamp and offset function to level shift the entire video signal to the best level before it reaches the input of the amplifier stage. These features are also helpful to avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The AC coupled video sync signal is pulled negative by a current source at the input of the comparator amplifier. When the sync tip goes below the comparator threshold the output comparator is driven negative, The PMOS device turns on clamping sync tip to near ground level. The network triggers on the sync tip of video signal.

Droop Voltage and DC Restoration

Selection of the input AC-coupling capacitance is based on the system requirements. A typical sync tip width of a $64\mu s$ NTSC line is $4\mu s$ during which clamp circuit restores its DC level. In the remaining $60\mu s$ period, the voltage droops because of a small constant $2.0\mu A$ sinking current. If the AC-coupling capacitance is $0.1\mu F$, the maximum droop voltage is about 1mV which is restored by the clamp circuit. The maximum pull-up current of the clamp circuit is 1.7mA. For a $4\mu s$ sync tip width and $0.1\mu F$ capacitor, the maximum restoration voltage is about 110mV.

The line droop voltage will increase if a smaller AC-coupling capacitance is used. For the same reason, if larger capacitance is used the line droop voltage will decrease. Table 1 is droop voltage and maximum restoration voltage of the clamp for typical capacitance.

CAP VALUE(nF)	DROOP IN 60µs(mV)	CHARGE IN 4µs(mV)
100	1.2	68
1000	0.12	6.8

Table 1. Maximum restoration voltage and droop voltage of Y signals for different capacitance

Low Pass Filter--Sallen Key

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the WS71441, the six-pole roll-off at around 54MHz. The six-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key.

Output Couple

WS71441 output could support both "AC Couple" and "DC Couple", if use "AC Couple", this capacitor is



typically between $220\mu F$ and $1000\mu F$, although $470\mu F$ is common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document.

The WS71441 internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, thereby saving board space and additional expense for capacitors. This makes the WS71441 extremely attractive for portable video applications. Additionally, this solution completely eliminates the issue of field tilt in the lower frequency. The trade off is greater demand of supply current. Typical load current for AC coupled is around 1mA, compared to typical 11.5mA used when DC coupling.

Output Drive Capability and Power Dissipation

With the high output drive capability of the WS71441, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area. The maximum power dissipation allowed in a package is determined according to Equation:

$$PD_{MAX} = (T_{JMAX--}T_{AMAX}) / \theta_{JA}$$

Where:

 T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

 θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or: for sourcing:

$$PD_{MAX}=V_S \times I_{SMAX}+(V_S-V_{OUT}) \times V_{OUT}/R_L$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

By setting the two PDMAX equations equal to each other, we can solve the output current and RLOAD to avoid the device overheat.

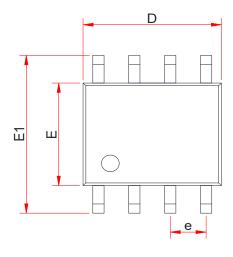
Power Supply Bypassing Printed Circuit Board Layout

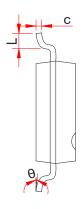
As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single $4.7\mu F$ tantalum capacitor in parallel with a $0.1\mu F$ ceramic capacitor from VS+ to GND will suffice.



PACKAGE OUTLINE DIMENSIONS

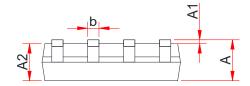
SOP-8L





TOP VIEW

SIDE VIEW



SIDE VIEW

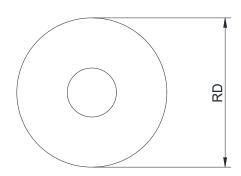
Symbol	Dime	Dimensions In Millimeters (mm)				
Symbol	Min.	Тур.	Max.			
А	1.35	1.55	1.75			
A1	0.05	0.15	0.25			
A2	1.25	1.40	1.65			
b	0.33	-	0.51			
С	0.15	-	0.26			
D	4.70	4.90	5.10			
E	3.70	3.90	4.10			
E1	5.80	6.00	6.20			
е		1.27BSC				
L	0.40	-	1.27			
θ	0°	-	8°			



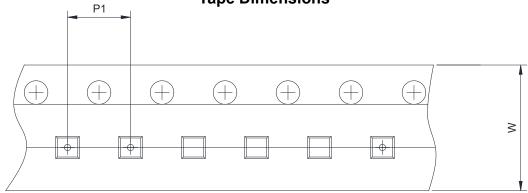
TAPE AND REEL INFORMATION

SOP-8L

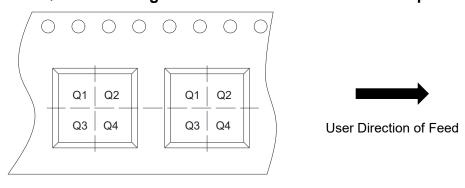
Reel Dimensions



Tape Dimensions



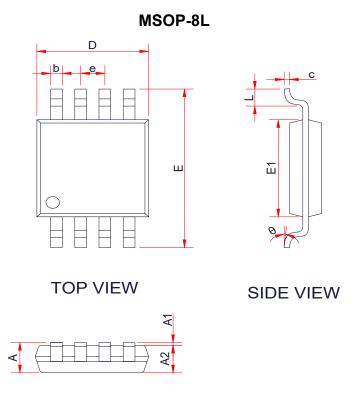
Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	7inch	✓ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm		
P1	Pitch between successive cavity centers	2mm	4mm	▼ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	□ Q2	□ Q3	□ Q4



PACKAGE OUTLINE DIMENSIONS



SIDE VIEW

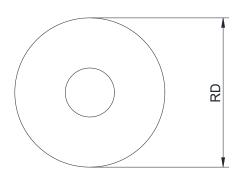
Symbol	Dimensions In Millimeters (mm)					
	Min.	Тур.	Max.			
А	-	-	1.10			
A1	0.02	-	0.15			
A2	0.75	0.80	0.95			
b	0.25	-	0.38			
С	0.09	-	0.23			
D	2.90	3.00	3.10			
E	4.75	4.90	5.05			
E1	2.90	3.00	3.10			
е	0.65 BSC					
L	0.40	-	0.80			
θ	0°	0° - 6°				



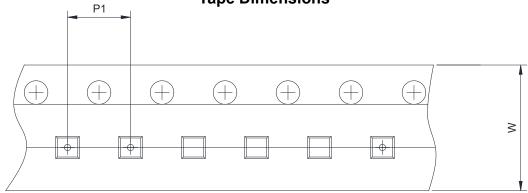
TAPE AND REEL INFORMATION

MSOP-8L

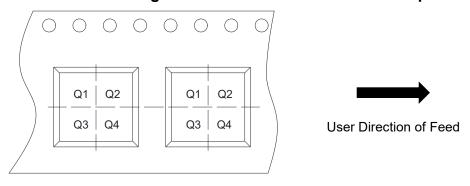
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	7inch	✓ 13inch		
W	Overall width of the carrier tape	□ 8mm	▼ 12mm		
P1	Pitch between successive cavity centers	2mm	4mm	▼ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	□ Q2	□ Q3	□ Q4