REASUNOS

N Channel MOSFET

Applications:

- Uninterruptible Power Supply(UPS)
- Power Factor Correction(PFC)
- •SMPS Power
- •DC-AC Inverter

Features:

- Low On Resistance
- ·Fast switching
- •Improved dv/dt capability
- •RoHS Compliant

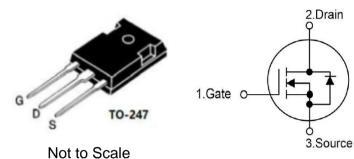
Ordering Information:

Part Number	Package	Marking
RS25N50W	TO-247	RS25N50W

PR

Lead Free Package and Finish

ΙD	RDS(ON)(Typ.)	VDSS
25A	0.13Ω	500V



Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS25N50W	Units
VDSS	Drain-to-Source Voltage (Note*1)	500	V
ID	Continuous Drain Current	25	A
ldм	Pulsed Drain Current (Note*2)	100	A
PD	Power Dissipation	230	W
VGS	Gate-to-Source Voltage	±30	V
EAS	Single Pulse Avalanche Engergy L=10mH	2500	mJ
	Maximum Temperature for Soldering		
TL TPKG	Leads at 0.063in(1.6mm)from Case for 10 seconds	300 260	*0
	Package Body for 10 seconds		${\mathbb C}$
TJ and TSTG	Operating Junction and Storage	-55 to 150	
	Temperature Range	33.13.100	

^{*}Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS25N50W	Units	Test Conditions
RθJC	Junction-to-Case	0.29	°C/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	62		1 cubic foot chamber,free air.

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OFF Characteristics $TJ=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
BVDSS	Drain-to-source Breakdown Voltage	500			V	Vgs=0V,ID=250µA
IDSS	Drain-to-Source Leakage Current			1.0	μΑ	VDS=500V,VGS=0V
Igss	Gate-to-Source Forward Leakage			100	۸	VGS=+30V VDS=0V
1655	Gate-to-Source Reverse Leakage			-100	μΑ	Vgs=-30V Vds=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
RDS(on)	Static Drain-to-Source On-Resistance (Note*3)		0.13	0.18	Ω	V _{GS} =10V,I _D =12.5A
Vgs(TH)	Gate Threshold Voltage	3.0		4.0	V	$Vgs=Vds,Id=250\mu A$

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
td(ON)	Turn-on Delay Time		66			V _{DS} =250V
trise	Rise Time		59		nc	I _D =25A
td(OFF)	Turn-OFF Delay Time		427		ns	$R_G = 25\Omega$
tfall	Fall Time		108			(Note:3,4)

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Ciss	Input Capacitance		4295			Vgs=0V
Coss	Output Capacitance		450		pF	Vps=25V
Crss	Reverse Transfer Capacitance		32			f=1.0MHz
Qg	Total Gate Charge		22			V _{DS} =250V
Qgs	Gate-to-Source Charge		4		nC	I _D =25A
Qgd	Gate-to-Drain("Miller") Charge		13			V _{GS} =10V (Note:3,4)

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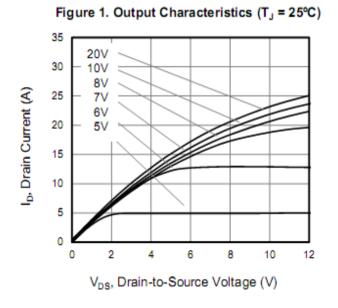
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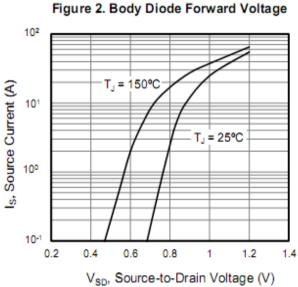
Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Тур.	Max.	Units	Test Conditions
Is	Continuous Source Current			25	Α	Integral pn-diode
Ism	Maximum Pulsed Current			100	Α	in MOSFET
Vsd	Diode Forward Voltage			1.4	V	$I_S=25A, V_{GS}=0V$
trr	Reverse Recovery Time		482		nS	V _{GS} =0V
Qrr	Reverse Recovery Charge		7.6		μC	I _S =25A,di/dt=100A/μs

Notes:

Typical Feature curve (TJ = 25°C, unless otherwise noted)





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^{*1.}TJ=±25°C to +150°C.

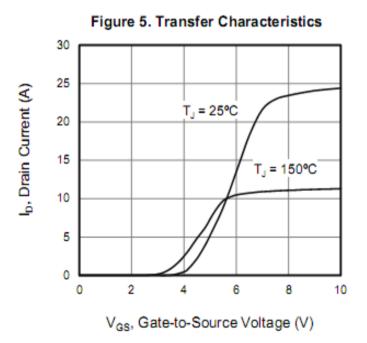
^{*2.}Repetitive rating; pulse width limited by maximum junction temperature.

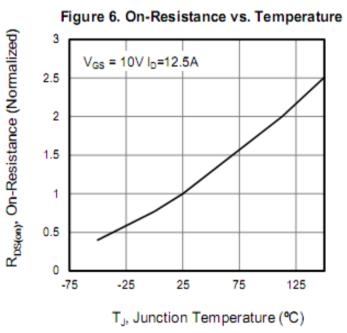
^{*3.}Pulse width≤300µs;duty cycle ≤1%.

Figure 3. Drain Current vs. Temperature

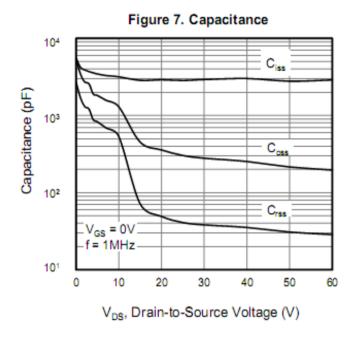
30
25
20
15
10
5
0
30
60
90
120
150
T_C, Case Temperature (A)

Figure 4. BV_{DSS} Variation vs. Temperature V_{GS} = 0V I_D=250uA 1.15 BV_{DSS} (Normalized) 1.1 1.05 0.95 0.9 -50 -25 50 75 100 125 150 T_C, Case Temperature (°C)





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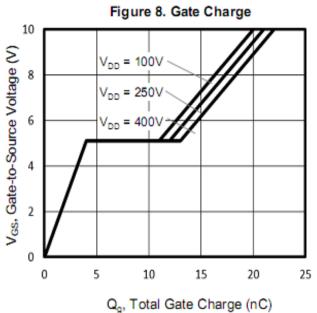
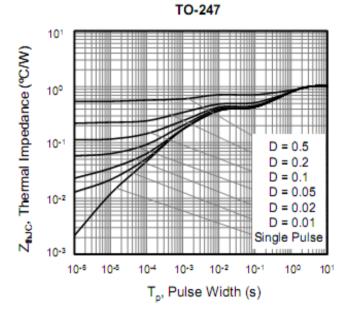


Figure 9. Transient Thermal Impedance



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Test Circuits and Waveforms

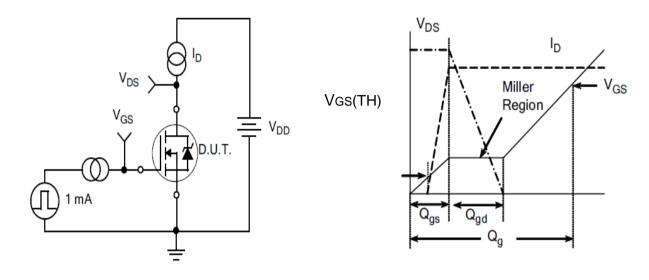


Figure 10.
Gate Charge Test Circuit

Figure 11.
Gate Charge Waveform

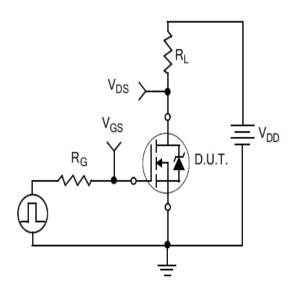


Figure 12.
Resistive Switching Test Circuit

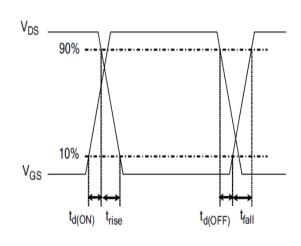


Figure 13.
Resistive Switching Waveforms

RS25N50W

Test Circuits and Waveforms

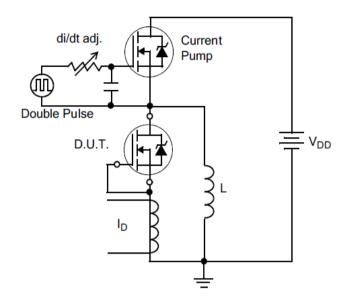


Figure14.Diode Reverse Recovery
Test Circuit

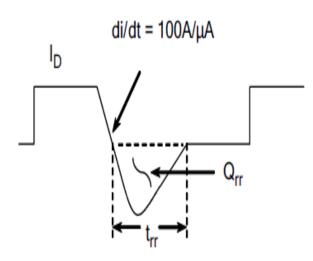


Figure 15. Diode Reverse Recovery Waveform

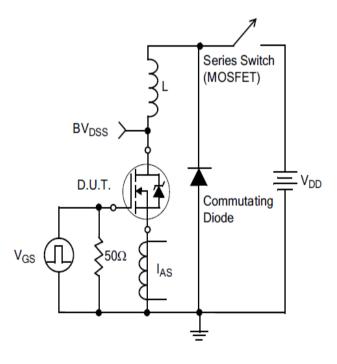
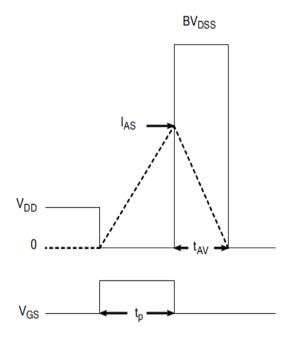


Figure 16. Unclamped Inductive Switching Test Circuit



$$EAS = \frac{IAS^2L}{2}$$

Figure 17. Unclamped Inductive Switching Waveforms

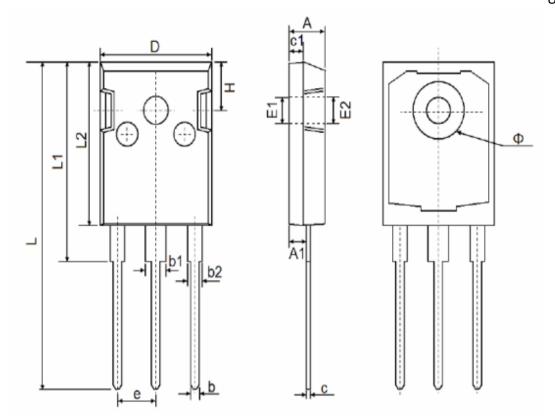
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Package outline drawing

Unit:mm



TO-247

O. mah ad	Dimensions	In Millimeters	Dimensions	In Inches
Symbol	Min.	Max.	Min.	Max.
Α	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
С	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 F	REF
E2	3.600 REF		0.142 F	REF
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
е	5.45	0 TYP	0.215 1	ГҮР
Н	5.98	0 REF	0.235 F	REF

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