N Channel MOSFET

Lead Free Package and Finish

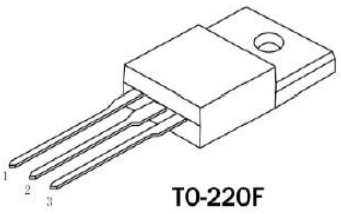
Applications:

•Adapter & Charger
•DC-AC inverter Power
•AC-DC Switching Power Supply
•LED driving power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
20A	0.2Ω	500V

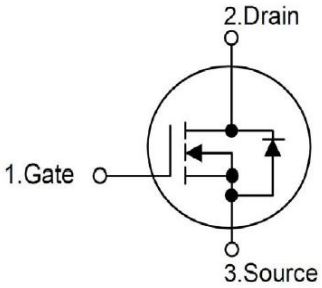
Features:

•Low On Resistance
•Low Gate Charge
•Peak Current vs Pulse Width Curve
•RoHS Compliant



TO-220F

Not to Scale



Ordering Information

Part Number	Package	Marking
RS20N50F	TO-220F	RS20N50F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS20N50F	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	500	V
I_D	Continuous Drain Current	20.0	A
I_D@ 100 ℃	Continuous Drain Current	12.6	
I_{DM}	Pulsed Drain Current (Note*2)	80.0	
P_D	Power Dissipation	190	W
	Derating Factor above 25℃	1.52	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy L=6mH I_{AS}=20A V_{DD}=50V R_G=25Ω T_J=25℃	1200	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_{PKG}	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS20N50F	Units	Test Conditions
RθJC	Junction-to-Case	0.7	℃/W	Drain lead soldered to water cooled heatsink,PD adjusted for a peak junction temperature of +150℃.
RθJA	Junction-to-Ambient	53.5		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	500	--	--	V	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=500V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	μA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	--	0.2	0.3	Ω	V_{GS}=10V,I_D=10A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	54	--	nS	V_{DS}=250V I_D=10A R_G=10Ω (Note:3,4)
t_{rise}	Rise Time	--	165	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	98	--		
t_{fall}	Fall Time	--	86	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2302	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	360	--		
C_{rss}	Reverse Transfer Capacitance	--	28	--		
Q_g	Total Gate Charge	--	51	--	nC	V_{DS}=400V I_D=20A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	12.7	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	22	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	20	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	80	A	
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=20A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	570.3	--	nS	V_{GS}=0V I_S=20A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	7.35	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤2%.
*4.Basically not affected by temperature.

Typical Feature curve

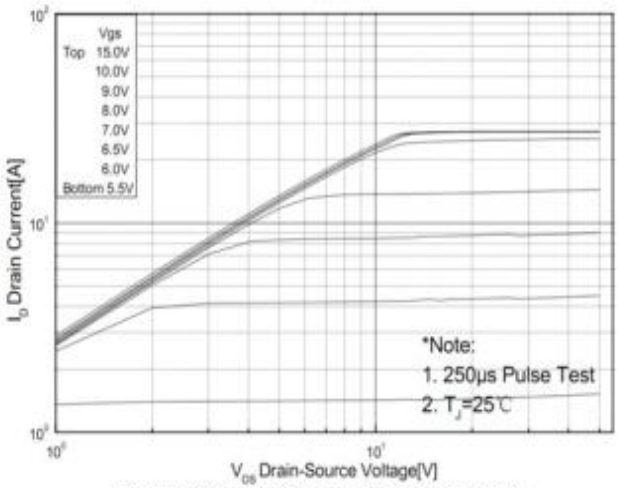


Figure 1. Typical Output Characteristics

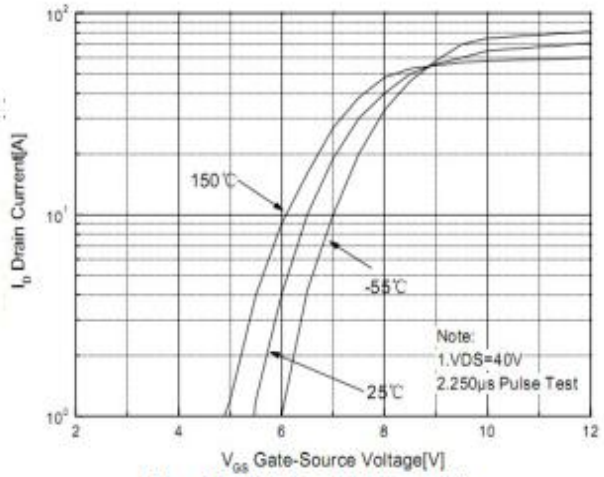


Figure2.Typical Transfer Characteristics

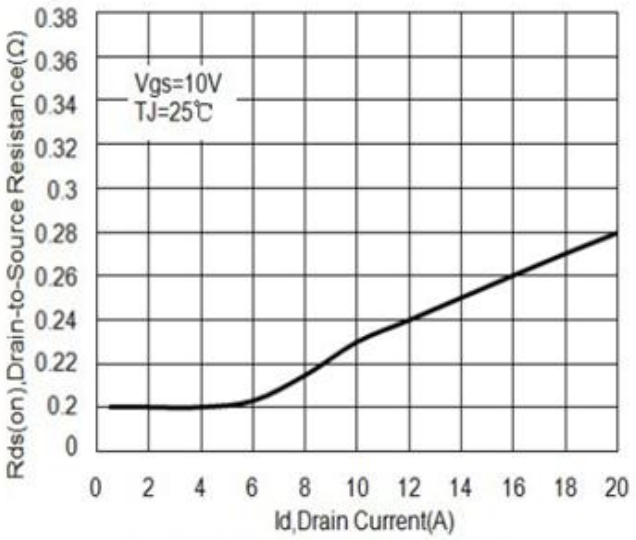


Figure 3.On-Resistance versus Drain Current

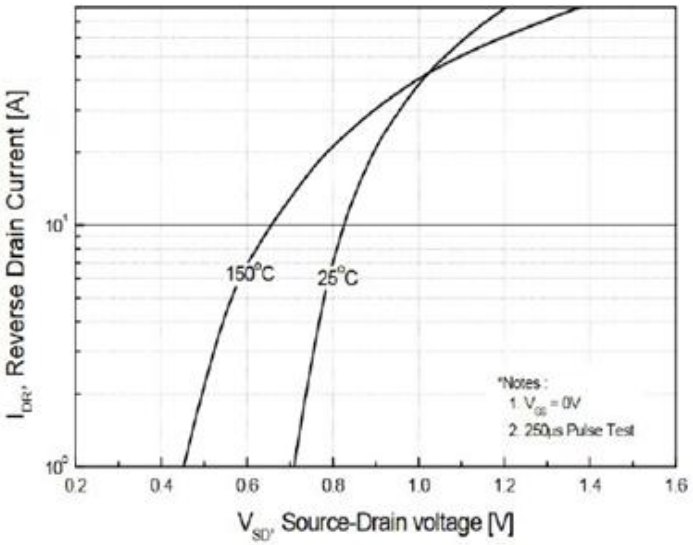


Figure 4.Diode Forward Voltage versus Current

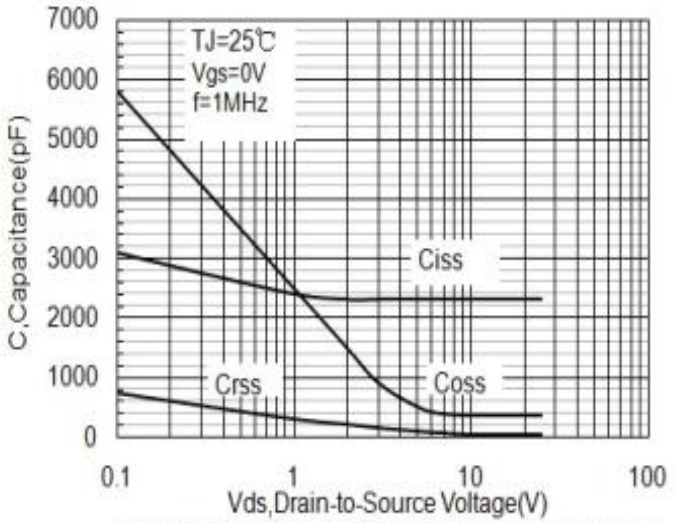


Figure 5.Typical Capacitance vs.Drian-to-Source Voltage

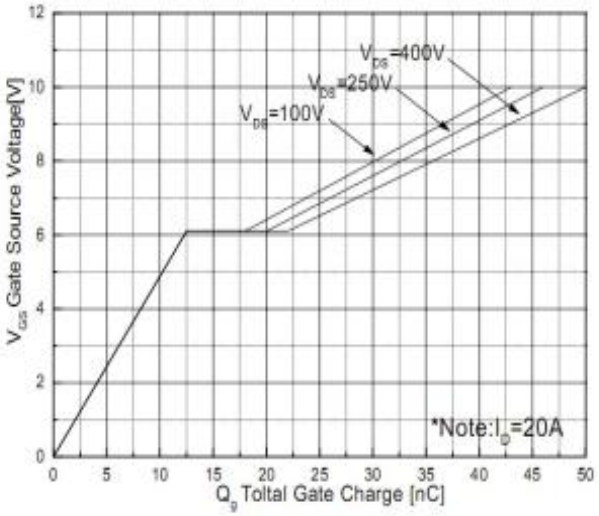


Figure 6.Typical Gate Charge vs.Vgs

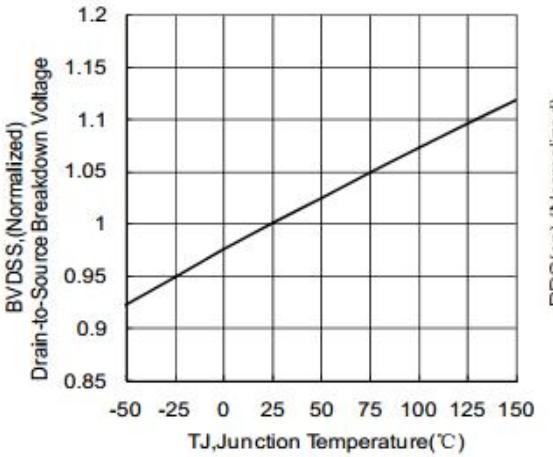


Figure 7.Bvdss Variation with Temperature

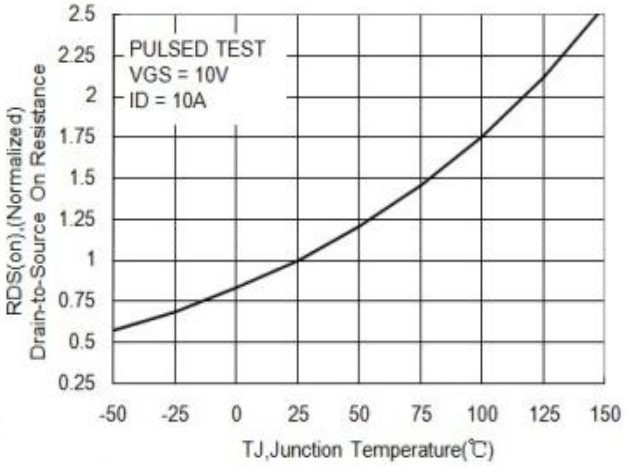


Figure 8.On-Resistance Variation with Temperature

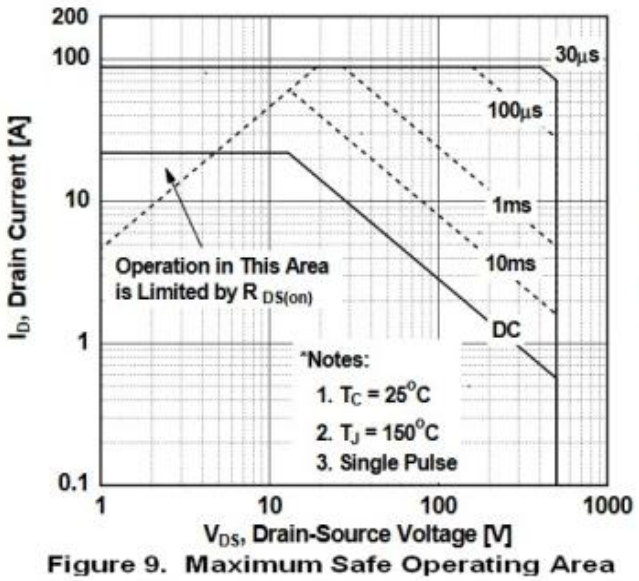


Figure 9. Maximum Safe Operating Area

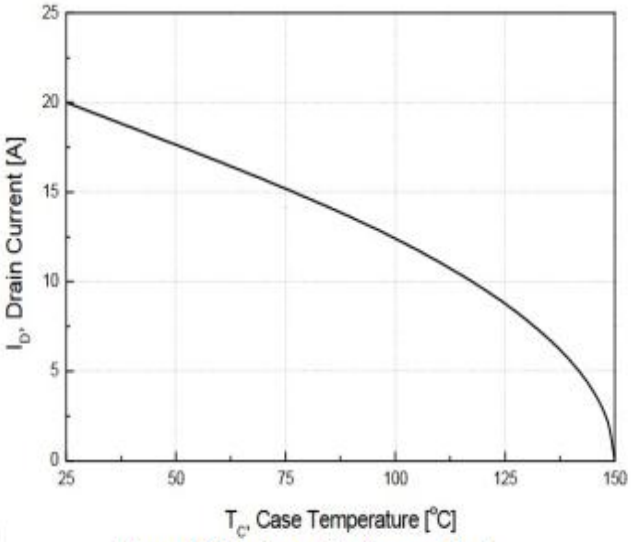


Figure 10. Maximum Continuous Drain Current vs Case Temperature

Test Circuits and Waveforms

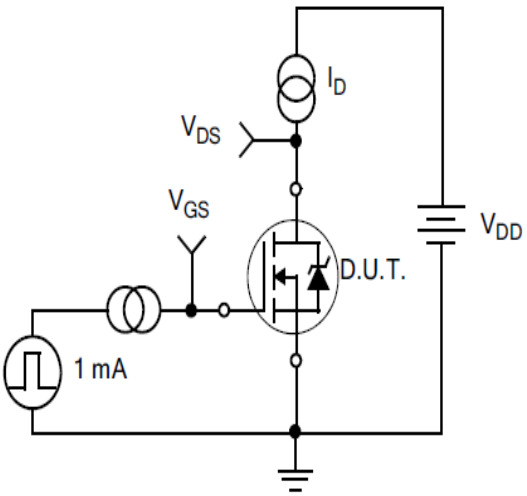


Figure11.
Gate Charge Test Circuit

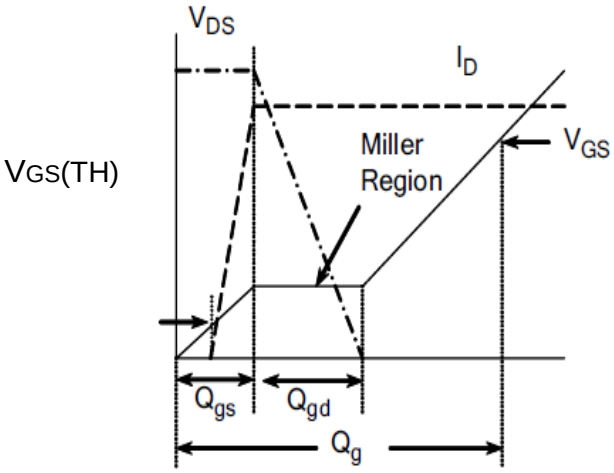


Figure12.
Gate Charge Waveform

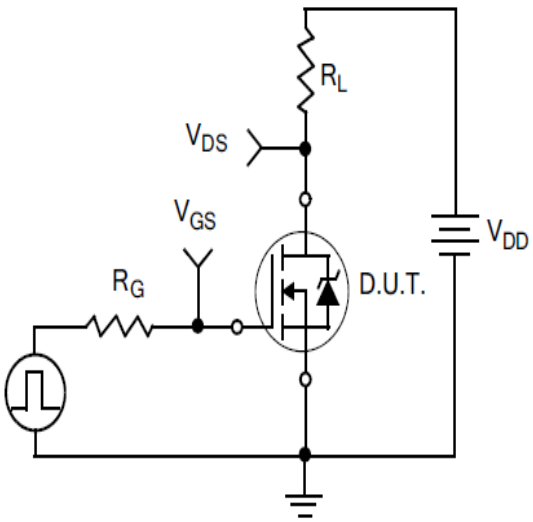


Figure13.
Resistive Switching Test Circuit

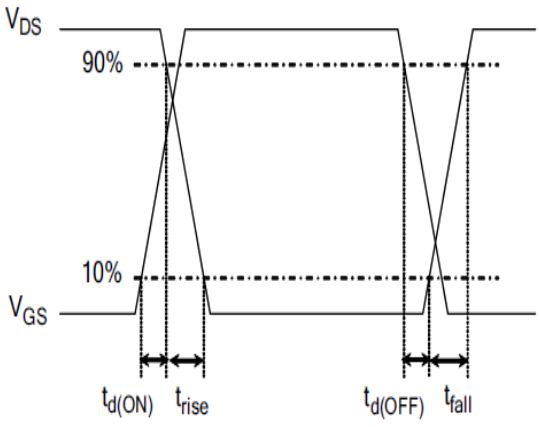


Figure14.
Resistive Switching Waveforms

Test Circuits and Waveforms

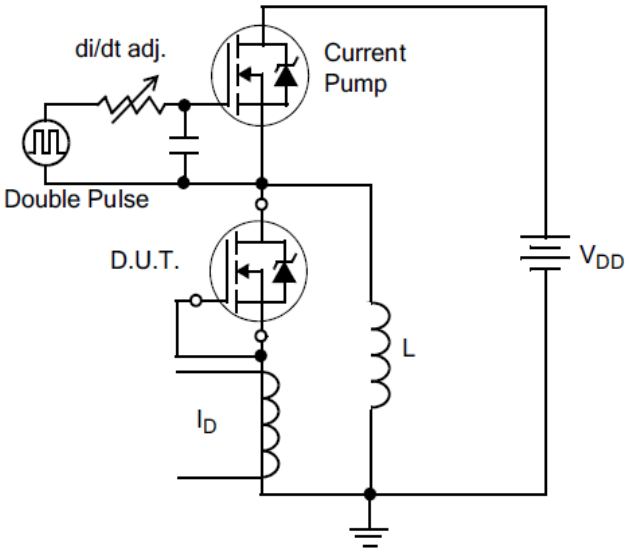


Figure15.Diode Reverse Recovery Test Circuit

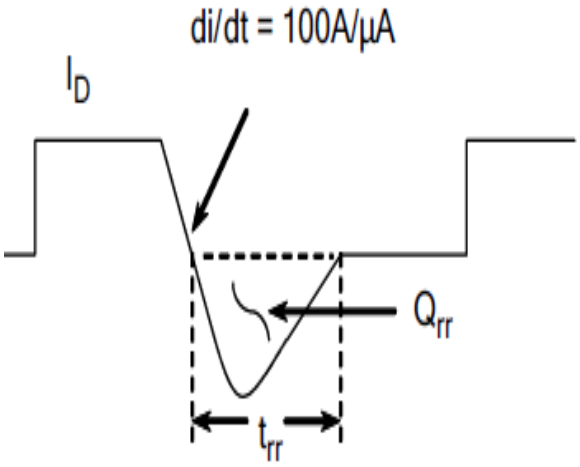


Figure16.Diode Reverse Recovery Waveform

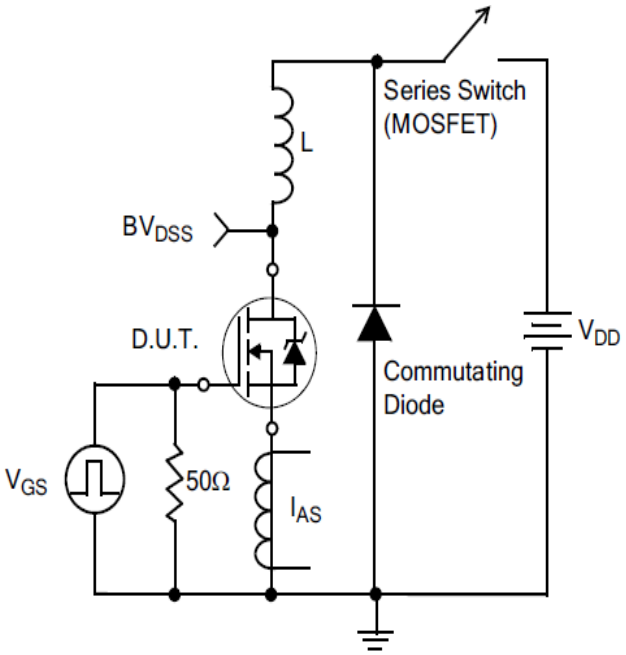
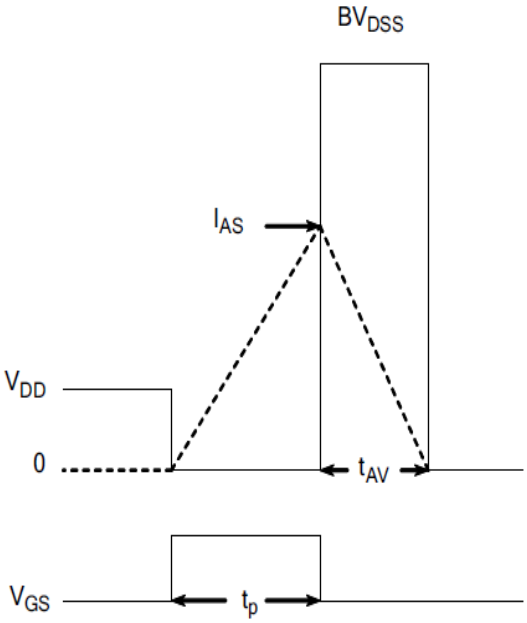


Figure17.Unclamped Inductive Switching Test Circuit

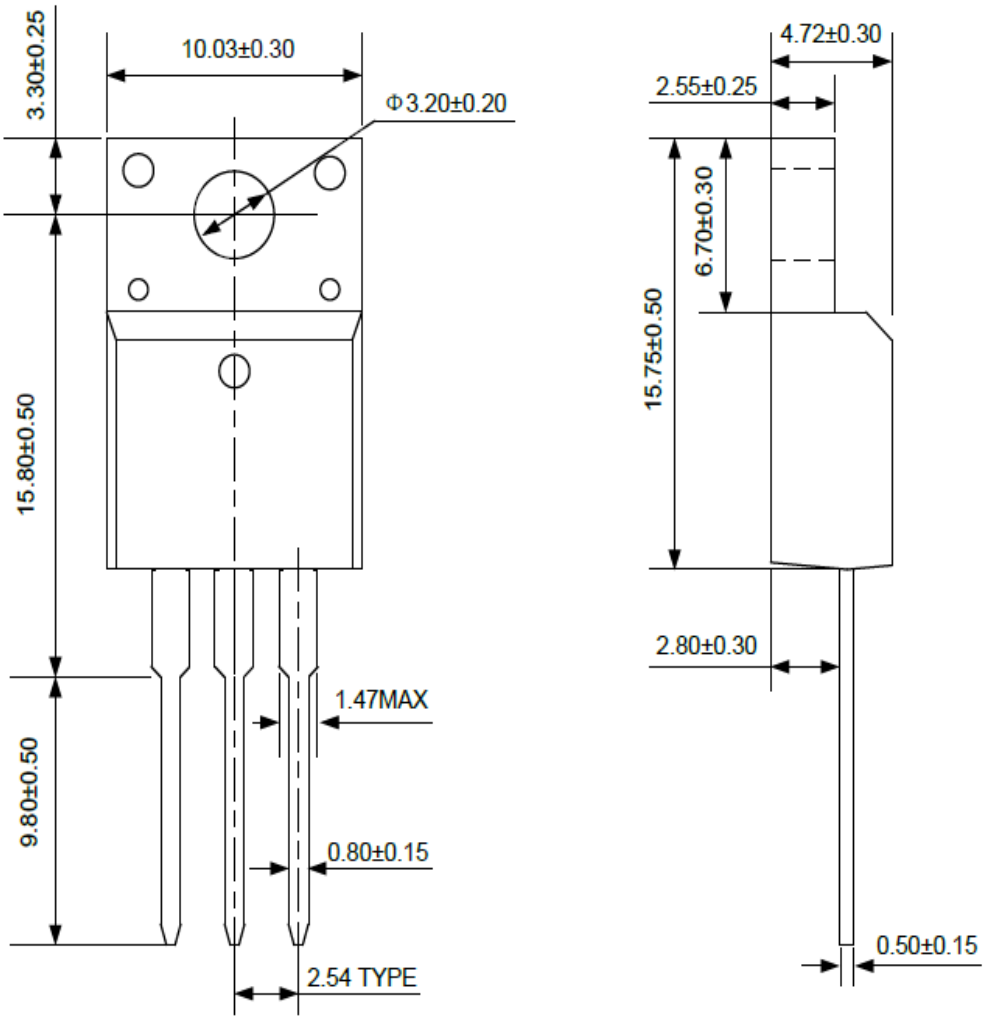


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure18.Unclamped Inductive Switching Waveforms

Package outline drawing

Unit:mm



TO-220F

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