REASUNOS

RS12N65F,RS12N65T

650V N-Channel MOSFET

Pb Lead Free Package and Finish

FEATURES

- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
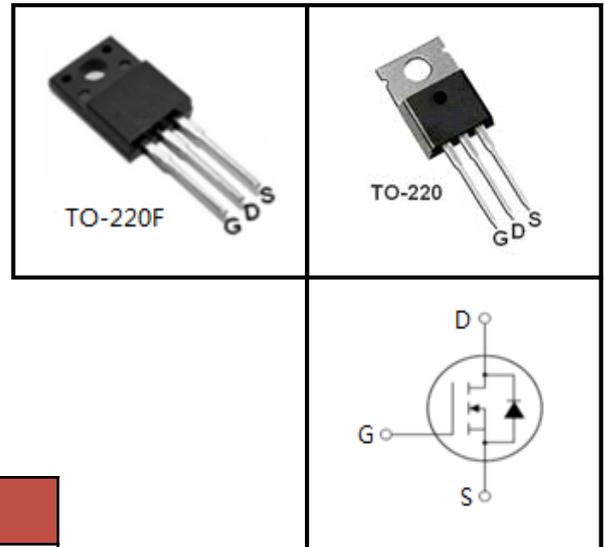
Device Marking and Package Information		
Device	**Package**	**Marking**
RS12N65F	TO-220F	RS12N65F
RS12N65T	TO-220	RS12N65T

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter		Symbol	Value		Unit
			TO-220F	**TO-220**	
Drain-Source Voltage (V_{GS} = 0V)		V_{DSS}	650		V
Continuous Drain Current		I_D	12		A
Pulsed Drain Current	(note1)	I_{DM}	48		A
Gate-Source Voltage		V_{GSS}	± 30		V
Single Pulse Avalanche Energy	(note2)	E_{AS}	810		mJ
Avalanche Current	(note1)	I_{AR}	13.0		A
Repetitive Avalanche Energy	(note1)	E_{AR}	228		mJ
Power Dissipation (T_C = 25ºC)		P_D	70	96	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~+150		ºC

Thermal Resistance

Parameter	Symbol	Value		Unit
		TO-220F	**TO-220**	
Thermal Resistance, Junction-to-Case	R_{thJC}	1.92	1.29	K/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62.5	60	

Specifications $T_J = 25^oC$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^oC$	--	--	1	µA
		$V_{DS} = 520V, V_{GS} = 0V, T_J = 25^oC$	--	--	100	µA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm30V$	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	3.0	--	4.0	V
Drain-Source On-Resistance (Note3)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6.0A$	--	0.45	0.68	Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$	--	1641	--	pF
Output Capacitance	C_{oss}		--	162	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Total Gate Charge	Q_g	$V_{DD} = 520V, I_D = 12A,$ $V_{GS} = 10V$	--	51	--	nC
Gate-Source Charge	Q_{gs}		--	7.1	--	
Gate-Drain Charge	Q_{gd}		--	24.5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 325V, I_D = 12A,$ $R_G = 25 \ \Omega$	--	47	--	ns
Turn-on Rise Time	t_r		--	32	--	
Turn-off Delay Time	$t_{d(off)}$		--	219	--	
Turn-off Fall Time	t_f		--	58	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25 \ ^oC$	--	--	12	A
Pulsed Diode Forward Current	I_{SM}		--	--	48	
Body Diode Voltage	V_{SD}	$T_J = 25^oC, I_{SD} = 6A, V_{GS} = 0V$	--	--	1.4	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0V, I_S = 12A,$ $di_F/dt = 100A /\mu s$	--	579	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.9	--	µC

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $L = 10.0mH, V_{DD} = 50V, R_G = 25 \ \Omega,$ Starting $T_J = 25 \ ^oC$

3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 1%

REASUNOS

Typical Characteristics $T_J = 25°C$, unless otherwise noted

Figure 1. Output Characteristics ($T_J = 25°C$)
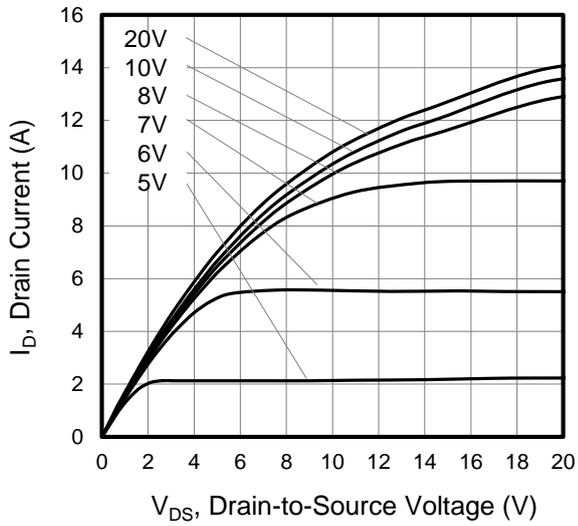
Figure 2. Body Diode Forward Voltage
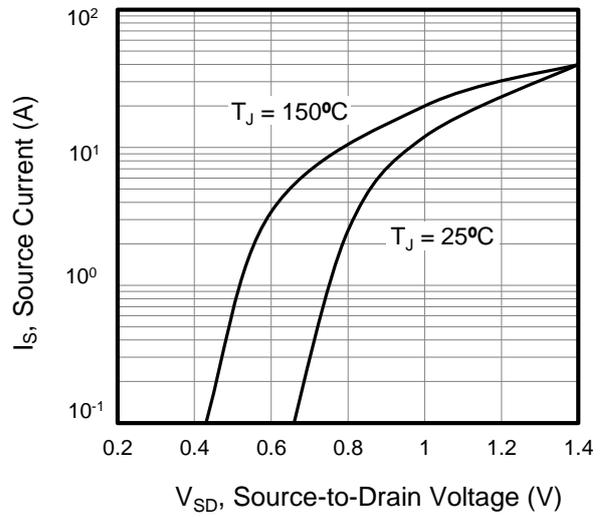
Figure 3. Drain Current vs. Temperature
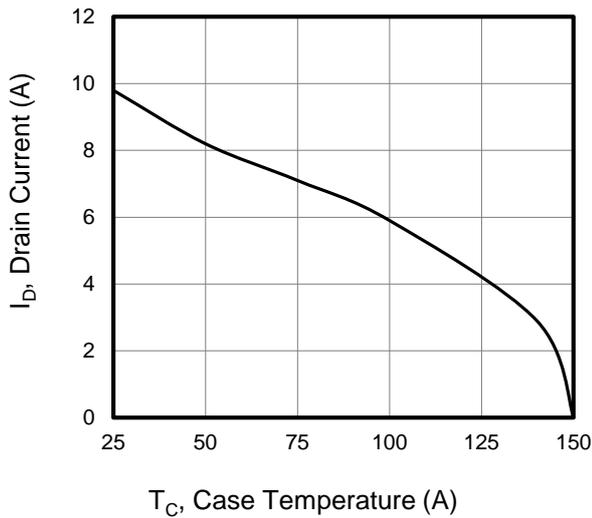
Figure 4. BV_{DSS} Variation vs. Temperature
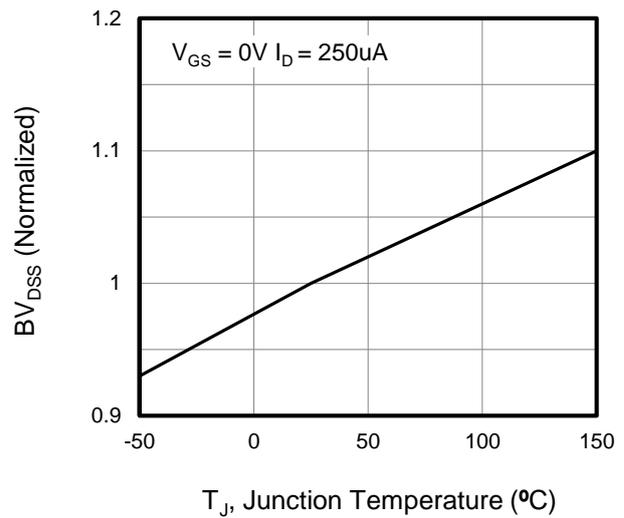
Figure 5. Transfer Characteristics
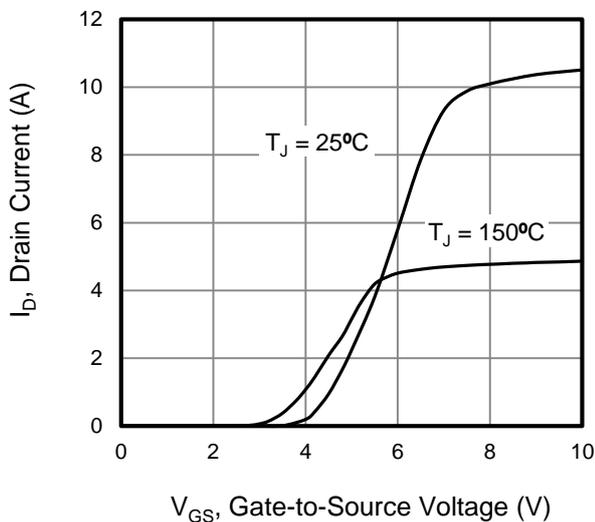
Figure 6. On-Resistance vs. Temperature

Typical Characteristics $T_J = 25^\mathbf{o}C$, unless otherwise noted

Figure 7. Capacitance

V_{DS}, Drain-to-Source Voltage (V)
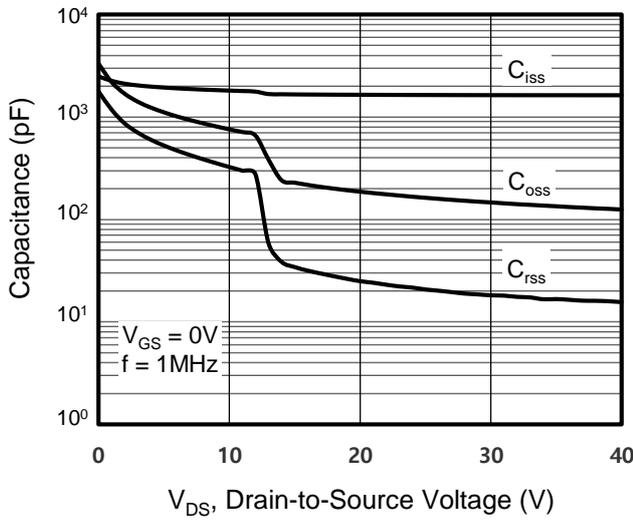
Figure 8. Gate Charge

Q_g, Total Gate Charge (nC)
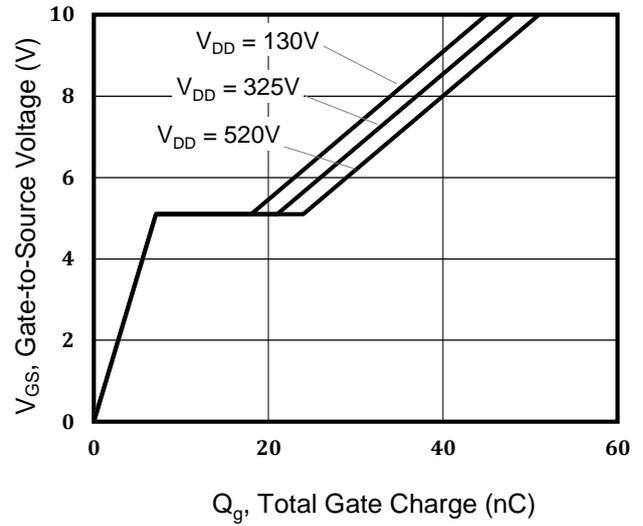
Figure 9. Transient Thermal Impedance TO-220F

T_p, Pulse Width (s)
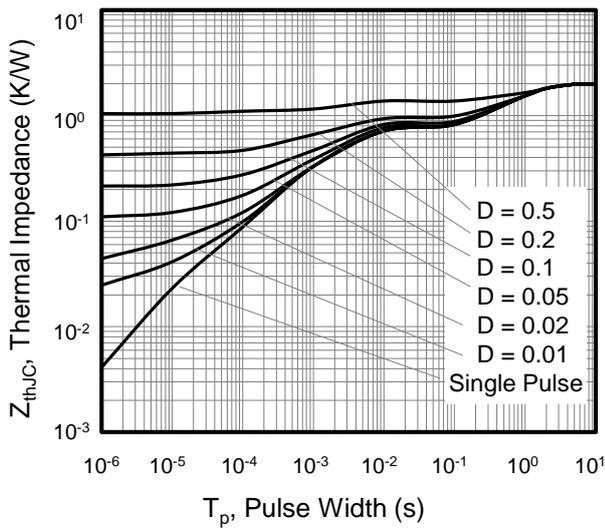
Figure 10. Transient Thermal Impedance TO-220


T_p, Pulse Width (s)
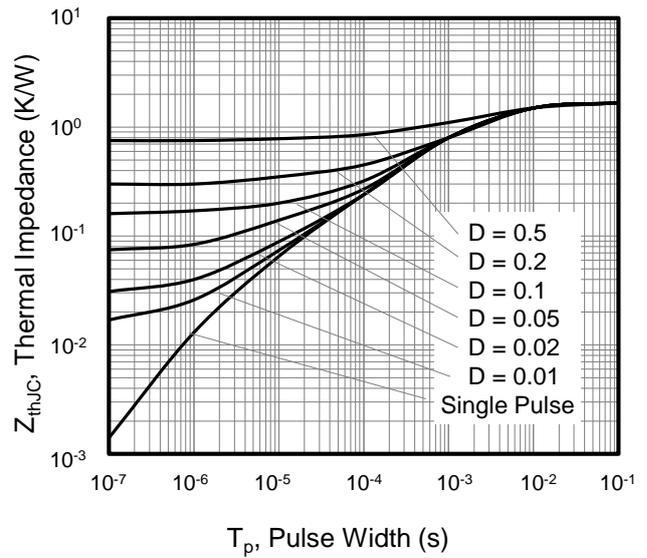
Figure A：Gate Charge Test Circuit and Waveform
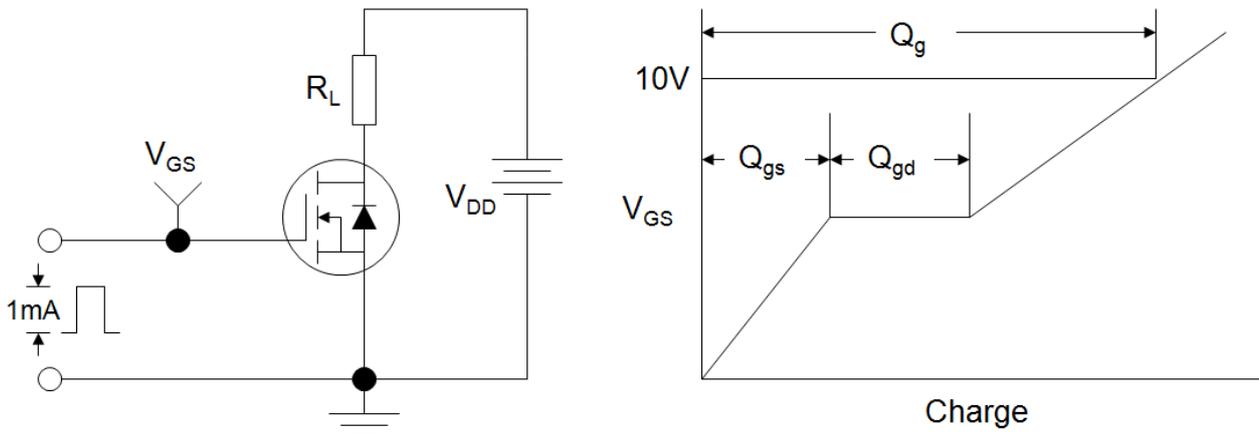

Figure B：Resistive Switching Test Circuit and Waveform
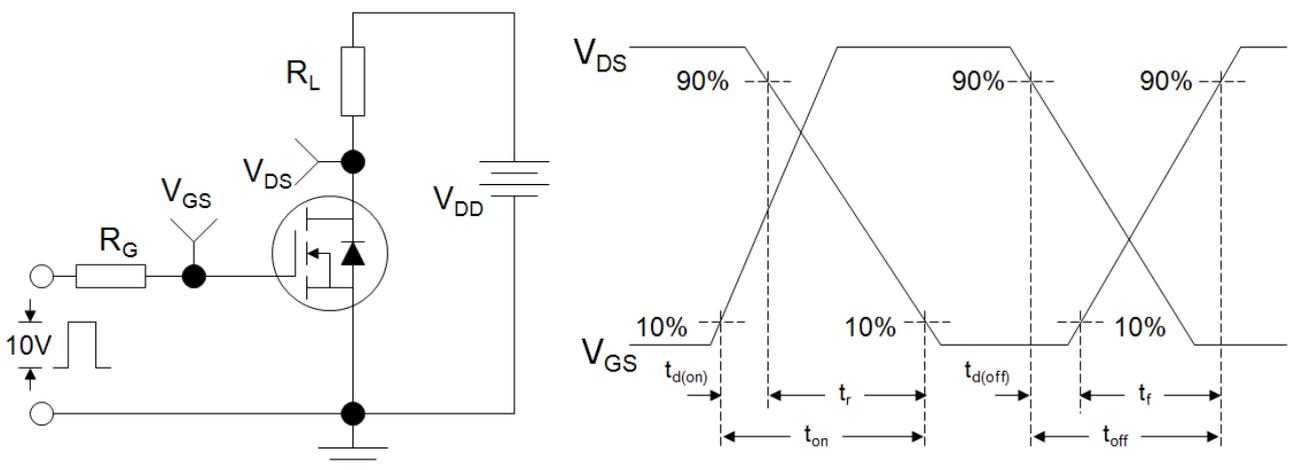
**Figure C：Unclamped Inductive Switching Test Circuit and Waveform**

REASUNOS
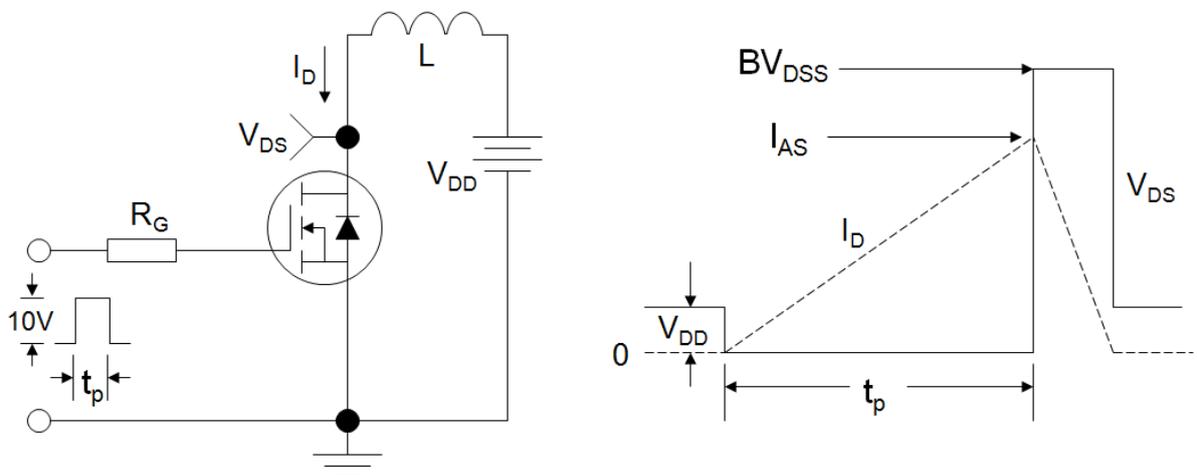
TO-220F

# TO-220
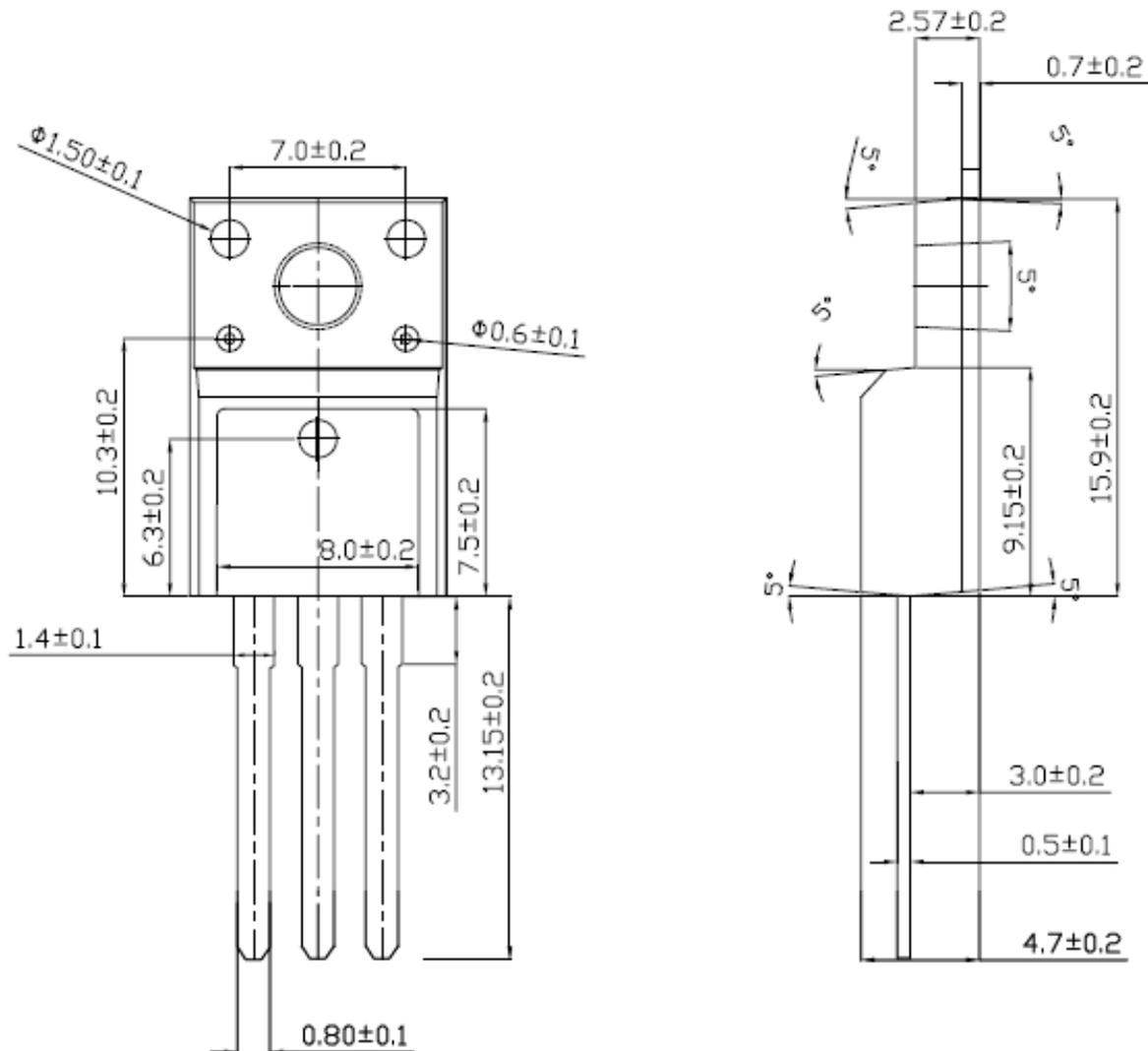
REASUNOS

Disclaimer

All product specifications and data are subject to change without notice.

For documents and material available from this datasheet, Reasunos does not warrant or assume any legal liability or responsibility for the accuracy, completeness of any product or technology disclosed hereunder.

No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted by this document or by any conduct of Reasunos .

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless. Customers using or selling Reasunos products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify for any damages arising or resulting from such use or sale.

Reasunos disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Reasunos terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

Reasunos SemiConductor CO., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

In the event that any or all Reasunos products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. Reasunos believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.