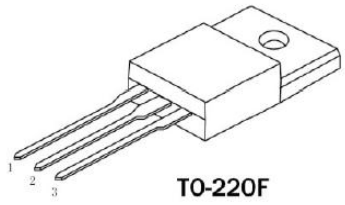
N Channel MOSFET

Lead Free Package and Finish

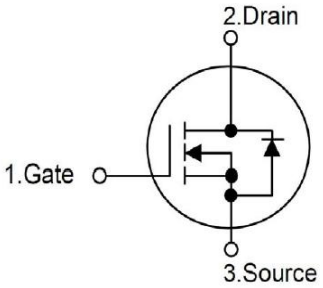
Applications:

•Adapter & Charger
•SMPS Standby Power
•AC-DC Switching Power Supply
•LED driving power

I_D	$R_{DS(ON)}$(Typ.)	V_{DSS}
10A	0.68Ω	650V



Not to Scale



Features:

•Low On Resistance
•Low Gate Charge
•Peak Current vs Pulse Width Curve
•RoHS Compliant

Ordering Information

Part Number	Package	Marking
RS10N65F	TO-220F	RS10N65F

Absolute Maximun Ratings Tc=25℃ unless otherwise specified

Symbol	Parameter	RS10N65F	Units
V_{DSS}	Drain-to-Source Voltage (Note*1)	650	V
I_D	Continuous Drain Current	10.0	A
I_D@ 100 ℃	Continuous Drain Current	5.5	
I_{DM}	Pulsed Drain Current (Note*2)	40.0	
P_D	Power Dissipation	50	W
	Derating Factor above 25℃	0.32	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Engergy L=10mH V_{DD}=150V R_G=25Ω T_J=25℃	562	mJ
T_L	Maximum Temperature for Soldering	300	℃
T_{PKG}	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the“Absolute Maximum Ratings”Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS10N65F	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.92	℃/W	Drain lead soldered to water cooled heatsink,P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber,free air.

OFF Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-source Breakdown Voltage	650	--	--	v	V_{GS}=0V,I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=650V,V_{GS}=0V
I_{GSS}	Gate-to-Source Forward Leakage	--	--	100	nA	V_{GS}=+30V V_{DS}=0V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}=-30V V_{DS}=0V

ON Characteristics TJ=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	--	0.68	0.85	Ω	V_{GS}=10V,I_D=5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{GS}=V_{DS},I_D=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	23	--	nS	V_{DS}=325V I_D=10A R_G=25Ω (Note:3,4)
t_{rise}	Rise Time	--	15	--		
$t_{d(OFF)}$	Turn-OFF Delay Time	--	90	--		
t_{fall}	Fall Time	--	30	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1294	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
C_{oss}	Output Capacitance	--	149	--		
C_{rss}	Reverse Transfer Capacitance	--	18	--		
Q_g	Total Gate Charge	--	35	--	nC	V_{DS}=520V I_D=10A V_{GS}=10V (Note:3,4)
Q_{gs}	Gate-to-Source Charge	--	7	--		
Q_{gd}	Gate-to-Drain("Miller"）Charge	--	18	--		

Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	--	--	10	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current	--	--	40	A	
V_{SD}	Diode Forward Voltage	--	--	1	V	I_S=10A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	320	--	nS	V_{GS}=0V I_S=10A,di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.2	--	μC	

Notes:

*1.TJ=±25℃ to +150℃.
*2.Repetitive rating;pulse width limited by maximum junction temperature.
*3.Pulse width≤300μs;duty cycle ≤1%.
*4.Basically not affected by temperature.

Typical Feature curve

Figure1.Typical Output Characteristics

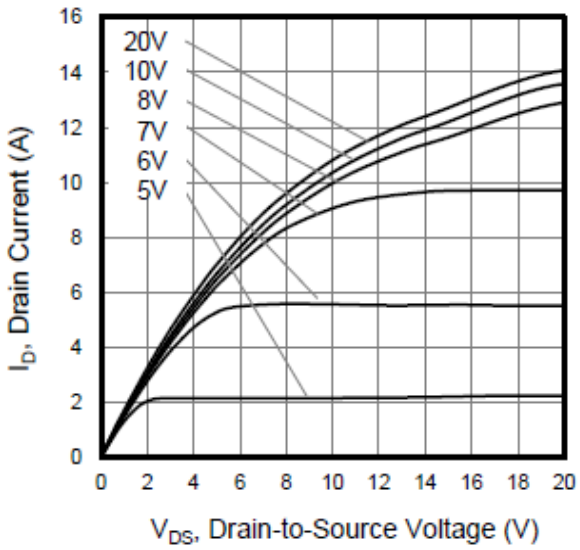
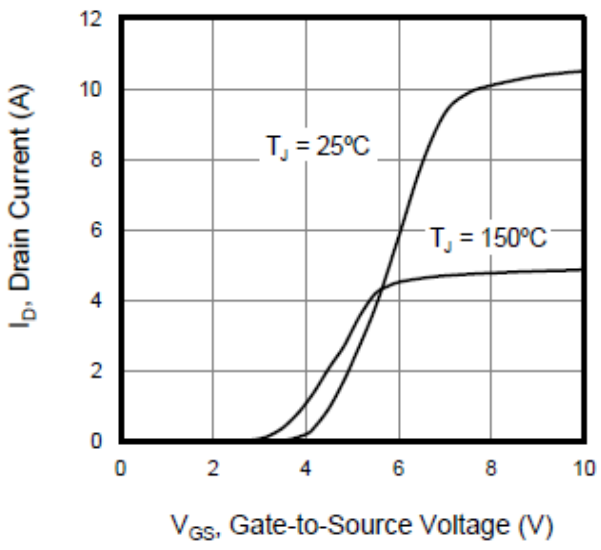
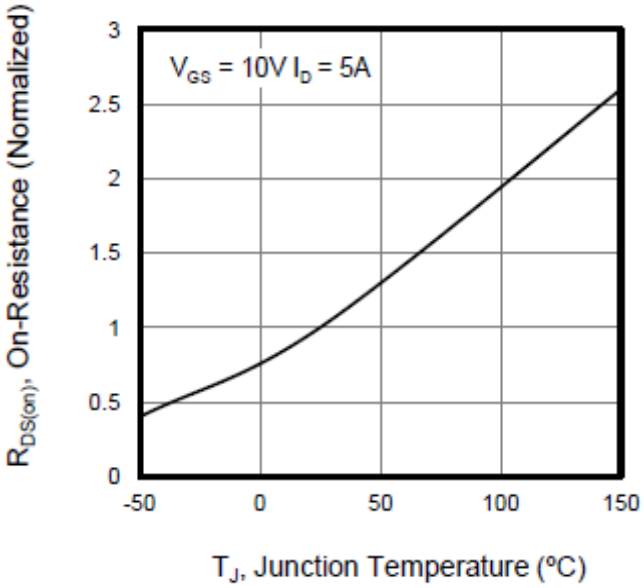


Figure2.Typical Transfer Characteristics



Figuer3.Typical ON Resistance vs Temperature



Figuer4.Typical Body Diode Transfer Characteristics

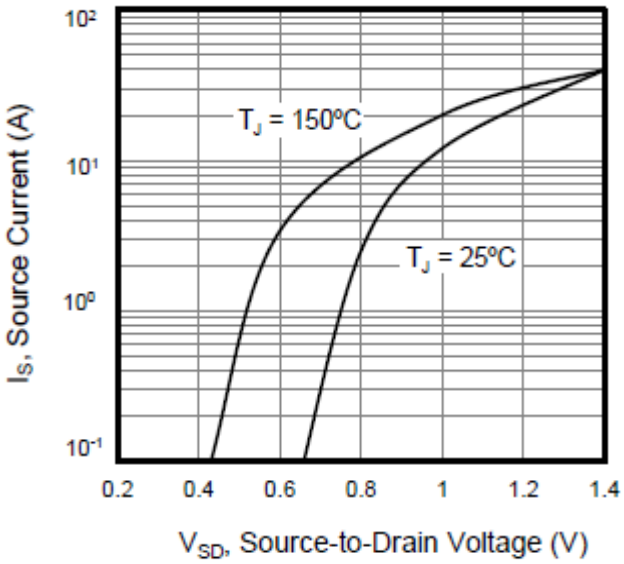


Figure5.Typical Drain current vs. Temperature

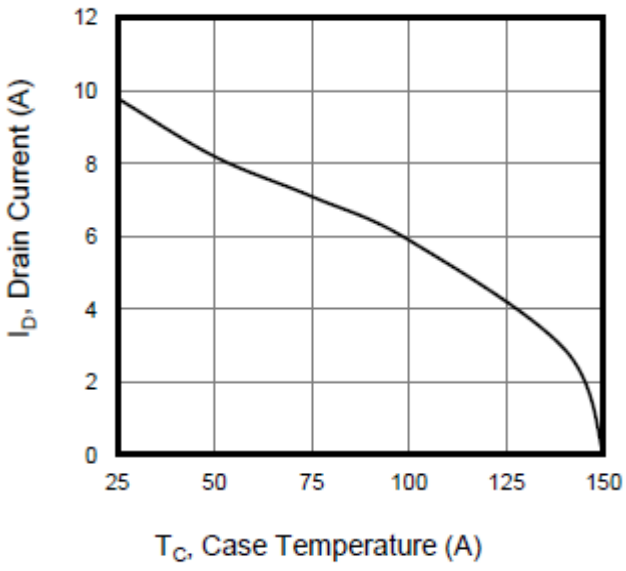


Figure6. BVDSS Variation vs. Temperature

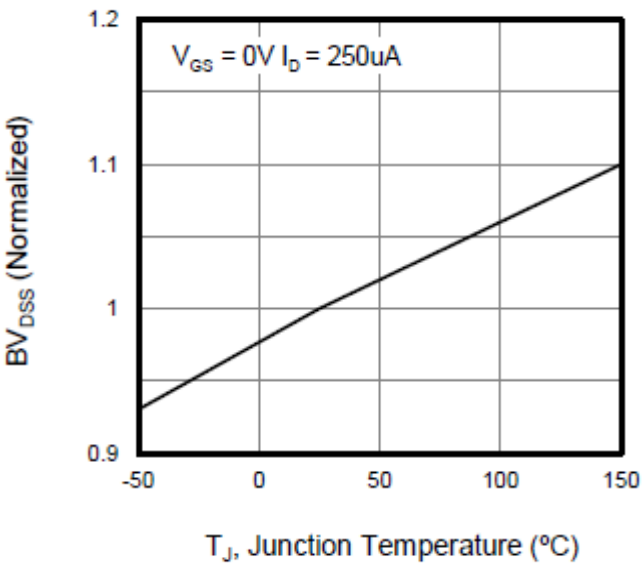


Figure7. Capacitance vs. Drain to Source Voltage

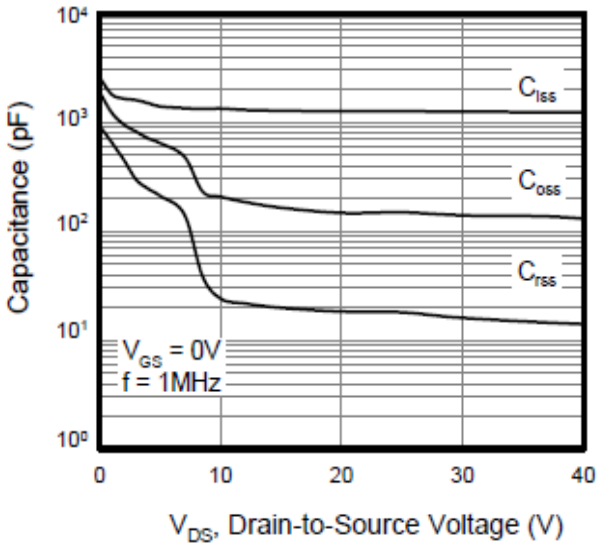


Figure8. Gate Charge

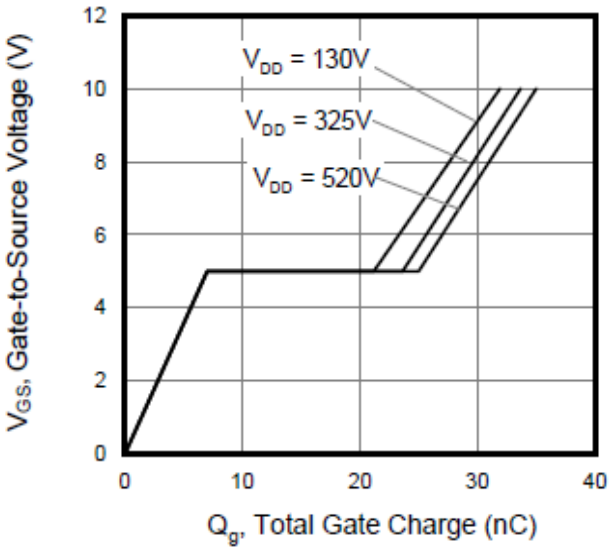
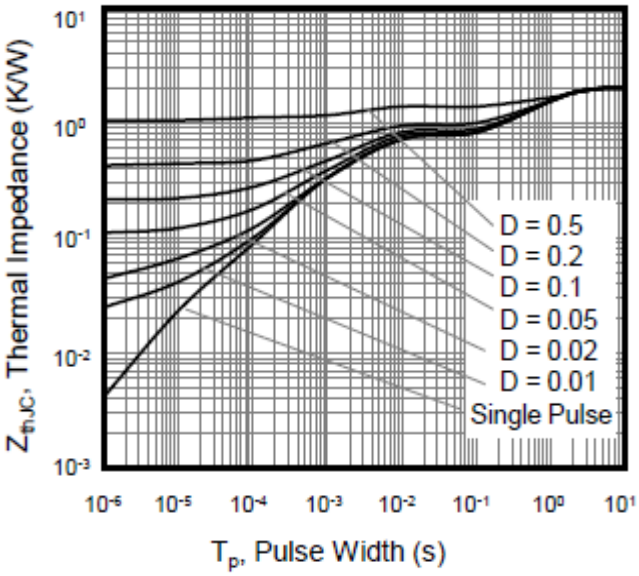


Figure9. Transient Thermal Impedance



Test Circuits and Waveforms

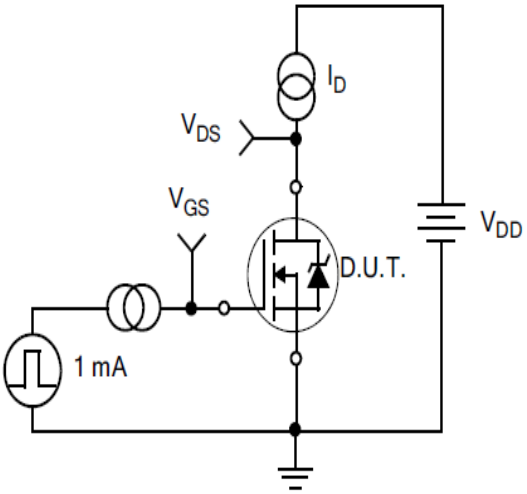


Figure11.
Gate Charge Test Circuit

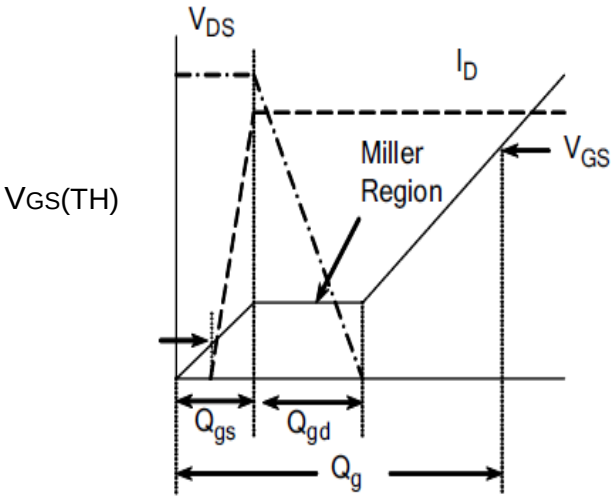


Figure12.
Gate Charge Waveform

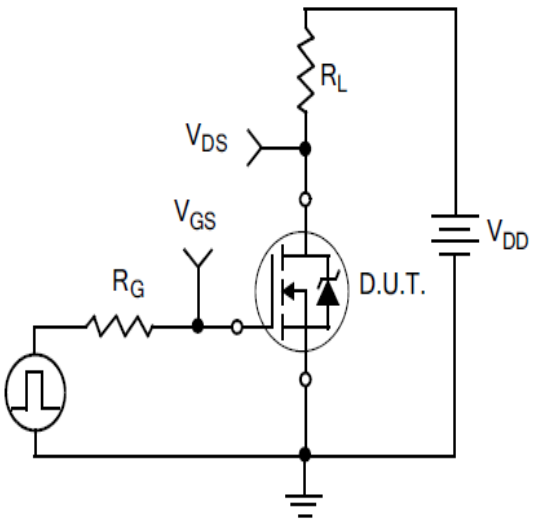


Figure13.
Resistive Switching Test Circuit

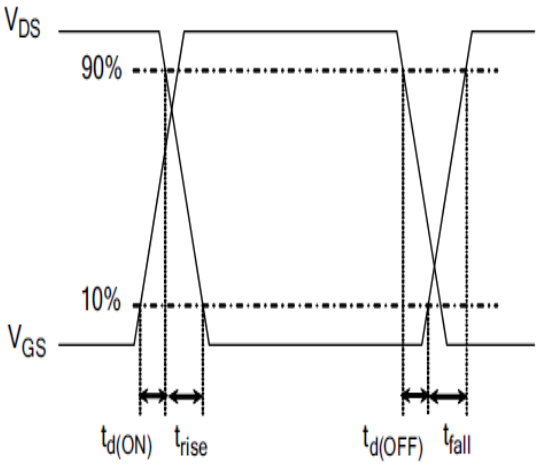


Figure14.
Resistive Switching Waveforms

Test Circuits and Waveforms

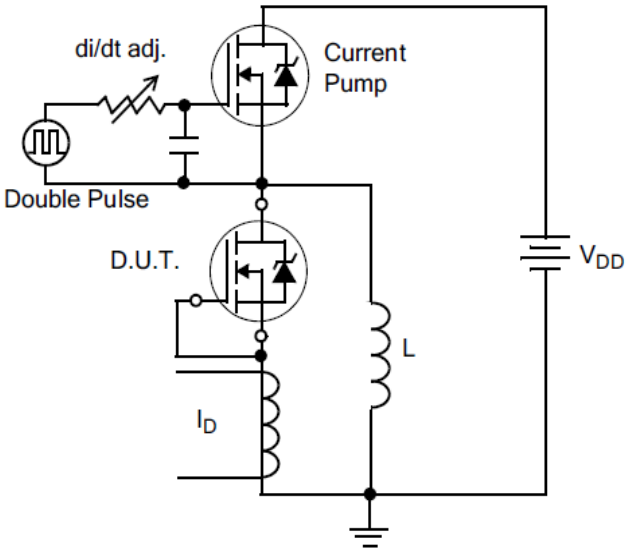


Figure15.Diode Reverse Recovery Test Circuit

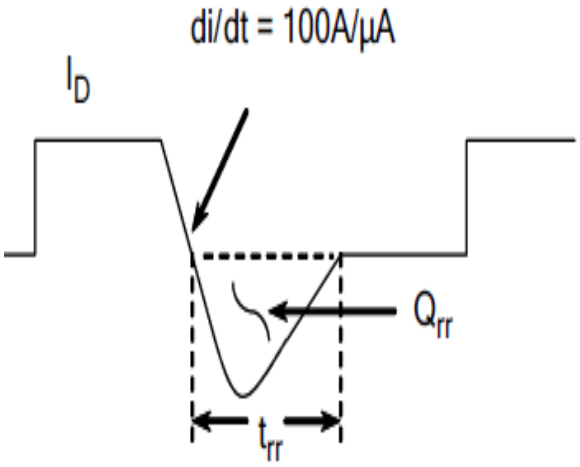


Figure16.Diode Reverse Recovery Waveform

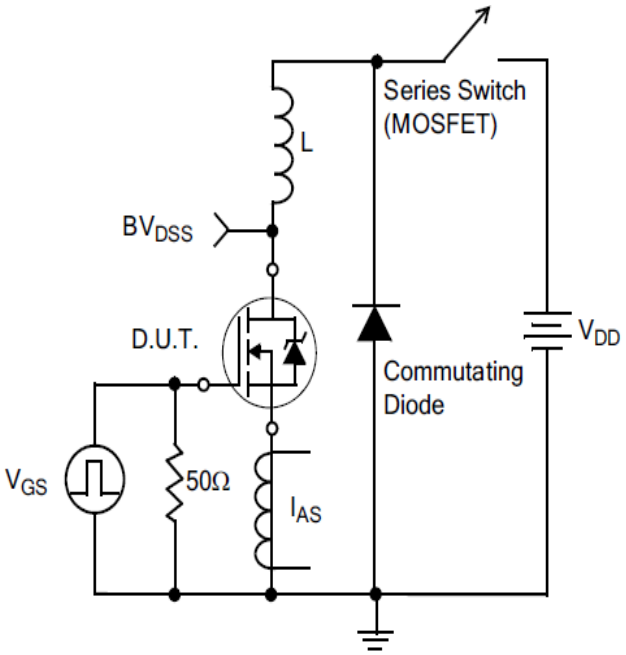
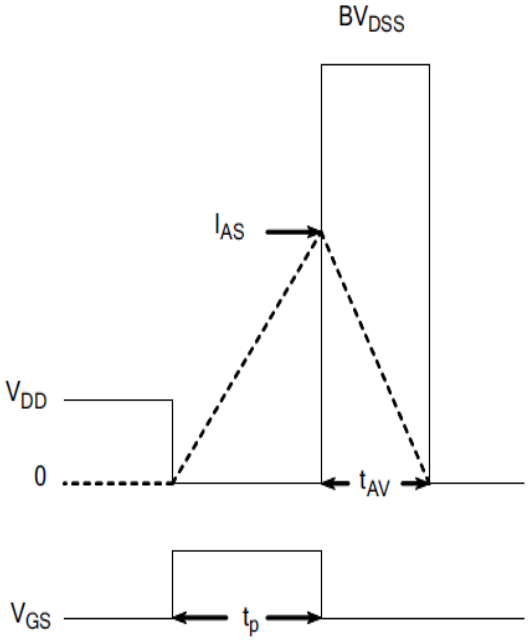


Figure17.Unclamped Inductive Switching Test Circuit

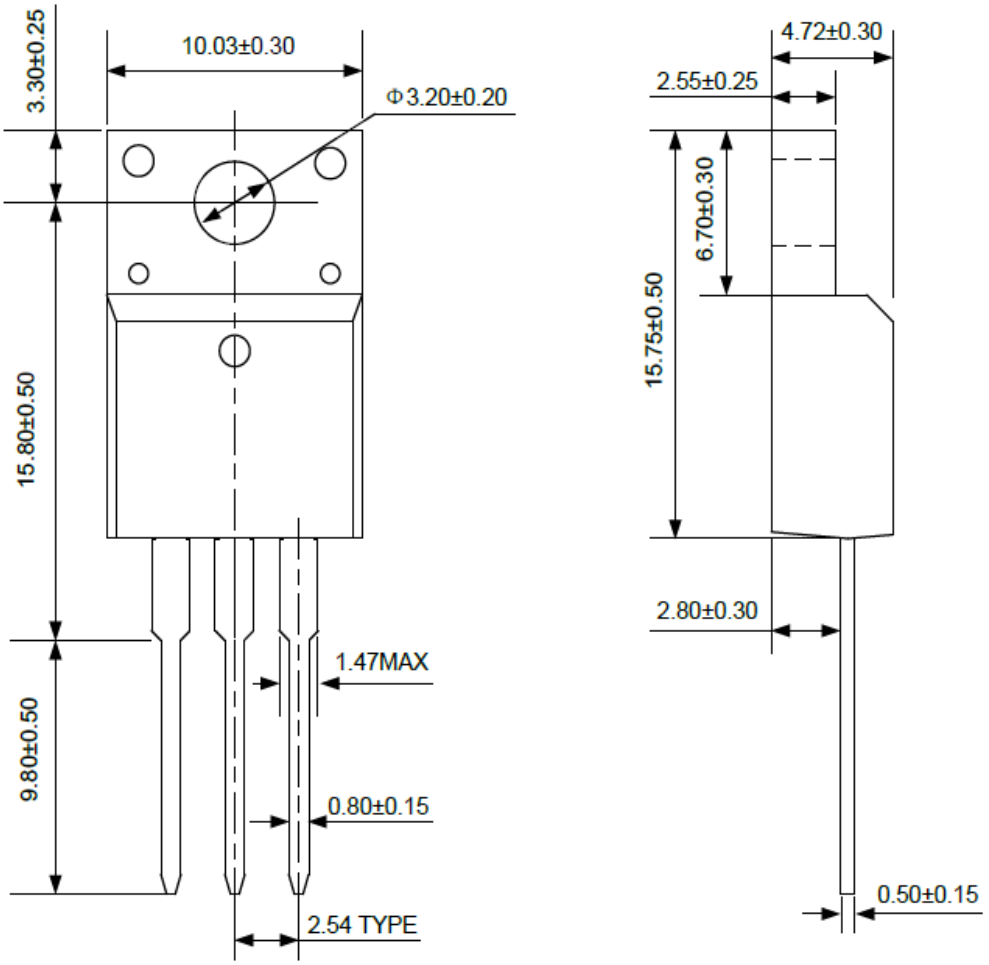


$$E_{AS}=\frac{I_{AS}^2 L}{2}$$

Figure18.Unclamped Inductive Switching Waveforms

Package outline drawing

Unit： mm



TO-220F

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