

ACPL-064L, ACPL-M61L, ACPL-W61L, ACPL-K64L

Low-Power 10-MBd Digital CMOS Optocouplers

Description

The Broadcom[®] low-power ACPL-x6xL digital optocouplers combine an AlGaAs light emitting diode (LED) and an integrated high gain photodetector. The optocoupler consumes low power, at maximum 1.3 mA I_{DD} current per channel across temperature. With a forward LED current as low as 1.6 mA, most microprocessors can directly drive the LED.

An internal Faraday shield provides a guaranteed common-mode transient immunity specification of 20 kV/ μ s. Maximum AC and DC circuit isolation is achieved while maintaining TTL/CMOS compatibility.

The optocouplers' CMOS outputs are slew-rate controlled and designed to allow the rise and fall time to be controlled over a wide load-capacitance range.

The ACPL-x6xL series operates from both 3.3V and 5V supply voltages with guaranteed AC and DC performance from -40°C to $+105^{\circ}\text{C}$.

These low-power optocouplers are suitable for high-speed logic interface applications.

Features

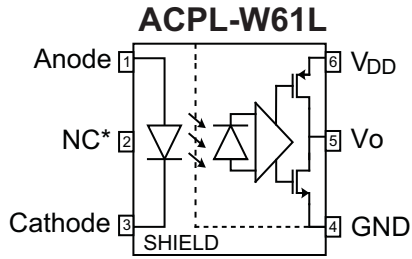
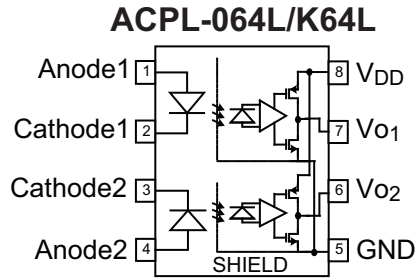
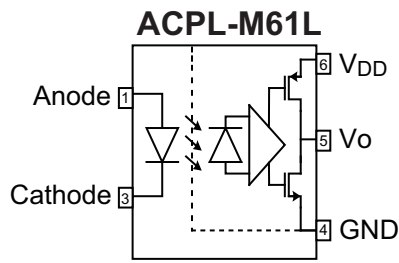
- Low I_{DD} current: 1.3 mA/channel maximum
- Low input current: 1.6 mA
- Built-in slew-rate controlled outputs
- 20 kV/ μ s minimum Common-Mode Rejection (CMR) at $V_{CM} = 1000\text{V}$
- High speed: 10 MBd minimum
- Guaranteed AC and DC performance over wide temperature: -40°C to $+105^{\circ}\text{C}$
- Package selection: SO-5, SO-8, stretched SO-6, and stretched SO-8
- Safety approval
 - UL 1577 recognized: 3750 V_{rms} for 1 minute for ACPL-064L/M61L and 5000 V_{rms} for 1 minute for ACPL-W61L/K64L
 - CSA approval
 - IEC/EN/DIN EN 60747-5-5 approval for Reinforced Insulation
- RoHS-compliant

Applications

- Communication interfaces: RS485, CANBus, and I²C
- Microprocessor system interfaces
- Digital isolation for A/D and D/A converters

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagrams



NOTE: A 0.1- μ F bypass capacitor must be connected as close as possible between pins V_{DD} and GND.

Truth Table

LED	Output
ON	L
OFF	H

Ordering Information

The ACPL-064L and ACPL-M61L are UL recognized with an isolation voltage of 3750 V_{rms} for 1 minute per UL1577. The ACPL-W61L and ACPL-K64L are UL recognized with an isolation voltage of 5000 V_{rms} for 1 minute per UL1577. All devices are RoHS-compliant.

Part Number	Option RoHS-Compliant	Package	Surface Mount	Tape and Reel	UL1577 5000 V _{rms} / 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-M61L	-000E	SO-5	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-064L	-000E	SO-8	X				100 per tube
	-060E		X			X	100 per tube
	-500E		X	X			1500 per reel
	-560E		X	X		X	1500 per reel
ACPL-W61L	-000E	Stretched S06	X		X		100 per tube
	-060E		X		X	X	100 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACPL-K64L	-000E	Stretched S08	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

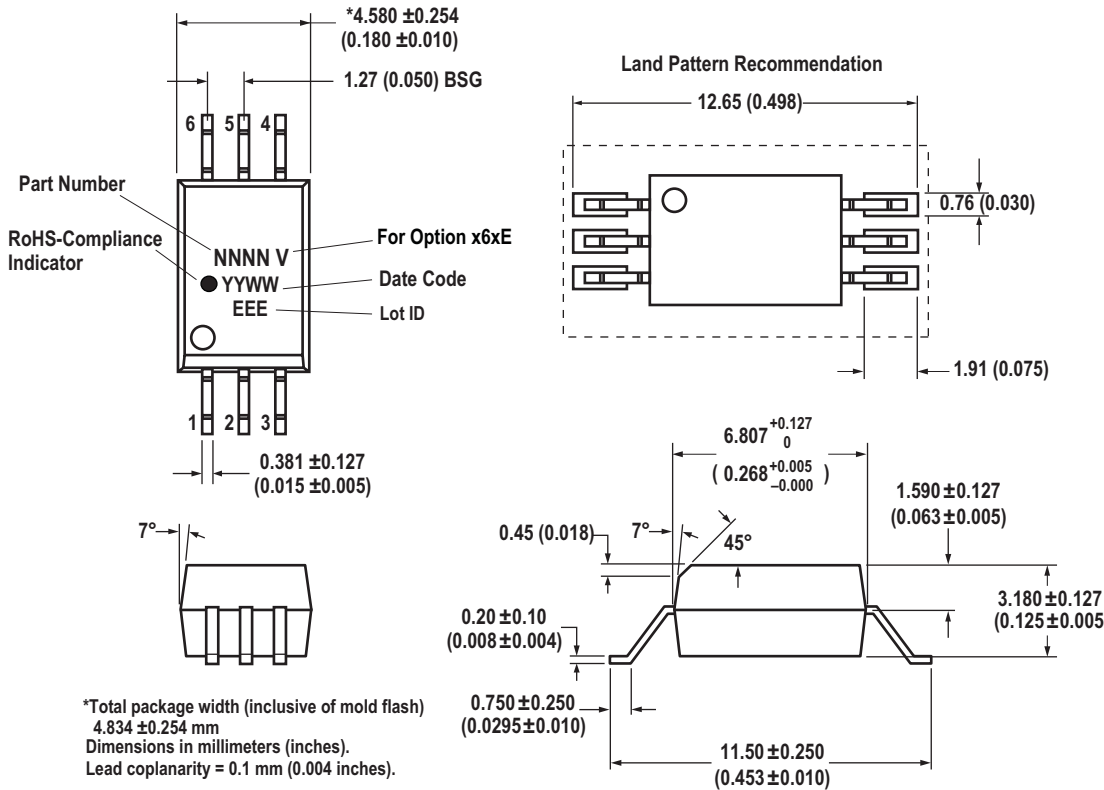
To form an ordering part number, choose a part number from the part number column and combine it with the desired option from the RoHS option column.

Example:

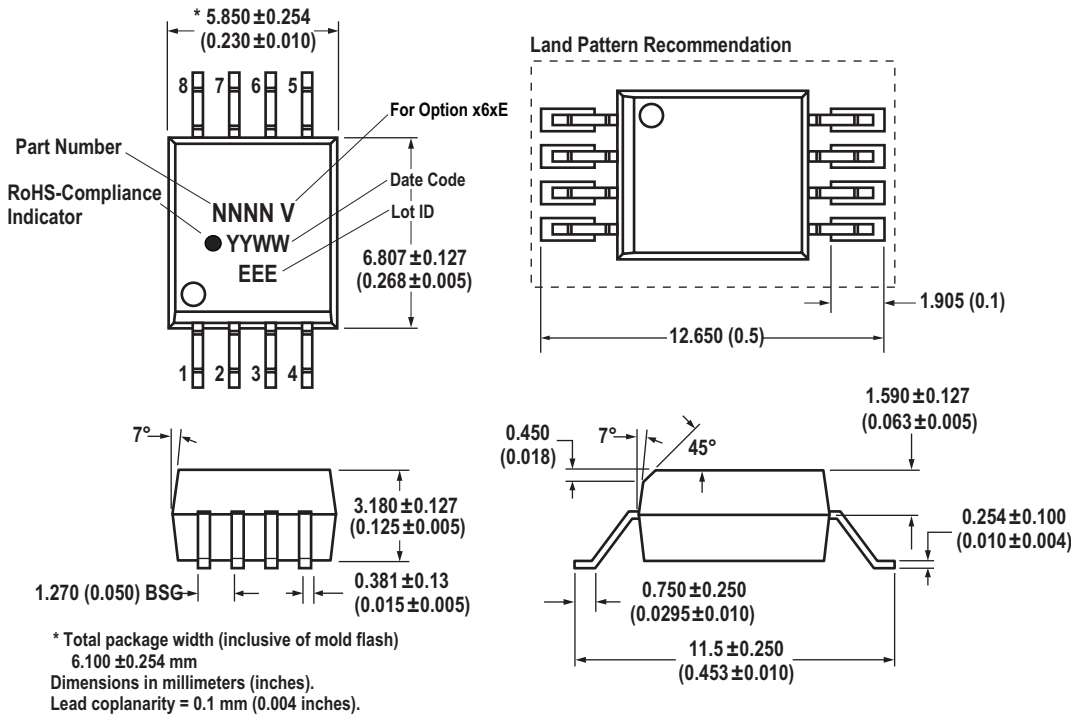
Part number ACPL-M61L-560E describes an optocoupler with a surface mount SO-5 package; delivered in Tape and Reel with 1500 parts-per-reel; with IEC/EN/DIN EN 60747-5-5 Safety Approval; and full RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

ACPL-W61L Stretched SO-6 Package



ACPL-K64L Stretched SO-8 Package



Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-064L, ACPL-M61L, ACPL-W61L, and ACPL-K64L are approved by the following organizations:

- **IEC/EN/DIN EN 60747-5-5 (Option 060 only)**
- **UL** — Approval under UL 1577 component recognition program up to $V_{ISO} = 3750 V_{rms}$ for the ACPL-M61L/064L and $V_{ISO} = 5000 V_{rms}$ for the ACPL-W61L/K64L File E55361.
- **CSA** — Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

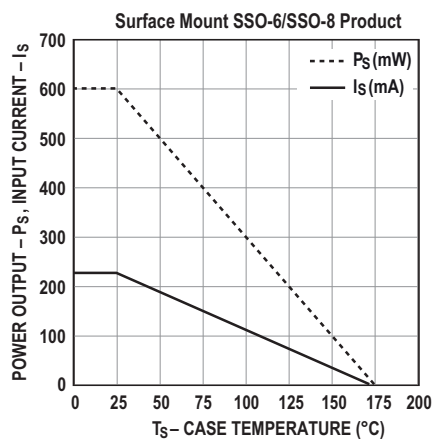
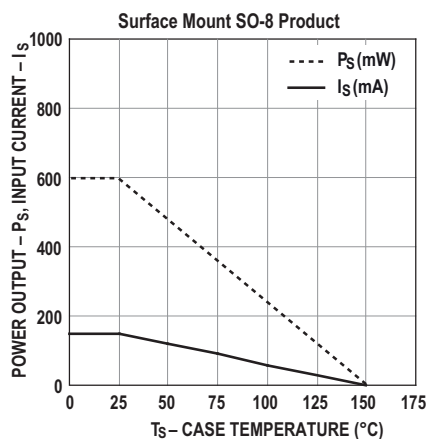
Parameter	Symbol	ACPL-064L	ACPL-M61L	ACPL-W61L ACPL-K64L	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	4.9	5	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	4.8	5	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	175	175	V	VDE 0303-11/DIN EN 60112 (2010-05)
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics^a (Option 060)

Description	Symbol	Characteristic		Unit
		ACPL-064L/ ACPL-M61L	ACPL-W61L/ ACPL-K64L	
Installation classification per DIN VDE 0110/39, Table 1 For Rated Mains Voltage $\leq 150 V_{rms}$ For Rated Mains Voltage $\leq 300 V_{rms}$ For Rated Mains Voltage $\leq 600 V_{rms}$ For Rated Mains Voltage $\leq 1000 V_{rms}$		I – IV I – IV I – III I – III	I – IV I – IV I – IV I – III	
Climatic Classification		55/105/21	55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	V_{IORM}	567	1140	V_{peak}
Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1s$, Partial Discharge $< 5 pC$	V_{PR}	1063	2137	V_{peak}
Input to Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10s$, Partial Discharge $< 5 pC$	V_{PR}	907	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage $t_{ini} = 60s$)	V_{IOTM}	6000	8000	V_{peak}
Safety-Limiting Values – maximum values allowed in the event of a failure				
Case Temperature	T_S	150	175	$^{\circ}C$
Input Current ^b	$I_{S, INPUT}$	150	230	mA
Output Power ^b	$P_{S, OUTPUT}$	600	600	mW
Insulation Resistance at T_S , $V_{IO} = 500V$	R_S	$>10^9$	$>10^9$	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

b. Refer to the following figures for dependence of P_S and I_S on ambient temperature:



NOTE: These optocouplers are suitable for *safe electrical isolation* only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Condition
Storage Temperature	T_S	-55	+125	°C	
Operating Temperature	T_A	-40	+105	°C	
Reverse Input Voltage	V_R	—	5	V	
Supply Voltage	V_{DD}	—	6.5	V	
Average Forward Input Current	I_F	—	8	mA	
Peak Forward Input Current (I_F at 1- μ s pulse width, <10% duty cycle)	$I_{F(TRAN)}$	—	1	A	$\leq 1\text{-}\mu\text{s}$ Pulse Width, <300 pulses/second
			80	mA	$\leq 1\text{-}\mu\text{s}$ Pulse Width, <10% Duty Cycle
Output Current	I_O	—	10	mA	
Output Voltage	V_O	-0.5	$V_{DD} + 0.5$	V	
Input Power Dissipation	P_I	—	14	mW	
Output Power Dissipation	P_O	—	20	mW	
Lead Solder Temperature	T_{LS}	—	260°C for 10s., 1.6 mm below seating plane		
Solder Reflow Temperature Profile	See Package Outline Drawings .				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	T_A	-40	+105	°C
Input Current, Low Level	I_{FL}	0	250	μ A
Input Current, High Level	I_{FH}	1.6	6.0	mA
Power Supply Voltage	V_{DD}	2.7	5.5	V
Forward Input Voltage	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over the recommended temperature ($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$) and supply voltage ($2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$). All typical specifications are at $V_{DD} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Channel	Min.	Typ.	Max.	Unit	Test Conditions
Input Forward Voltage	V_F		0.95	1.3	1.7	V	$I_F = 2\text{ mA}$; Figure 1 and Figure 2
Input Reverse Breakdown Voltage	BV_R		3	5	—	V	$I_R = 10\text{ }\mu\text{A}$
Logic High Output Voltage	V_{OH}		$V_{DD} - 0.1$	V_{DD}	—	V	$I_F = 0\text{ mA}$, $V_I = 0\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or ($R_T = 870\Omega$), $I_O = -20\text{ }\mu\text{A}$
			$V_{DD} - 1.0$	V_{DD}	—	V	$I_F = 0\text{ mA}$, $V_I = 0\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or ($R_T = 870\Omega$), $I_O = -3.2\text{ mA}$
Logic Low Output Voltage	V_{OL}		—	0.03	0.1	V	$I_F = 2\text{ mA}$, $V_I = 5\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or $V_I = 3.3\text{V}$ ($R_T = 870\Omega$), $I_O = 20\text{ }\mu\text{A}$
			—	0.18	0.4	V	$I_F = 2\text{ mA}$, $V_I = 5\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or $V_I = 3.3\text{V}$ ($R_T = 870\Omega$), $I_O = 3.2\text{ mA}$
Input Threshold Current	I_{TH}		—	0.7	1.3	mA	Figure 3
Logic Low Output Supply Current	I_{DDL}	Single	—	0.8	1.3	mA	Figure 4
		Dual	—	1.6	2.6		
Logic High Output Supply Current	I_{DDH}	Single	—	0.8	1.3	mA	Figure 5
		Dual	—	1.6	2.6		
Input Capacitance	C_{IN}		—	60	—	pF	$f = 1\text{ MHz}$, $V_F = 0\text{V}$
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		—	-1.6	—	mV/ $^\circ\text{C}$	$I_F = 2\text{ mA}$

Switching Specifications (AC)

Over the recommended temperature ($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$) and supply voltage ($2.7\text{V} \leq V_{DD} \leq 5.5\text{V}$).
All typical specifications are at $V_{DD} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Propagation Delay Time to Logic Low Output ^a	t_{PHL}	—	46	80	ns	$I_F = 2\text{ mA}$, $V_I = 5\text{V}$, $R_T = 1.68\text{ k}\Omega$, $C_L = 15\text{ pF}$, CMOS Signal Levels. $I_F = 2\text{ mA}$, $V_I = 3.3\text{V}$, $R_T = 870\Omega$, $C_L = 15\text{ pF}$, CMOS Signal Levels. Figure 6 and Figure 7
Propagation Delay Time to Logic High Output ^a	t_{PLH}	—	40	80	ns	
Pulse Width	t_{PW}	100	—	—	ns	
Pulse Width Distortion ^b	PWD	—	6	30	ns	
Propagation Delay Skew ^c	t_{PSK}	—	—	30	ns	
Output Rise Time (10% to 90%)	t_R	—	12	—	ns	
		—	10	—	ns	$I_F = 2\text{ mA}$, $V_I = 3.3\text{V}$, $R_T = 870\Omega$, $C_L = 15\text{ pF}$, CMOS Signal Levels.
Output Fall Time (90% to 10%)	t_F	—	12	—	ns	$I_F = 2\text{ mA}$, $V_I = 5\text{V}$, $R_T = 1.68\text{ k}\Omega$, $C_L = 15\text{ pF}$, CMOS Signal Levels.
		—	10	—	ns	$I_F = 2\text{ mA}$, $V_I = 3.3\text{V}$, $R_T = 870\Omega$, $C_L = 15\text{ pF}$, CMOS Signal Levels.
Static Common-Mode Transient Immunity at Logic High Output ^d	$ CM_H $	20	35	—	kV/ μs	$V_{CM} = 1000\text{V}$, $T_A = 25^\circ\text{C}$, $I_F = 0\text{ mA}$, $V_I = 0\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or ($R_T = 870\Omega$), $C_L = 15\text{ pF}$, CMOS Signal Levels. Figure 8
Static Common-Mode Transient Immunity at Logic Low Output ^e	$ CM_L $	20	35	—	kV/ μs	$V_{CM} = 1000\text{V}$, $T_A = 25^\circ\text{C}$, $V_I = 5\text{ V}$ ($R_T = 1.68\text{ k}\Omega$) or $V_I = 3.3\text{V}$ ($R_T = 870\Omega$), $I_F = 2\text{ mA}$, $C_L = 15\text{ pF}$, CMOS Signal Levels. Figure 8
Dynamic Common-Mode Transient Immunity ^f	CMR_D	—	35	—	kV/ μs	$V_{CM} = 1000\text{ V}$, $T_A = 25^\circ\text{C}$, $I_F = 2\text{ mA}$, $V_I = 5\text{V}$ ($R_T = 1.68\text{ k}\Omega$) or $V_I = 3.3\text{ V}$ ($R_T = 870\Omega$), 10 MBd data rate, the absolute increase of PWD < 10 ns Figure 8

- t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.
- PWD is defined as $|t_{PHL} - t_{PLH}|$.
- t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is seen between units at any given temperature within the recommended operating conditions.
- CM_H is the maximum tolerable rate of rise of the common-mode voltage to assure that the output remains in a high logic state.
- CM_L is the maximum tolerable rate of fall of the common-mode voltage to assure that the output remains in a low logic state.
- CM_D is the maximum tolerable rate of the common-mode voltage during data transmission to assure that the absolute increase of the PWD is less than 10 ns.

Package Characteristics

All typical specifications are at $T_A = 25^\circ\text{C}$.

Parameter	Symbol	Part Number	Min.	Typ.	Max.	Unit	Test Conditions
Input-Output Insulation ^a	V_{ISO}	ACPL-064L ACPL-M61L	3750	—	—	V_{rms}	RH < 50% for 1 min. $T_A = 25^\circ\text{C}$
		ACPL-W61L ACPL-K64L	5000	—	—		
Input-Output Resistance	$R_{\text{I-O}}$		—	10^{12}	—	Ω	$V_{\text{I-O}} = 500\text{V}$
Input-Output Capacitance	$C_{\text{I-O}}$		—	0.6	—	pF	$f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$

a. In accordance with UL 1577, ACPL-064L/M61L is proof tested by applying an insulation test voltage $\geq 4500 V_{\text{rms}}$ for 1 second, and ACPL-W61L/K64L is proof tested by applying an insulation test voltage $\geq 6000 V_{\text{rms}}$ for 1 second, (Leakage detection current limit, $I_{\text{I-O}} \leq 5 \mu\text{A}$).

Figure 1: Typical Input Diode Forward Current Characteristic

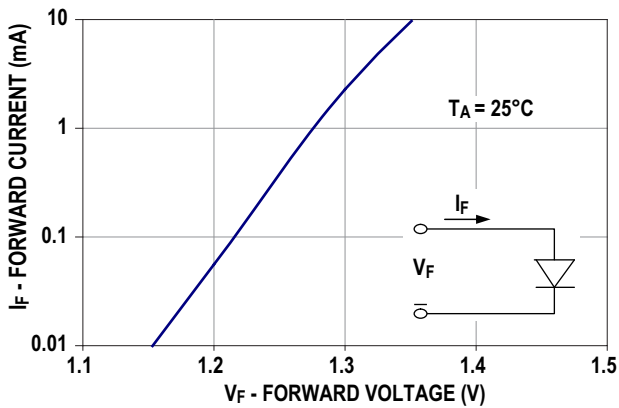


Figure 2: Typical V_F versus Temperature

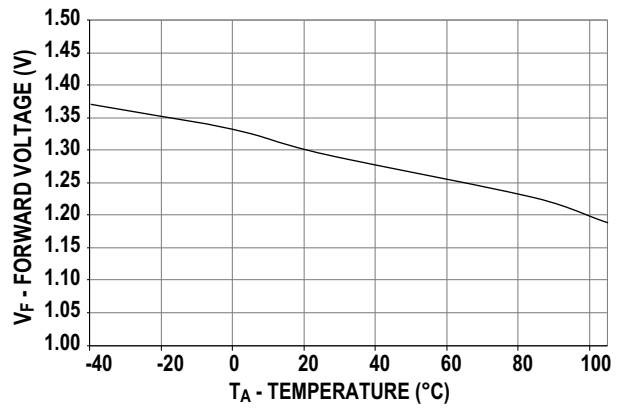


Figure 3: Typical Input Threshold Current versus Temperature

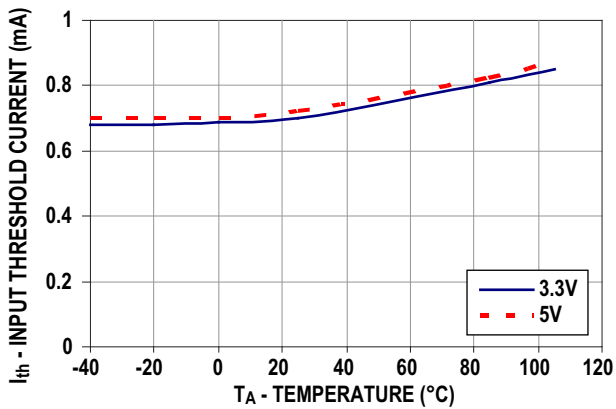


Figure 4: Typical Logic Low Output Supply Current (Per Channel) versus Temperature

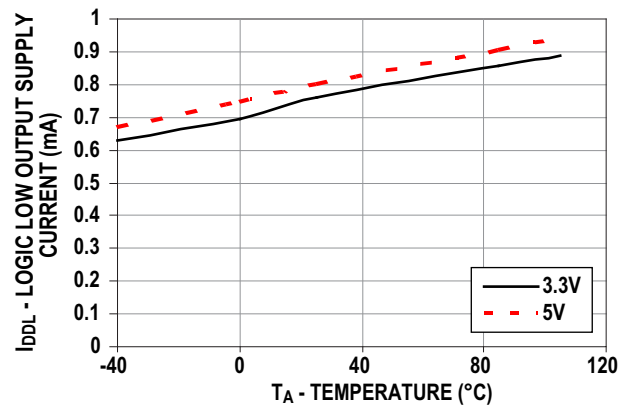


Figure 5: Typical Logic High Output Supply Current (Per Channel) versus Temperature

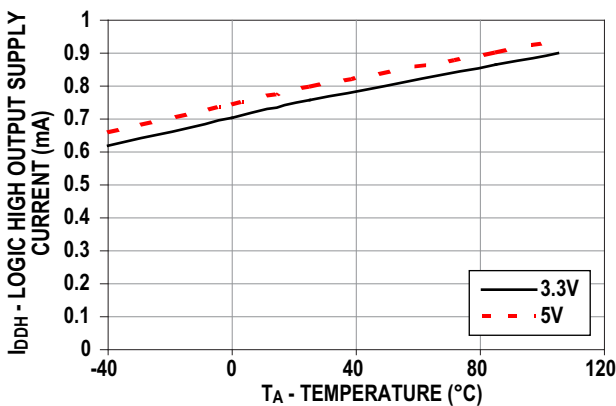


Figure 6: Typical Switching Speed versus Pulse Input with a 5V Supply Voltage

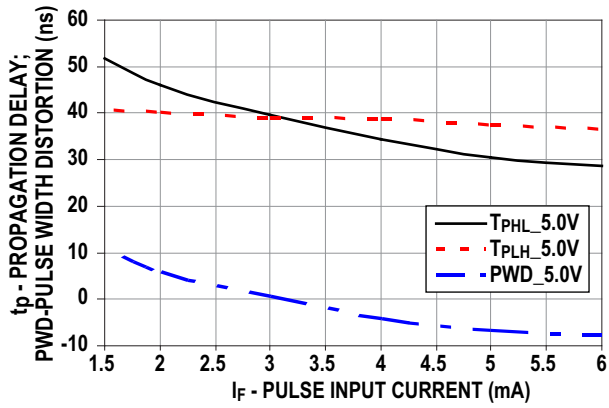
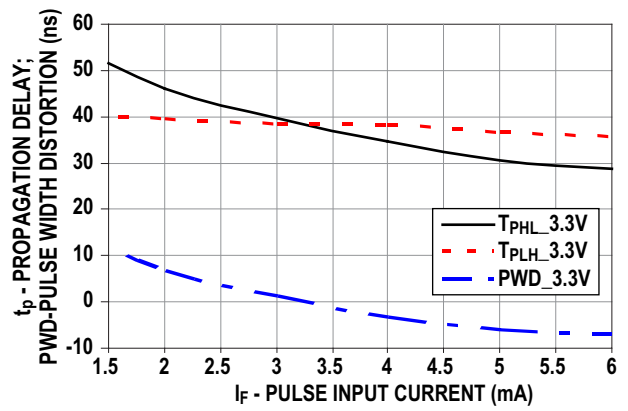


Figure 7: Typical Switching Speed versus Pulse Input Current with a 3.3V Supply Voltage



Supply Bypassing, LED Bias Resistors, and PC Board Layout

The ACPL-x6xL optocouplers are extremely easy to use and feature high-speed, push-pull CMOS outputs. Pull-up resistors are not required.

The external components required for proper operation are the input limiting resistors and the output bypass capacitor. Capacitor values should be 0.1 μF and should be placed as close as possible to the power-supply pins of the optocoupler.

For ACPL-M61L/W61L:

$$V_1 = 3.3\text{V}: R_1 = 510\Omega \pm 1\%, R_2 = 360\Omega \pm 1\%$$

$$V_1 = 5.0\text{V}: R_1 = 1000\Omega \pm 1\%, R_2 = 680\Omega \pm 1\%$$

$$R_T = R_1 + R_2 \quad R_1/R_2 = 1.5$$

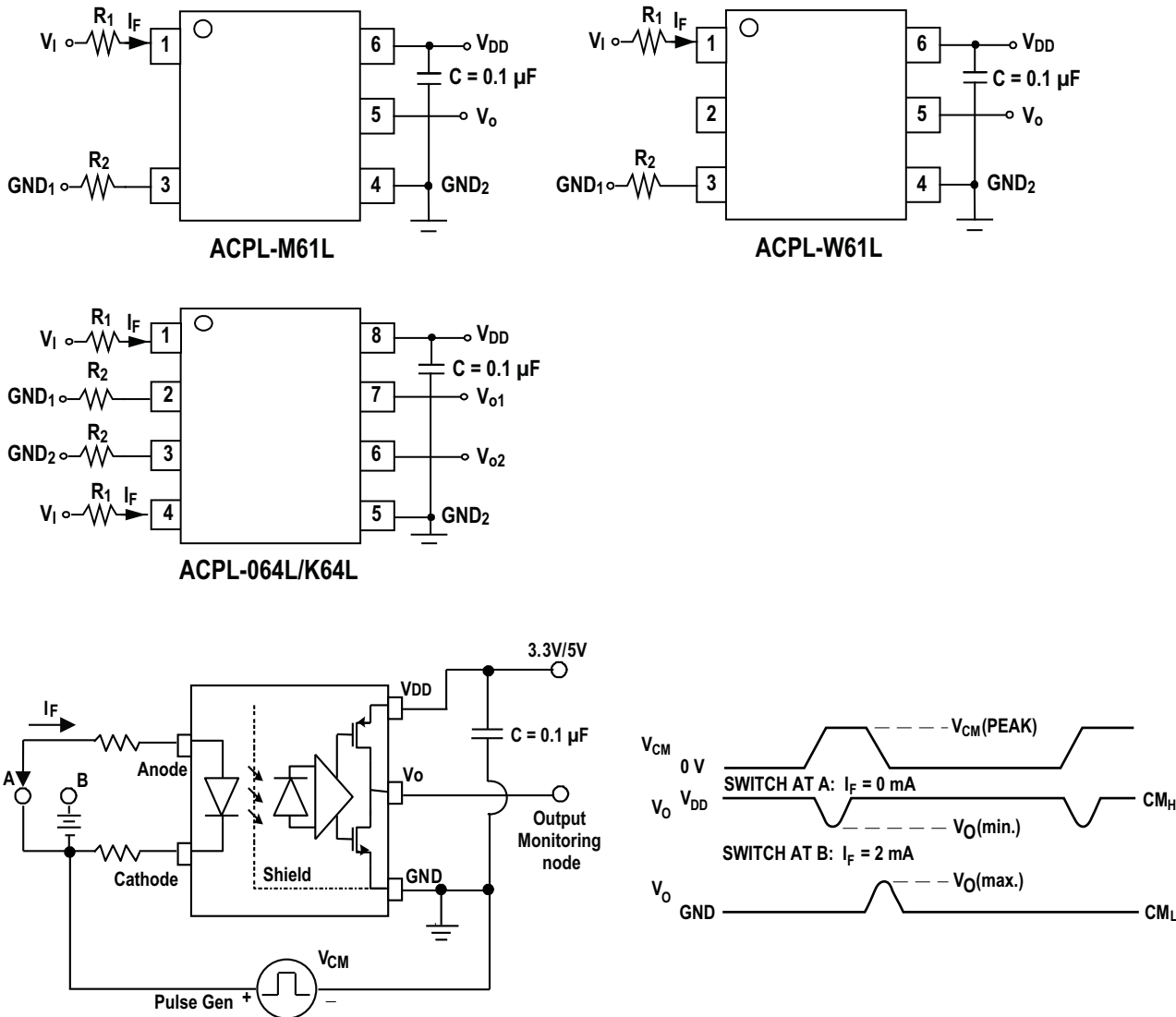
For ACPL-064L/K64L:

$$V_1 = 3.3\text{V}: R_1 = 430\Omega \pm 1\%, R_2 = 430\Omega \pm 1\%$$

$$V_1 = 5.0\text{V}: R_1 = 845\Omega \pm 1\%, R_2 = 845\Omega \pm 1\%$$

$$R_T = R_1 + R_2 \quad R_1/R_2 = 1$$

Figure 8: Recommended PCB Layout and Input Current-Limiting Resistor Selection



Propagation Delay, Pulse-Width Distortion, and Propagation Delay Skew

Propagation delay is a figure of merit that describes how quickly a logic signal propagates through a system. The propagation delay from low-to-high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high.

Similarly, the propagation delay from high-to-low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high-to-low (see Figure 9).

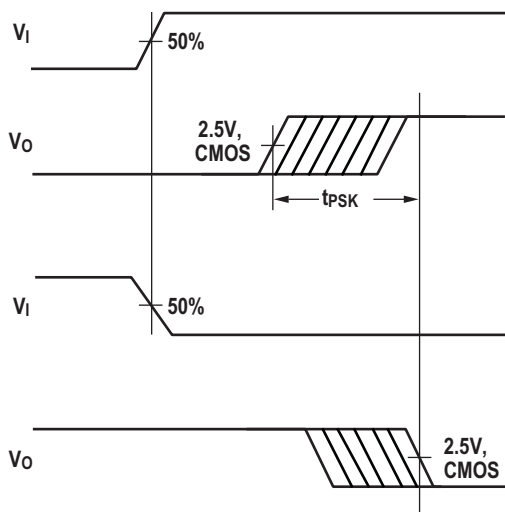
Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} . PWD determines the maximum data rate of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, a PWD of 20% to 30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK} , is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern.

If the parallel data is being sent through a group of optocouplers, differences in propagation delays cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it determines the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} , for any given group of optocouplers which are operating

Figure 9: Propagation Delay Skew Waveform



under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As shown in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL} , and the longest propagation delay, either t_{PLH} or t_{PHL} . As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate.

Figure 10 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

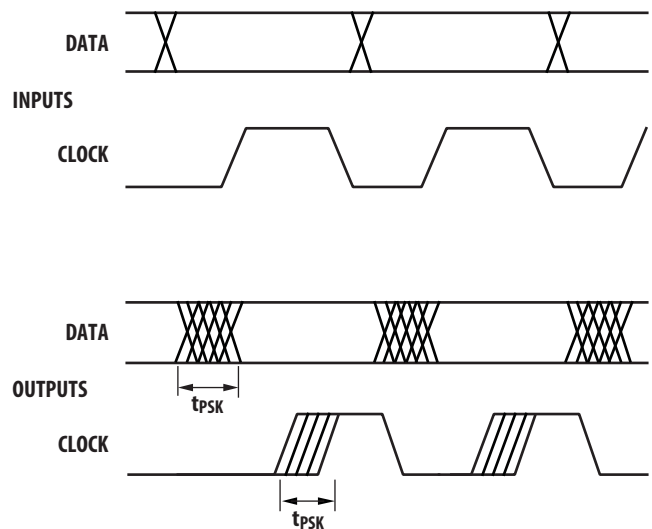
Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler.

Figure 10 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap. Otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs might start to change before the clock signal has arrived.

From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK} . A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature and power supply ranges.

Figure 10: Parallel Data Transmission Example



Optocoupler CMR Performance

The principal protection against common-mode noise comes from the fundamental isolation properties of the optocoupler, and this in turn is directly related to the Input-Output leakage capacitance of the optocoupler.

To provide maximum protection to circuitry connected to the input or output of the optocoupler, the leakage capacitance is minimized by having large separation distances at all points in the optocoupler construction, including the LED/photodiode interface.

In addition to the optocouplers' basic physical construction, additional circuit design steps mitigate the effects of common-mode noise. The most important of these is the Faraday shield on the photodetector stage.

A Faraday shield is effective in optocouplers because the internal modulation frequency (light) is many orders of magnitude higher than the common-mode noise frequency.

Improving CMR Performance at the Application Level

In an end application, it is desirable that the optocouplers' common-mode isolation be as close as possible to that indicated in the data sheet specifications. The first step in meeting this goal is to ensure maximum separation between PCB interconnects on either side of the optocoupler is maintained and that PCB tracks beneath the optocoupler are avoided.

It is inevitable that a certain amount of CMR noise will be coupled into the inputs and this can potentially result in false-triggering of the input. This problem is frequently observed in devices with high input impedance. In some cases, this can cause momentary missing pulses and can even cause input circuitry to latch-up in some alternate technologies.

The ACPL-x6xL optocoupler family does not have an input latch-up issue. Even at very high CMR levels, such as those experienced in end equipment level tests (for example IEC61000-4-4), the ACPL-x6xL series is immune to latch-up because of the simple diode structure of the LED.

In some cases, achieving the rated data sheet CMR performance level is not possible in an application. This is often because of the practical requirement to actually connect the isolator input to the output of a dynamically changing signal rather than statically tying the input to VDD or GND.

To address achievable end application performance on data sheets, the ACPL-x6xL optocouplers include an additional typical performance specification for dynamic CMR in the electrical parameter table. The dynamic CMR specification indicates the typical achievable CMR performance as the input is toggled on or off during a CMR transient.

The logic output of the ACPL-x6xL optocouplers is mainly controlled by LED current level, and since the LED current features very fast rise and fall times, dynamic noise immunity is essentially the same as static noise immunity.

Despite their immunity to input latch-up and the excellent dynamic CMR immunity, ACPL-x6xL optocoupler devices are still potentially vulnerable to misoperation caused by turning the LED either on or off during a CMR disturbance. If the LED status could be ensured by design, the overall application level CMR performance would be that of the photodetector. To benefit from the inherently high CMR capabilities of the ACPL-x6xL family, take the following precautions when operating the LED at the application level.

In particular, ensure that the LED stays either on or off during a CMR transient. Some common design techniques to accomplish this include the following:

Keep the LED On:

1. Overdrive the LED with a higher-than-required forward current.

Keep the LED Off:

1. Reverse bias the LED during the off state.
2. Minimize the off-state impedance across the anode and cathode of the LED during the off state.

All of these methods allow the full CMR capability of the ACPL-x6xL family to be achieved, but they do have practical implementation issues or require a compromise on power consumption.

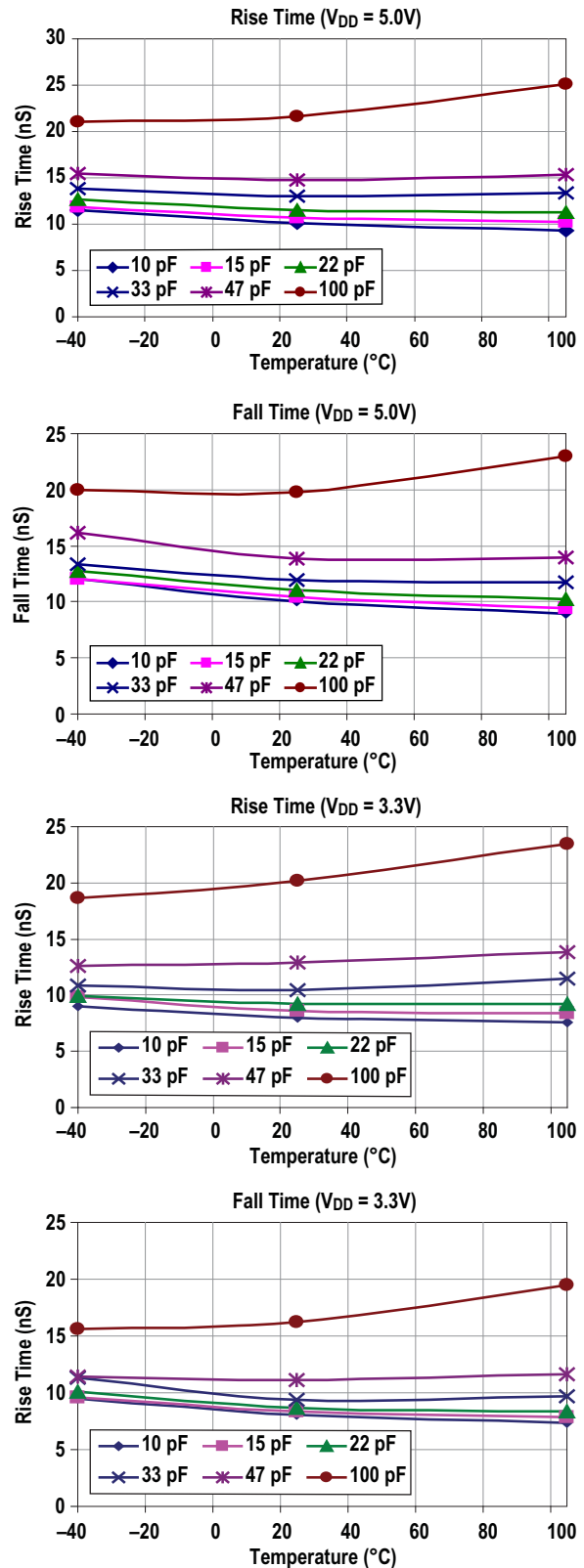
There is, however, an effective method to meet the goal of maintaining the LED status during a CMR event with no other design compromises other than a single added resistor.

This CMR optimization takes advantage of the differential connection to the LED. By ensuring the common-mode impedances at both the cathode and anode of the LED are equal, the CMR transient on the LED is effectively canceled. As shown in [Figure 11](#), this is easily achieved by using two, instead of one, input bias resistors.

Slew-Rate Controlled Outputs Feature

Typically, the output slew rate (rise and fall time) varies with the output load, as more time is required to charge up the higher load. The propagation delay and the PWD both increase with the load capacitance. This will be an issue especially in parallel communication because different communication lines will have different load capacitances. However, optocoupler ACPL-x6xL has a built-in slew-rate controlled feature to ensure that the output slew rate remains stable across wide load capacitance. Figure 13 shows the rise time and fall time for ACPL-x6xL at 3.3V and 5V.

Figure 13: Rise and Fall Time of ACPL-x6xL across Wide-Load Capacitance



Speed Improvement

A peaking capacitor can be placed across the input current-limit resistor (Figure 14) to achieve enhanced speed performance. The value of the peaking capacitor is dependent on the rise and fall time of the input signal, supply voltages, and LED input driving current (I_F). Figure 15 shows significant improvement of propagation delay and pulse width distortion with an added peak capacitor at a driving current of 2 mA and 3.3V/5V power supply.

Figure 14: Connection of Peaking Capacitor (C_{peak}) in Parallel with the Input Limiting Resistor (R_1) to Improve Speed Performance

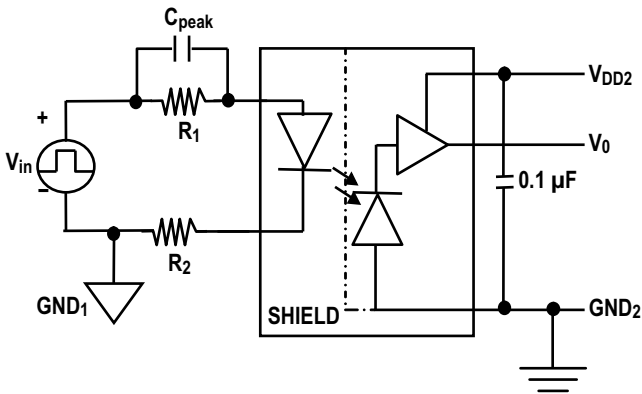
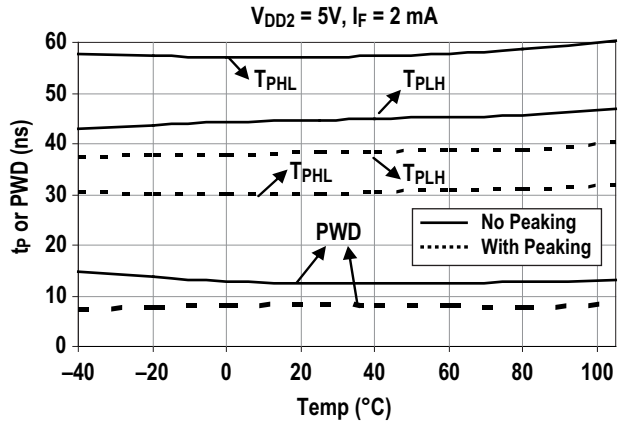
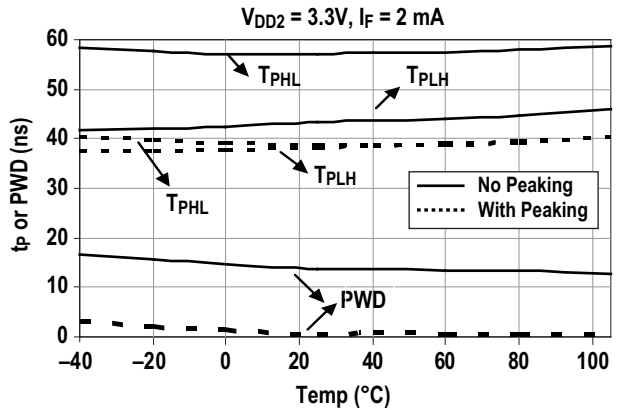


Figure 15: Improvement of t_p and PWD with an Added 100-pF Peaking Capacitor in Parallel of Input Limiting Resistor

a. $V_{DD} = 5V, C_{peak} = 47 \text{ pF}, R_1 = 845\Omega$



b. $V_{DD} = 3.3V, C_{peak} = 47 \text{ pF}, R_1 = 430\Omega$



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