5A ,2.1MHz,I2C Programmable Synchronous Buck Converter

FEATURES

- Compatible I2C Interface Up to 3.4MHz
- Input Voltage Range :2.5~5.5V
- Up to 5A Output Current
- Mode Selection Between PFM and PWM at Light Load
- Typical 50uA Quiescent Current in Light Load PFM Mode
- 2.1MHz Switching Frequency
- Integrated Soft-Start
- Input UVLO and OVP
- Build in Thermal Shutdown and OCP
- 0.25uH Inductor Support
- Compact WLCSP-20 Package

APPLICATIONS

- Smart Phones
- DSP or CPUs Processors
- Tablet, MID

GENERAL DESCRIPTION

STI8070A is an I^2C Programmable, high efficiency,2.1MHz, Synchronous Buck converter that operates in wide input voltage range from 2.5V to 5.5V. The output Voltage could be programmed from 0.72V to 1.5V. Very low standby current ensure high efficiency in light load PFM mode. The forced PWM mode could be set to avoid application problems caused by low switching frequency. A COT(Constant On-Time) structure is adaptive to achieve the fixed switching frequency and fast load transient response. STI8070A provides up to 5A output current with Integrated 28 mΩ(high side) and 18 mΩ(low side) power switch. STI8070A also implement a internal soft-start and cycle-by-cycle over current protection function. In addition, the input UVLO and OVP protection, Thermal shutdown protection.

APPILCATIONS

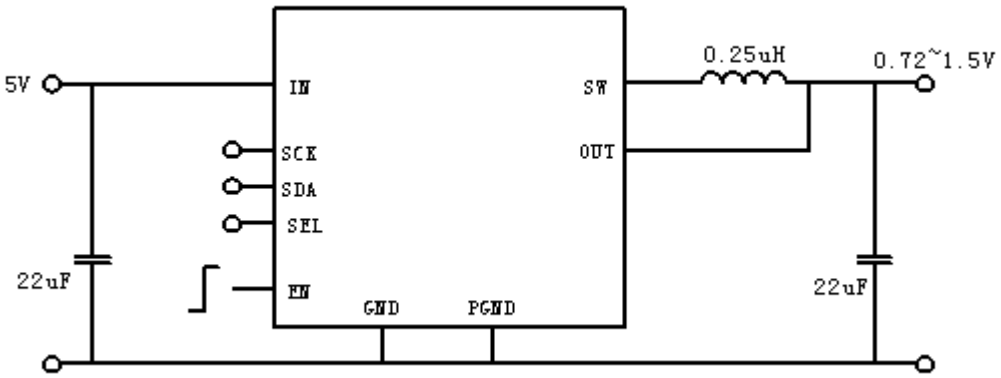
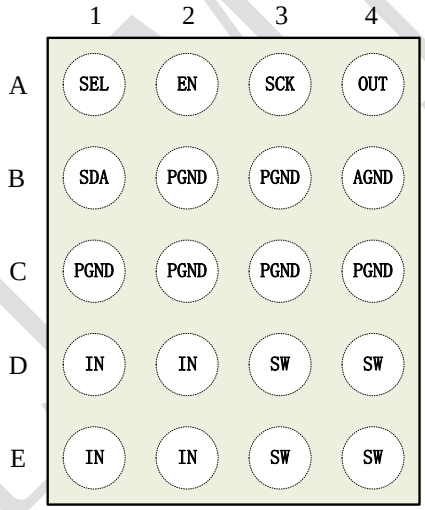


Figure 1. Basic Application Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Value	Unit
ALL Voltage Range	-0.3~6.5	V
Junction Temperature(Note2)	-40~150	°C
Storage Temperature	-65~150	°C
Junction-to-ambient Thermal Resistance	38	°C/W
Junction-to-case Thermal Resistance	9	°C/W
Power Dissipation	2.6	W

PACKAGE/ORDER INFORMATION



WLCSP-20

Top Mark: S70AXX (S70A: Device Code, XX: Inside Code)

Part Number	Package	Top mark	Quantity/ Reel
STI8070A	WLCSP-20	S70AXX	3000

PIN DESCRIPTIONS

Pin	Name	Function
A1	SEL	Voltage select pin, 0: VSEL0 register, 1: VSEL1 register
A2	EN	Enable pin, 0: Shut down, 1: Enable
A3	SCK	I^2C Clock pin
A4	OUT	Output voltage sense pin, Connect to output capacitor
B1	SDA	I^2C Data pin
B2~B3 C1~C4	PGND	Power Ground pins
B4	AGND	Analog Ground pin
D1~B2 E1~E2	IN	Power input pin, Connect to input capacitor
D3~B4 E3~E4	SW	Switching Pin, Connect to external Inductor

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	2.5	5.5	V
TA	Operating Temperature Range	-40	85	°C

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ELECTRICAL CHARACTERISTICS (Note 3)

(V_{IN}=3.6V , V_{OUT}=1V T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Under Voltage Lockout	V_{UVLO}	Vin rising		2.45		V
UVLO Hysteresis	V_{UVLO_HY}			100		mV
Input OVP Voltage	V_{INOVP}	Vin rising		6.15		V
Input OVP Hysteresis	V_{OVP_HY}			400		mV
OVP blank time	T_{OVP_BT}			20		uS
Input Supply Current	I_{IN}	EN=1, I_{load}=0, V_{out}>105%*V_{set}		50		uA
Input Shutdown current	I_{SDN}	EN="0"		0.1	1	uA
	I_{SDI2C}	I^2C set shutdown EN=1		20	30	uA
EN/SDA/SCK/MODE Logic high Threshold	V_{INH}		1.1			V
EN/SDA/SCK/MODE Logic low Threshold	V_{INL}				0.4	V
PFET peak Current limit	I_{LIM_MAX}		6.7			A
Switch On-Resistance (high side)	R_{DSONH}			28		mΩ
Switch On-Resistance (low side)	R_{DSONL}			18		mΩ
Switching Frequency	F_{osc}			2.1		MHz
Minimum Turn-on Time	T_{ON_MIN}			52		nS
Soft-start Time	T_{sst}			300		uS
Thermal Shutdown Threshold	T_{SDN}	rising		163		℃
Thermal Shutdown Hysteresis	T_{SDN_HY}			133		℃

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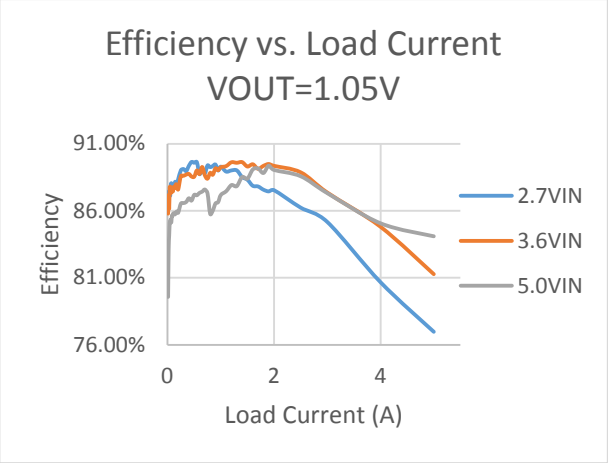
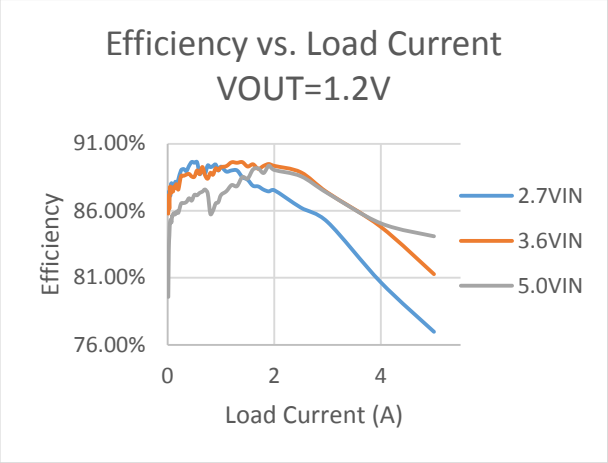
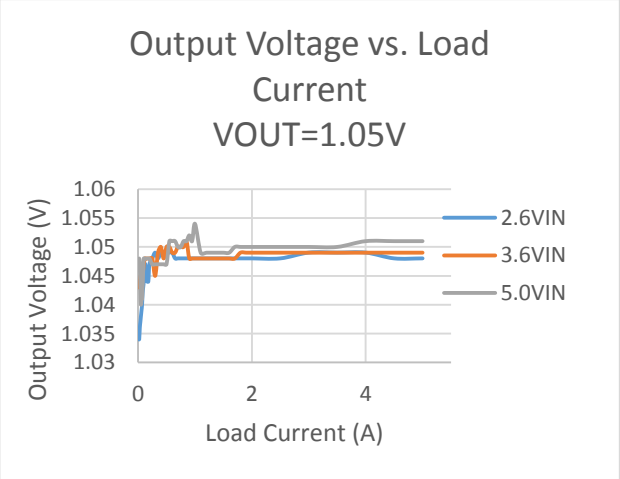
Typical Characteristics



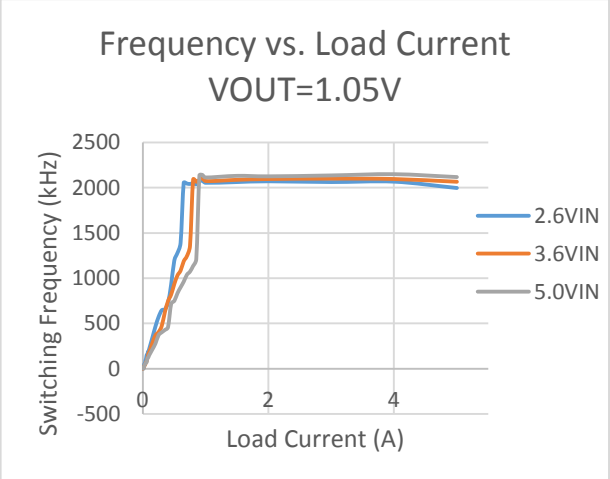
Efficiency vs. Load Current



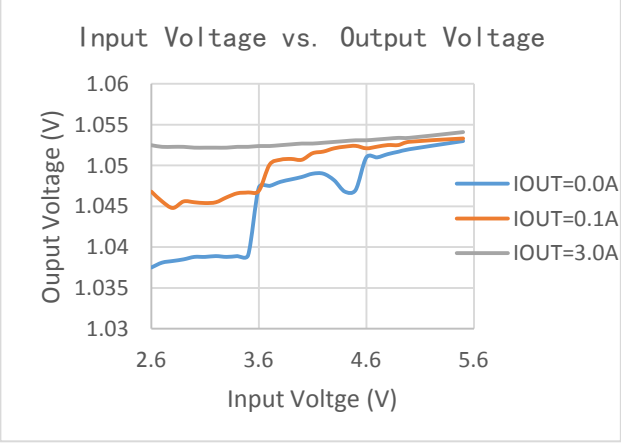
Efficiency vs. Load Current



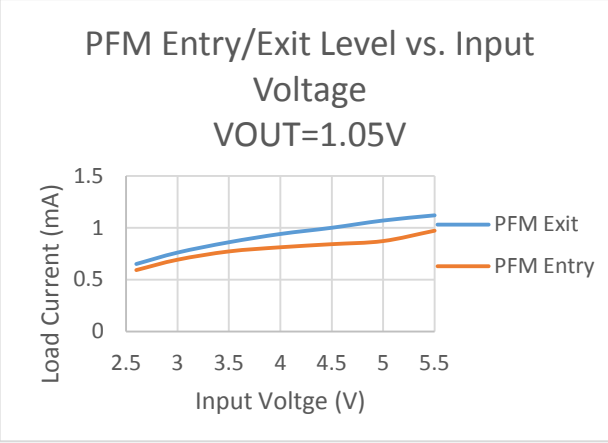
Load Current vs. Output Voltage



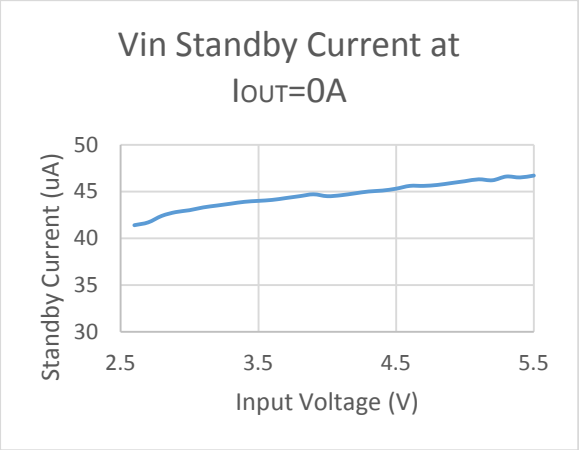
Frequency vs. Load Current



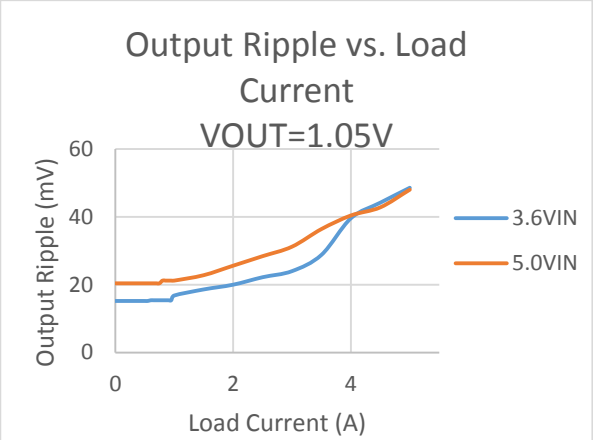
Input Voltage vs. Output Voltage



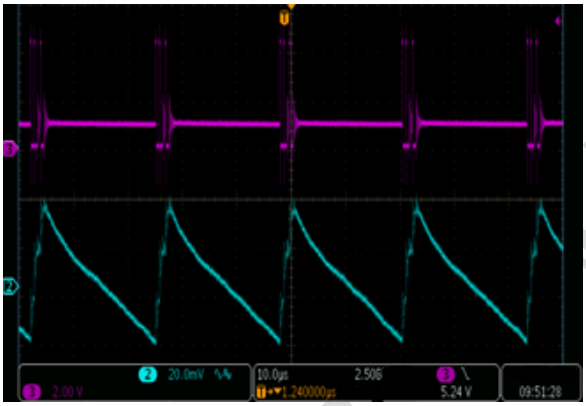
PFM Entry/Exit Level vs. Input Voltage



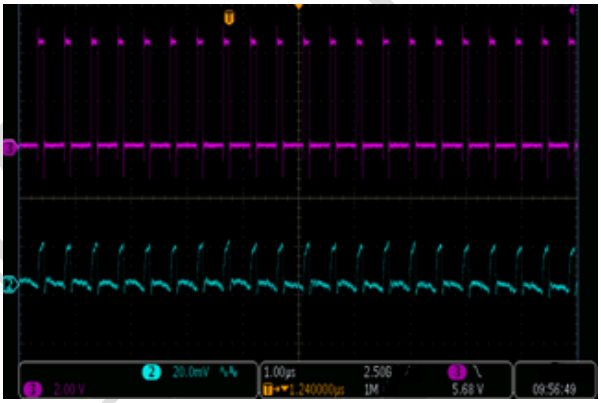
Standby Current Vs Input Voltage



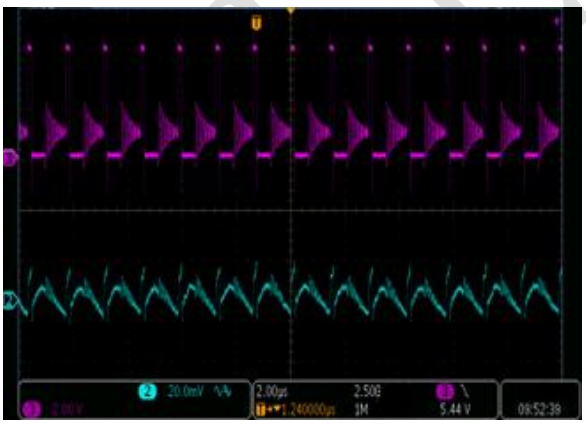
Output Ripple vs. Load Current



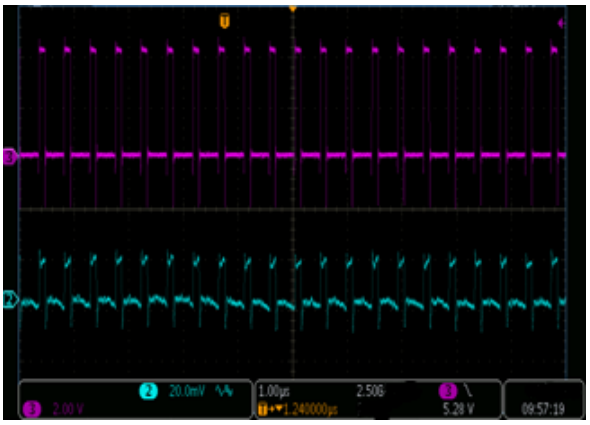
V_{IN}=5V, I_{OUT}=0.1A Ripple Waveform



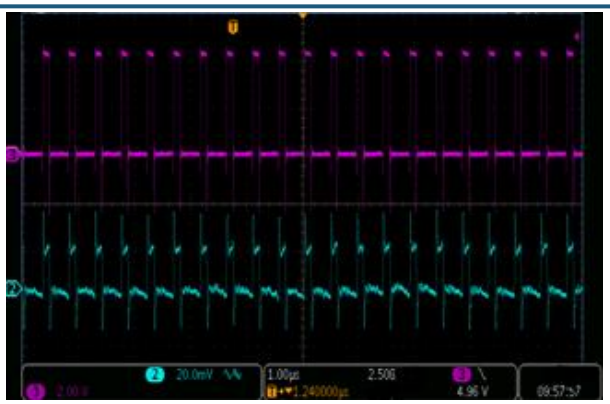
V_{IN}=5V, I_{OUT}=1.0A Ripple Waveform



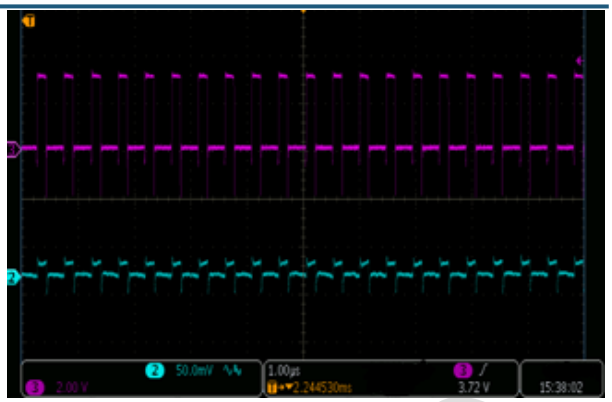
V_{IN}=5V, I_{OUT}=0.5A Ripple Waveform



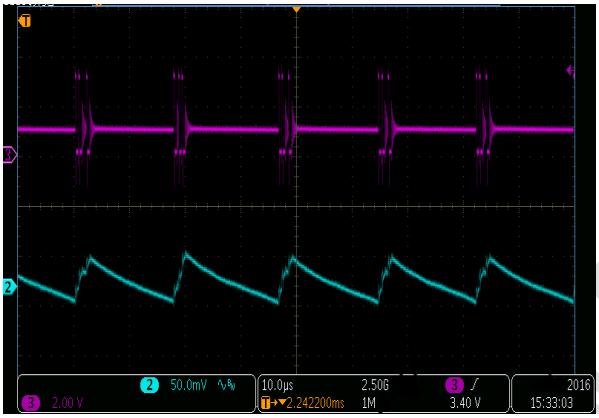
V_{IN}=5V, I_{OUT}=3.0A Ripple Waveform



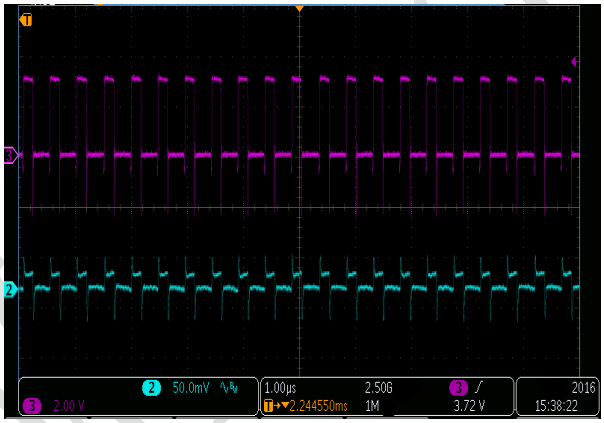
V_{IN}=5V, I_{OUT}=5.0A Ripple Waveform



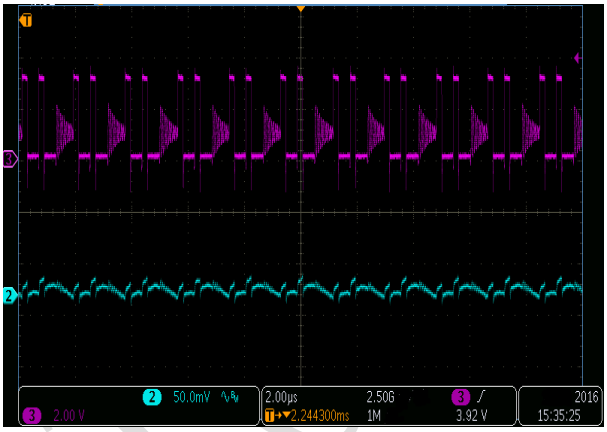
V_{IN}=3.6V, I_{OUT}=3.0A Ripple Waveform



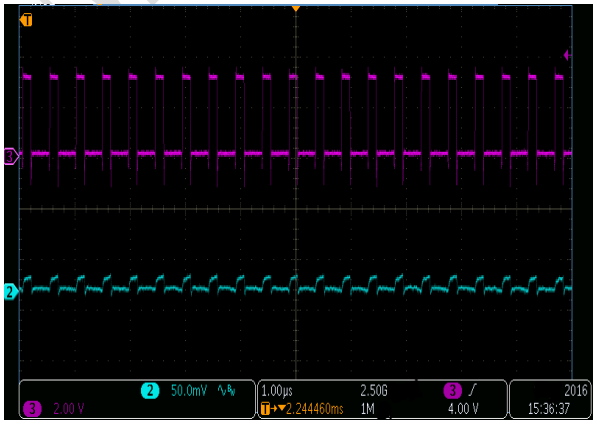
V_{IN}=3.6V, I_{OUT}=0.1A Ripple Waveform



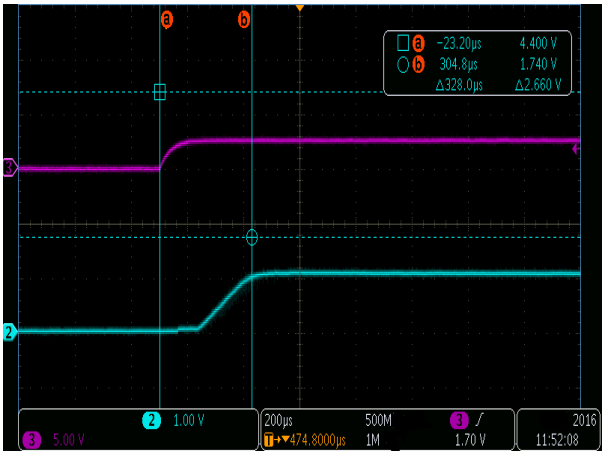
V_{IN}=3.6V, I_{OUT}=5.0A Ripple Waveform



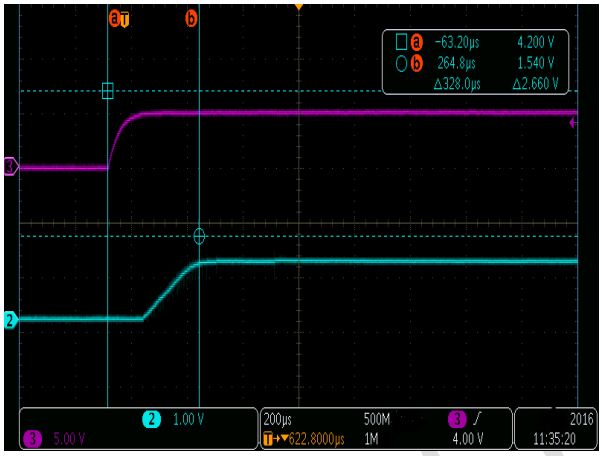
V_{IN}=3.6V, I_{OUT}=0.6A Ripple Waveform



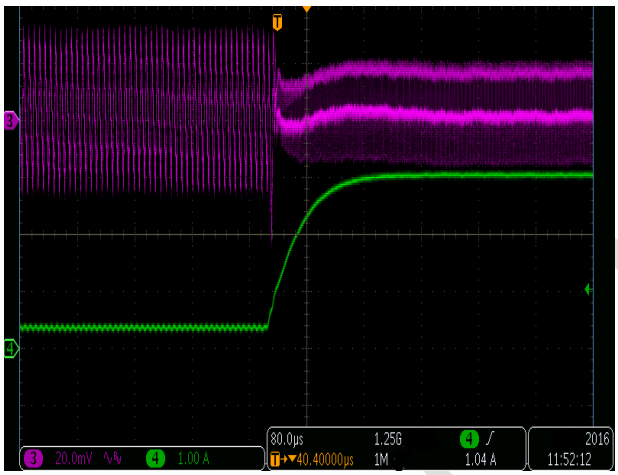
V_{IN}=3.6V, I_{OUT}=1.0A Ripple Waveform



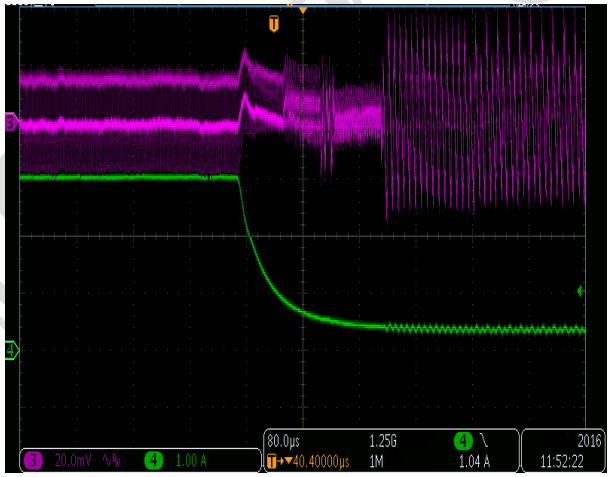
Soft-Start WaveformV_{IN}=2.6V， I_{OUT}=0



Soft-Start Waveform V_{IN}=5.0V， I_{OUT}=0



Load Transient from 0.3A to 3A



Load Transient from 3A to 0.3A

FUNCTIONAL DESCRIPTION

Enable

EN Pin controls chip start. Also STI8070A allows software to enable converter by I2C interface, BUCK_EN0 and BUCK_EN1 bits. The true table is showed as below.

Pins		Bits		
EN	**SEL**	**BUCK_EN0**	**BUCK_EN1**	**OUTPUT**
0	x	x	x	OFF
1	0	0	x	OFF
1	0	1	x	ON
1	1	x	0	OFF
1	1	x	1	ON

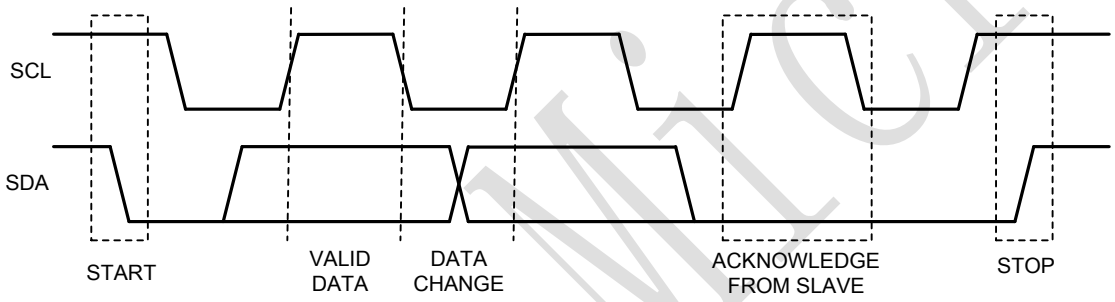
I2C Timing

STI8070A allows the HOST to set the output voltage or other configurable function using an I^2C compatible interface and STI8070A always operates as a SLAVE device. The I^2C

interface supports CLK frequency up to 3.4MHz and all data is transmitted with MSB(bit 7) first. In hex form, the address of STI8070A is 0x80.

STI8070A is addressed using a 7-bit address followed by a direction bit. If the direction bit is 1, the HOST reads data from STI8070A and if the direction bit is 0, the HOST writes data to STI8070A.

A transaction begins with a START condition which is a HIGH to LOW transition of the SDA line while the SCL is HIGH. A transaction ends with a STOP condition which is a LOW to HIGH transition of the SDA line while the SCL is HIGH. The data on the SDA line must stay unchanged when the SCL line is HIGH and vary only when the SCL is LOW, otherwise, STI8070A will consider it as a START or STOP condition. Each transaction contains nine clock pulses. During the ninth pulse, if the SDA line is pulled LOW by STI8070A, it is defined as an acknowledge(ACK) bit, otherwise, it is defined as an NO ACK bit.

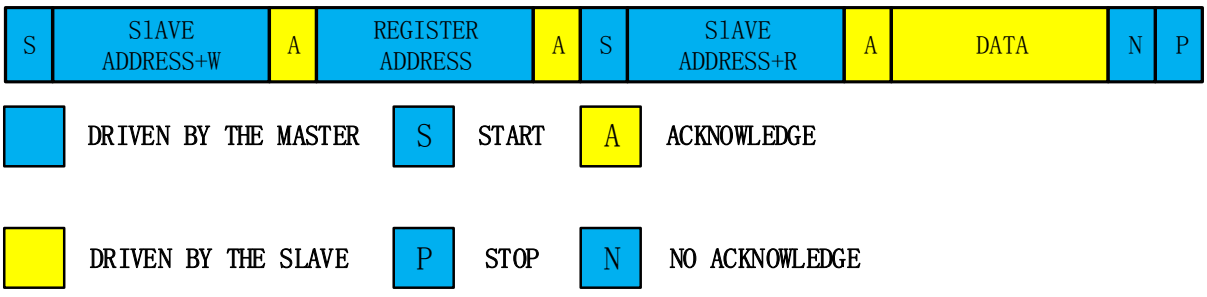


Write period

When the master needs to write data to STI8070A, it generates a START condition followed by the 7-bit address 0x80 and the direction bit 0, STI8070A then acknowledges by pulling SDA LOW during the ninth pulse; the master then transmits register address and the data it needs to write, the operation ends with a STOP condition.

Read period

When the master needs to read data from STI8070A, it generate a START condition followed by the 7-bit address 0x80 and the direction bit 0, the master then transmit register address it needs to read from; after STI8070A acknowledges to the operation, the master issues a START condition again, followed by the 7-bit address 0x80 but the direction bit is modified to 1; the STI8070A then acknowledges and shifts out the data to the master, the master gives NO ACK and ends the operation with a STOP condition.



I²C device Address: 0x80,

1、VSEL0(0x00)

Field	Bit	R/W	Default	Description
BUCK_EN0	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE0	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
VSEL0	5:0	R/W	010111(Vout=1V) (0.720+n*0.0125)	000000 = 0.7200V 000001 = 0.7325V 000010 = 0.7450V …… 010111 = 1.0000V …… 111111 = 1.5000V

2、VSEL1(0x01)

Field	Bit	R/W	Default	Description
BUCK_EN1	7	R/W	1	Software buck enable. When EN pin is low, the regulator is off. When EN pin is high, BUCK_EN bit takes precedent.
MODE1	6	R/W	0	0=Allow auto-PFM mode during light load. 1=Forced PWM mode
VSEL1	5:0	R/W	010111(Vout=1V) (0.720+n*0.0125)	000000 = 0.7200V 000001 = 0.7325V 000010 = 0.7450V …… 010111 = 1.0000V …… 111111 = 1.5000V

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3、Control Register(0x02)

Field	Bit	R/W	Default	Description
Output Discharge	7	R/W	1	0 = discharge resistor is disabled. 1 = discharge resistor is enabled.
Slew Rate	6:4	R/W	000(10mV/0.15uS)	Set the slew rate for positive voltage transitions. 000 = 10mV/0.15us 001 = 10mV/0.3us 010 = 10mV/0.6us 011 = 10mV/1.2us 100 = 10mV/2.4us 101 = 10mV/4.8us 110 = 10mV/9.6us 111 = 10mV/19.2us
reserved	3	R/W	0	Always reads back 0
Reset	2	R/W	0	Setting to 1 resets all registers to default values.
reserved	1:0	R/W	00	Always reads back 0

4、ID1 Register(0x03)

Field	Bit	R/W	Default	Description
VENDOR	7:5	R	101	IC vendor code.
reserved	4	R	0	Always reads back 0
DIE_ID	3:0	R	1101	IC option code

5、ID2 Register(0x04)

Field	Bit	R/W	Default	Description
reserved	7:4	R	0000	Always Reads back 0
DIE_REV	3:0	R	0001	IC mask revision code

6、PGOOD Register(0x05)

Field	Bit	R/W	Default	Description
PGOOD	7	R	0	1: Buck is enabled and soft-start is completed.
reserved	6:0	R	000000	Always reads back 0

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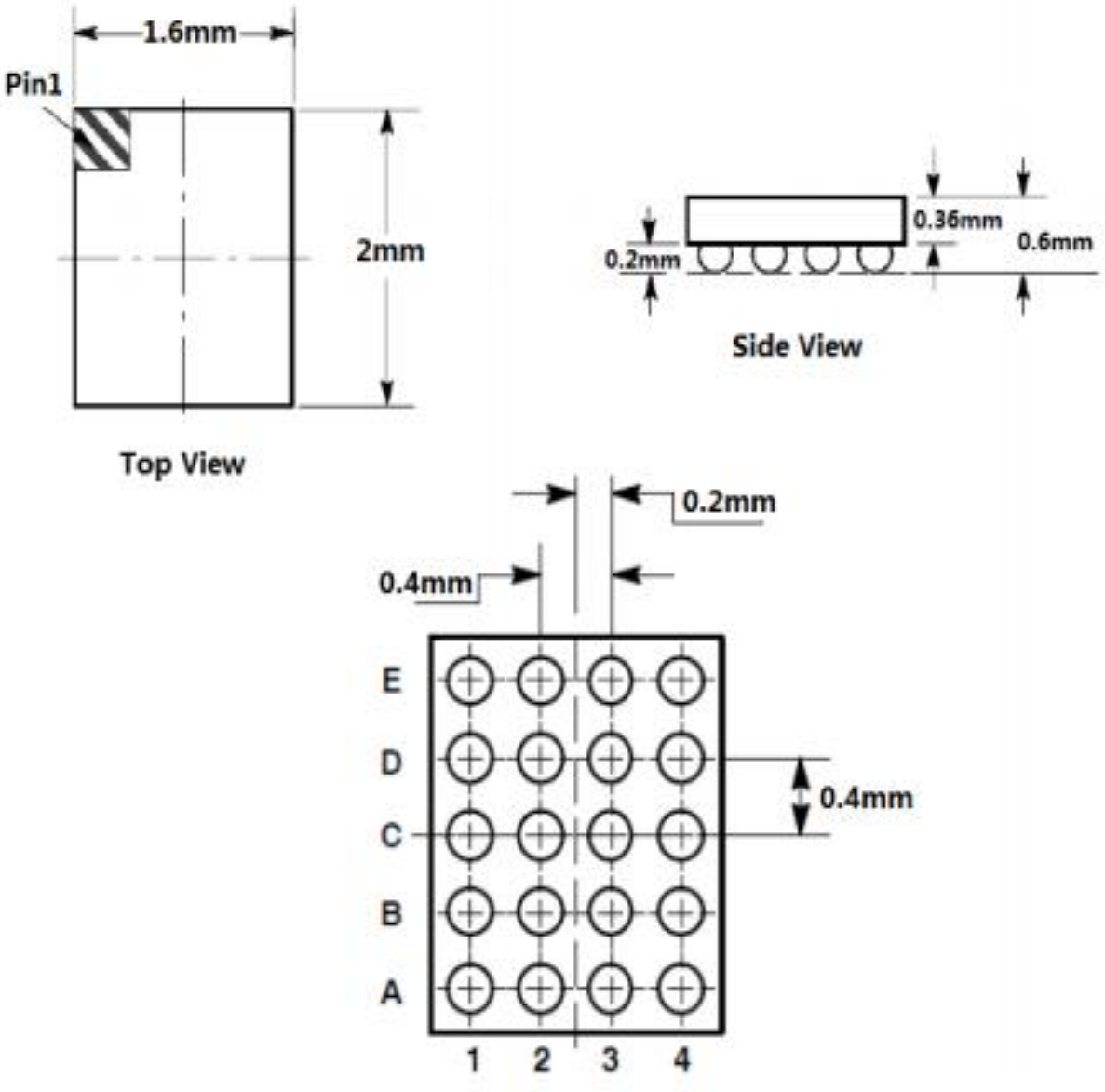
PACKAGE INFORMATION



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Note:

1) All dimensions are in millimeters.

2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.

5) Pin 1 is lower left pin when reading top mark from left to right.