74HC04/74HCT04(文件编号：S&CIC0463)

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection
  HBM EIA/JESD22-A114-A exceeds 2000V
  MM EIA/JESD22-A115-A exceeds 200V
- Specified from –40 to +85℃ and –40 to +125℃

DESCRIPTION

The 74HC04/74HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC04/74HCT04 provide six inverting buffers.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25℃; t_f = t_f≤6.0ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC04	HCT04	
T_{PLH}/t_{PLH}	Propagation delay nA to nY	C_L = 15pF; V_{CC} = 5V	7	8	ns
C_I	Input capacitance		3.5	3.4	pF
C_{PD}	Power dissipation capacitance per gate	Notes 1 and 2	21	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in uW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in volts;
   N = total load switching outputs;
2. For 74HC04: the condition is V_I = GND to V_{CC}.
   For 74HCT04: the condition is V_I = GND to V_{CC}-1.5V

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC04N	–40 to +125℃	14	DIP14	Plastic	SOT27-1
74HCT04N	–40 to +125℃	14	DIP14	Plastic	SOT27-1
74HC04D	–40 to +125℃	14	SO14	Plastic	SOT108-1
74HCT04D	–40 to +125℃	14	SO14	Plastic	SOT108-1
74HC04DB	–40 to +125℃	14	SSOP14	Plastic	SOT337-01
74HCT04DB	–40 to +125℃	14	SSOP14	Plastic	SOT337-01
74HC04PW	–40 to +125℃	14	TSSOP14	Plastic	SOT402-1
74HCT04PW	–40 to +125℃	14	TSSOP14	Plastic	SOT402-1
74HC04BQ	–40 to +125℃	14	DHVQF14	Plastic	SOT762-1
74HCT04BQ	–40 to +125℃	14	DHVQF14	Plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	Data input
2	1Y	Data output
3	2A	Data input
4	2Y	Data output
5	3A	Data input
6	3Y	Data output
7	GND	Ground (0V)
8	4Y	Data output
9	4A	Data input
10	5Y	Data output
11	5A	Data input
12	6Y	Data output
13	6A	Data input
14	VCC	Supply votage

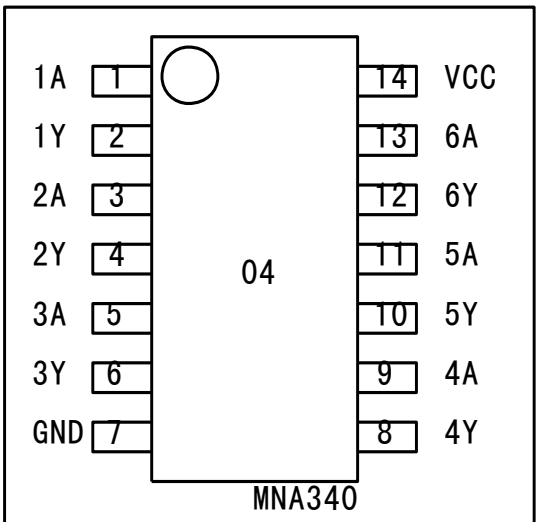
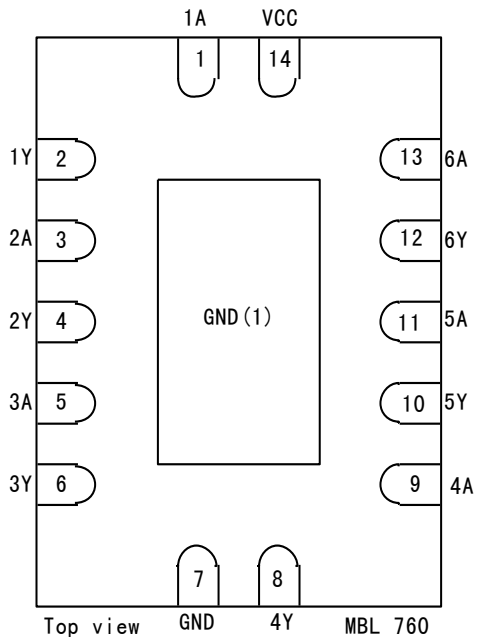


Fig. 1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material.it can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

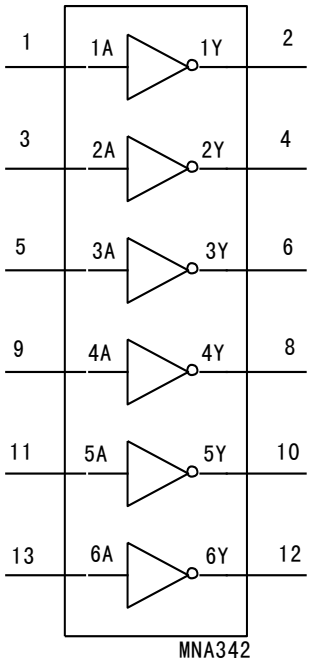


Fig.3 Logic symbol.

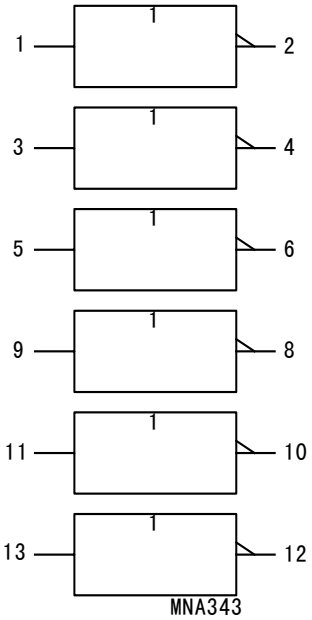


Fig.4 IEC logic symbol.

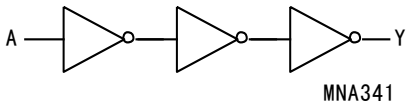


Fig.5 Logic diagram(one inverter).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC04			74HCT04			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VCC	Supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	Input voltage		0	-	Vcc	0	-	Vcc	V
VO	Output voltage		0	-	Vcc	0	-	Vcc	V
Tamb	Ambient temperature	See DC and AC Characteristics per Device	-40	+25	+125	-40	+25	+125	℃
tr, tf	Input rise and fall times	Vcc = 2.0V	-	-	1000	-	-	-	ns
		Vcc = 4.5V	-	6.0	500	-	6.0	500	ns
		Vcc = 6.0V	-	-	400	-	-	-	ns

LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 60134); voltages are referenced to GND (fround = 0V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX
Vcc	Suupply voltage		-0.5	+7.0	V
I_{IK}	Input diode current	V_I<-0.5V<or V_I<Vcc+0.5V	-	±20	mA
I_{OK}	Output diode currer	V_O<-0.5V<or V_O<Vcc+0.5V	-	±20	mA
I_O	Output source of sink current	-0.5V<V_O<Vcc+0.5V	-	±25	mA
Icc, I_{GND}	Vcc or GND currer		-	±50	mA
T_{stg}	Storage temperature		-65	±150	℃
P_{tot}	Power dissipation				
	DIP 14 package	T_{amb} = -40 to +125℃; note 1	-	750	mW
	Other packages	T_{amb} = -40 to +125℃; note 2	-	500	mW

Notes

1. For DIP14 packages: above 70℃ derate linearly with 12 mW/K.
2. For SO14 packages: above 70℃ derate linearly with 8 mW/K.
   For SSOP14 and TSSOP14 packages: above 60℃ derate linearly with 5.5mW/K.
   For DHVQFN14 packages: above 60℃ derate linearly with 4.5mW/K.

DC CHARACTERISTICS

Type 74HC04

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		OTHER	Vcc (V)				
T_{amb} = 25℃							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	-	V
			4.5	3.15	2.4	-	V
			6.0	4.2	3.2	-	V
V_{IL}	LOW-level input voltage		2.0	-	0.8	0.5	V
			4.5	-	2.1	1.35	V
			6.0	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20uA	2.0	1.9	2.0	-	V
		I_O = -20uA	4.5	4.4	4.5	-	V
		I_O = -4.0mA	4.5	3.98	4.32	-	V
		I_O = -20uA	6.0	5.9	6.0	-	V
		I_O = -5.2mA	6.0	5.48	5.81	-	V
V_{OL}	LOW-level output voltage						
		I_O =20uA	2.0	-	0	0.1	V
		I_O =20uA	4.5	-	0	0.1	V
		I_O =4.0uA	4.5	-	0.15	0.26	V
		I_O =20uA	6.0	-	0	0.1	V
		I_O =5.2uA	6.0	-	0.16	0.26	V
I_{LI}	Input leakage current	V_I = Vcc or GND	6.0	-	0.1	±0.1	uA
I_{OZ}	3-state output OFF current	V_I = VIH or VIL; V_O = Vcc or GND	6.0	-	-	±0.5	uA
Icc	Quiescent supply current	V_I = Vcc or GND; I_O = 0	6.0	-	-	2	uA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		OTHER	Vcc (V)				
T_{amb} = -40 to +85℃							
V_{IH}	HIGH-level input voltage		2.0	1.5	-	-	V
			4.5	3.15	-	-	V
			6.0	4.2	-	-	V
V_{IL}	LOW-level input voltage		2.0	-	-	0.5	V
			4.5	-	-	1.35	V
			6.0	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20uA	2.0	1.9	-	-	V
		I_O = -20uA	4.5	4.4	-	-	V
		I_O = -4.0mA	4.5	3.84	-	-	V
		I_O = -20uA	6.0	5.9	-	-	V
		I_O = -5.2mA	6.0	5.34	-	-	V
V_{OL}	LOW-level output voltage						
		I_O =20uA	2.0	-	-	0.1	V
		I_O =20uA	4.5	-	-	0.1	V
		I_O =4.0uA	4.5	-	-	0.33	V
		I_O =20uA	6.0	-	-	0.1	V
		I_O =5.2uA	6.0	-	-	0.33	V
I_{LI}	Input leakage current	V_I = Vcc or GND	6.0	-	-	±0.1	uA
I_{OZ}	3-state output OFF current	V_I = VIH or VIL; V_O = Vcc or GND	6.0	-	-	±5.0	uA
Icc	Quiescent supply current	V_I = Vcc or GND; I_O = 0	6.0	-	-	20	uA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		OTHER	Vcc (V)				
T_{amb} = -40 to +125℃							
V_{IH}	HIGH-level input voltage		2.0	1.5	-	-	V
			4.5	3.15	-	-	V
			6.0	4.2	-	-	V
V_{IL}	LOW-level input voltage		2.0	-	-	0.5	V
			4.5	-	-	1.35	V
			6.0	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20uA	2.0	1.9	-	-	V
		I_O = -20uA	4.5	4.4	-	-	V
		I_O = -20 uA	6.0	5.9	-	-	V
		I_O = -4.0mA	4.5	3.7	-	-	V
		I_O = -5.2mA	6.0	5.2	-	-	V
V_{OL}	LOW-level output voltage						
		I_O =20uA	2.0	-	-	0.1	V
		I_O =20uA	4.5	-	-	0.1	V
		I_O =20uA	6.0	-	-	0.1	V
		I_O =4.0uA	4.5	-	-	0.4	V
		I_O =5.2uA	6.0	-	-	0.4	V
I_{LI}	Input leakage current	V_I = Vcc or GND	6.0	-	-	±1.0	uA
I_{OZ}	3-state output OFF current	V_I = VIH or VIL; V_O = Vcc or GND	6.0	-	-	±10.0	uA
Icc	Quiescent supply current	V_I = Vcc or GND; I_O = 0	6.0	-	-	40	uA

Type 74HCT04

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		OTHER	Vcc (V)				
T_{amb} = 25℃							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	-	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20 uA	4.5	4.4	4.5	-	V
		I_O = -4.0mA	4.5	3.84	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 uA	4.5	-	0	0.1	V
		I_O = 4.0mA	4.5	-	0.15	0.26	V
I_{LI}	Input leakage current	V_I = Vcc or GND	5.5	-	-	±0.1	uA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}	5.5	-	-	±0.5	uA
		V_I = Vcc or GND					
		I_O = 0					
Icc	Quiescent supply current	V_I = Vcc or GND	5.5	-	-	2	uA
		I_O = 0					
△Icc	Abbitional supply current per input	V_I = Vcc –2.1V	4.5 to 5.5	-	120	432	uA
		I_O = 0					
T_{amb} = -40 to +85℃							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	-	-	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20 uA	4.5	4.4	-	-	V
		I_O = -4.0mA	4.5	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 uA	4.5	-	-	0.1	V
		I_O = 4.0mA	4.5	-	-	0.33	V
I_{LI}	Input leakage current	V_I = Vcc or GND	5.5	-	-	±1.0	uA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}	5.5	-	-	±5.0	uA
		V_I = Vcc or GND					
		I_O = 0					
Icc	Quiescent supply current	V_I = Vcc or GND I_O = 0	5.5	-	-	20	uA
△Icc	Abbitional supply current per input	V_I = Vcc –2.1V I_O = 0	4.5 to 5.5	-	-	540	uA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		OTHER	Vcc (V)				
T_{amb} = -40 to +125℃							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	-	-	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = -20 uA	4.5	4.4	-	-	V
		I_O = -4.0mA	4.5	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 uA	4.5	-	-	0.1	V
		I_O = 4.0mA	4.5	-	-	0.4	V
I_{LI}	Input leakage current	V_I = Vcc or GND	5.5	-	-	±1.0	uA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}	5.5	-	-	±10	uA
		V_I = Vcc or GND					
		I_O = 0					
Icc	Quiescent supply current	V_I = Vcc or GND	5.5	-	-	40	uA
		I_O = 0					
△Icc	Abbitional supply current per input	V_I = Vcc –2.1V	4.5 to 5.5	-	-	590	uA
		I_O = 0					

AC CHARACTERISTICS

Family 74HC04

GND = 0V; $t_r=t_f \leqslant 6.0ns$; $C_L = 50pF$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		WAVEFORMS	Vcc (V)				
T_{amb} = 25℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	2.0	-	25	85	ns
			4.5	-	9	17	ns
			6.0	-	7	14	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	2.0	-	19	75	ns
			4.5	-	7	15	ns
			6.0	-	6	13	ns
T_{amb} = -40 to +85℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	2.0	-	-	105	ns
			4.5	-	-	21	ns
			6.0	-	-	18	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	2.0	-	-	95	ns
			4.5	-	-	19	ns
			6.0	-	-	16	ns
T_{amb} = -40 to +125℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	2.0	-	-	130	ns
			4.5	-	-	26	ns
			6.0	-	-	22	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	2.0	-	-	110	ns
			4.5	-	-	22	ns
			6.0	-	-	19	ns

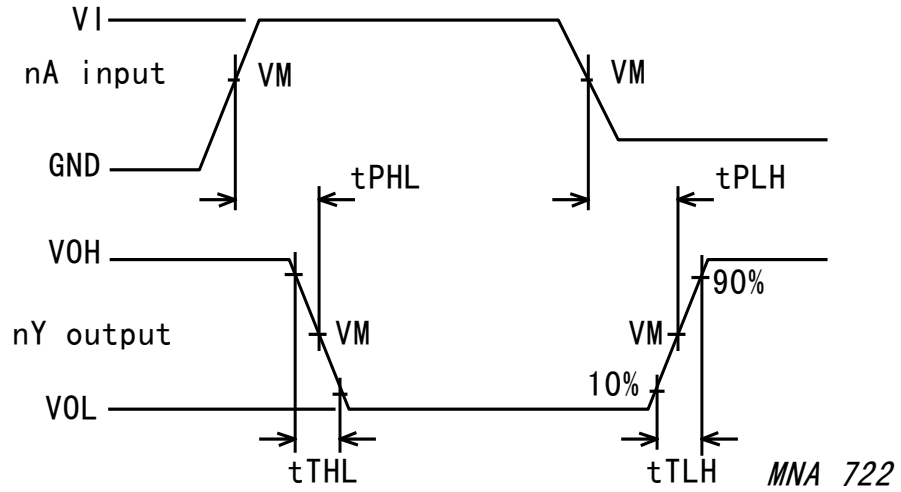
74HC04/74HCT04(文件编号：S&CIC0463)

Family 74HCT04

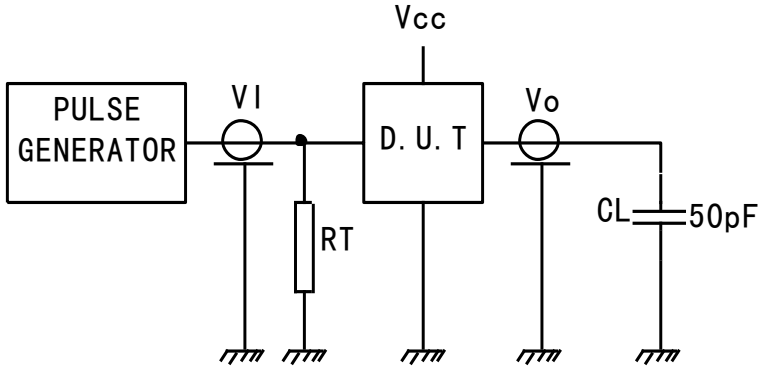
GND = 0V; $t_r=t_f \leqslant 6.0$ns; C_L = 50pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		WAVEFORMS	Vcc (V)				
T_{amb} = 25℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	4.5	-	10	19	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	4.5	-	7	15	ns
T_{amb} = -40 to +85℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	4.5	-	-	24	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	4.5	-	-	19	ns
T_{amb} = -40 to +125℃							
t_{PHL}/t_{PLH}	Propagation delay nA to nY	See figs 6 and 7	4.5	-	-	29	ns
t_{THL}/t_{TLH}	Output transition time	See figs 6 and 7	4.5	-	-	22	ns

AC WAVEFORMS



For 74HC04: VM=50%; VI=GND to VCC.
For 74HCT04: VM=1.3V; VI=GND to 3.0V.
Fig.6 Waveforms showing the data input(nA) to data output (nY) propagation delays and the output transition times.

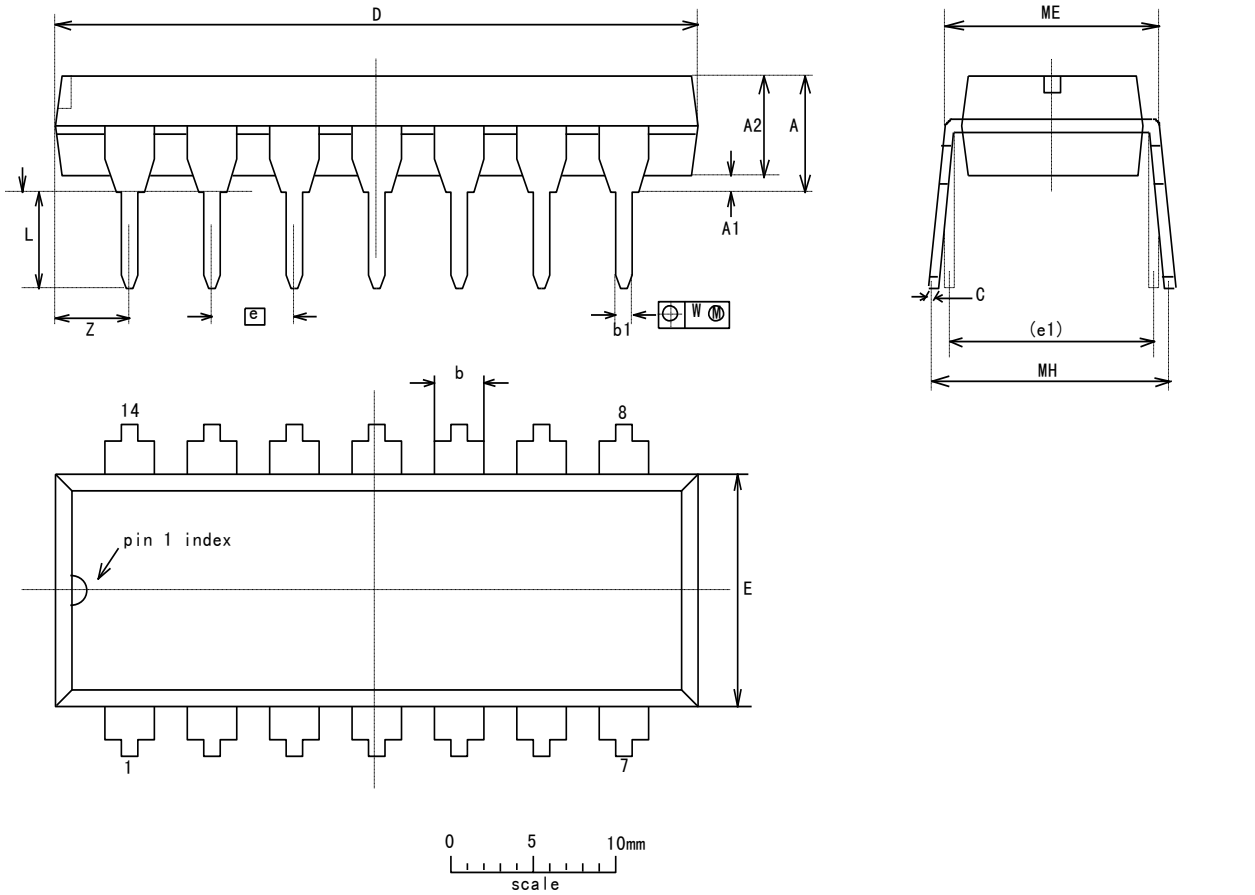


Definitions for test circuit:
CL=Load capacitance including jig
and probe capacitance.
Rt=Termination resistance ahould be equal to the output
impedance Zo of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

DIP 14: plastic dual in-line package; 14 leads (300 minl) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max	A1 min	A2 max	b	B1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	W	$Z^{(1)}$ max
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

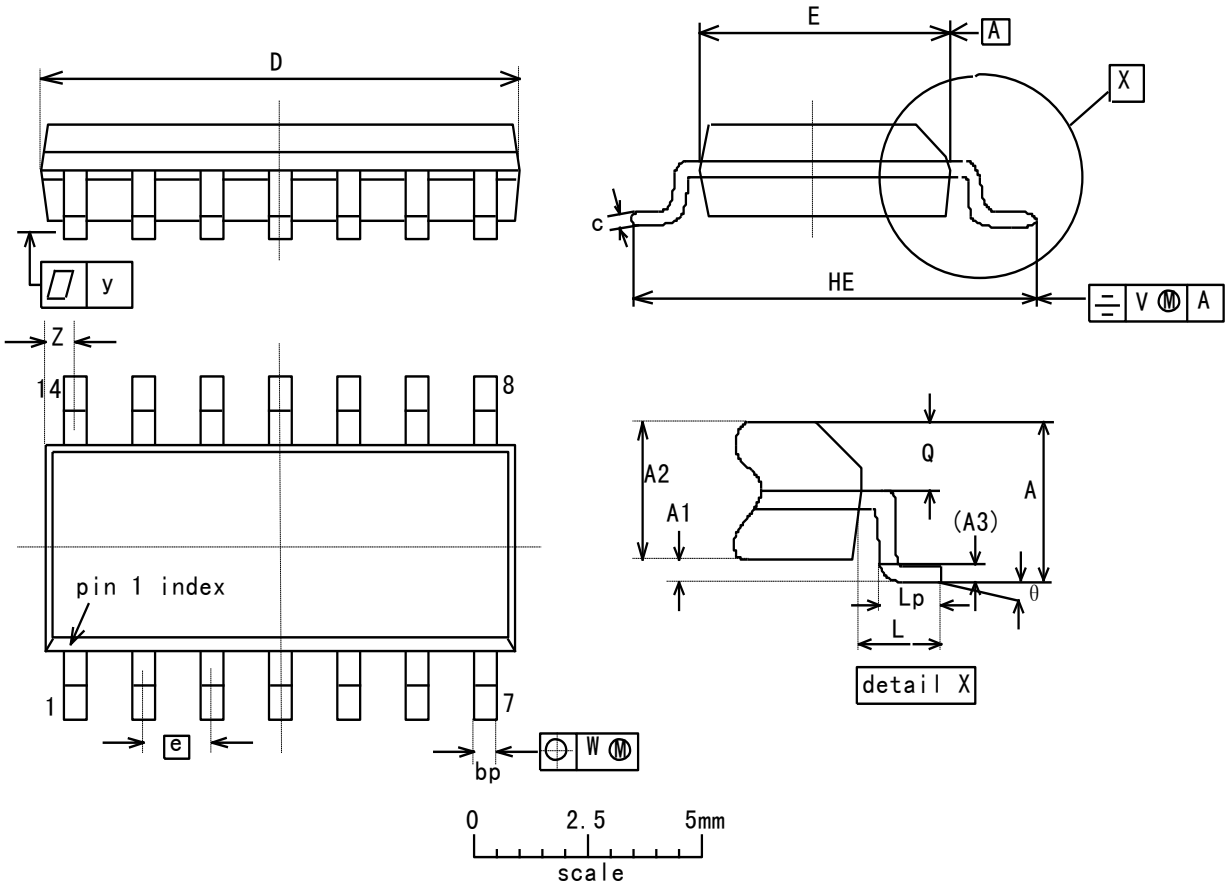
Note

1. Plastic or metal protrusions of 0.25mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-201-14			~~99-12-27~~ 03-02-13

74HC04/74HCT04(文件编号：S&CIC0463)

SO14: plastic small outline package; 14 leads; body width 3.9mm **SOT108-1**

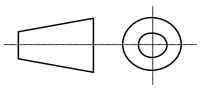


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max	A1	A2	A3	bp	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	Lp	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

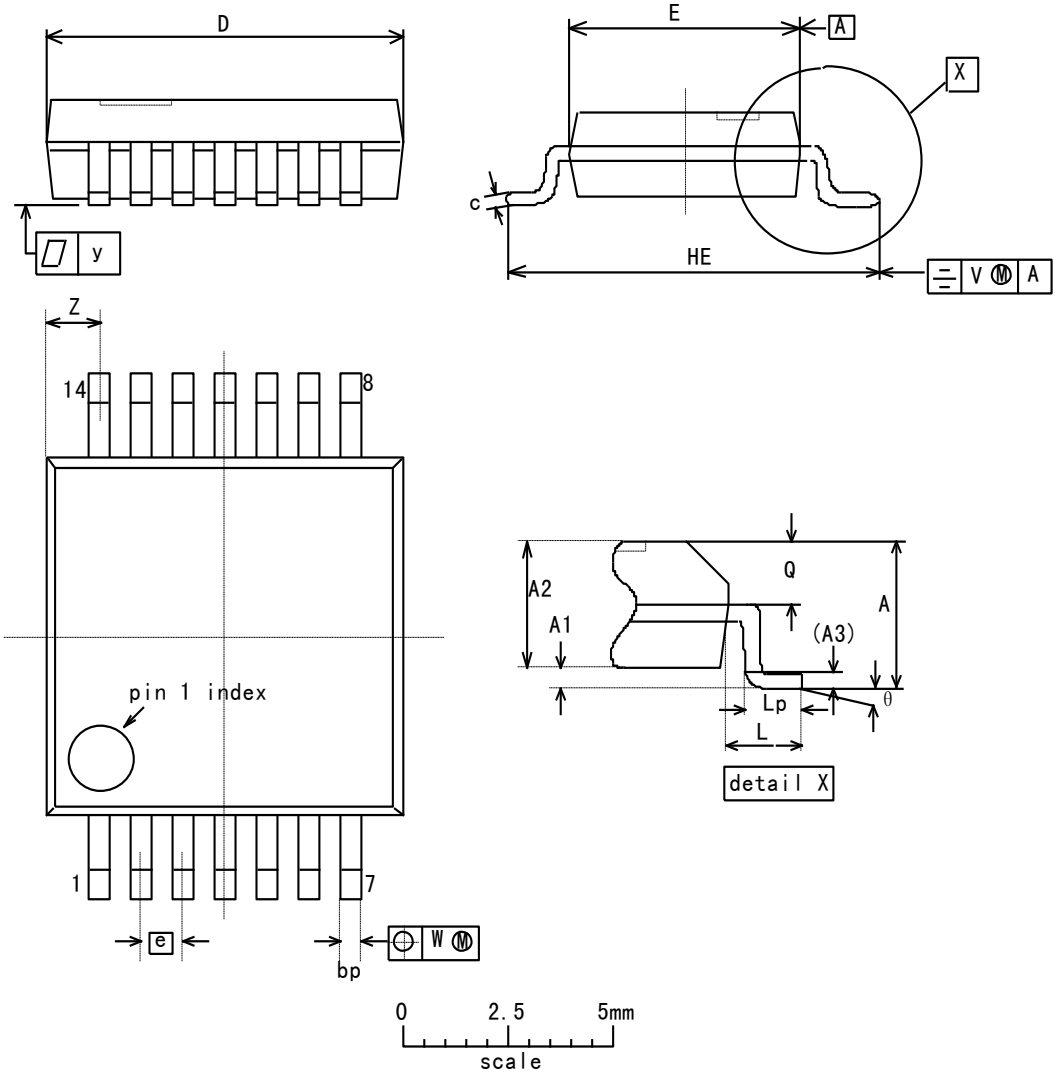
Note

1. Plastic or metal protrusions of 0.15mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012	SC-201-14			~~99-12-27~~ 03-02-19

74HC04/74HCT04(文件编号：S&CIC0463)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3mm **SOT337-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max	A1	A2	A3	bp	c	D(1)	E(1)	e	H_E	L	Lp	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

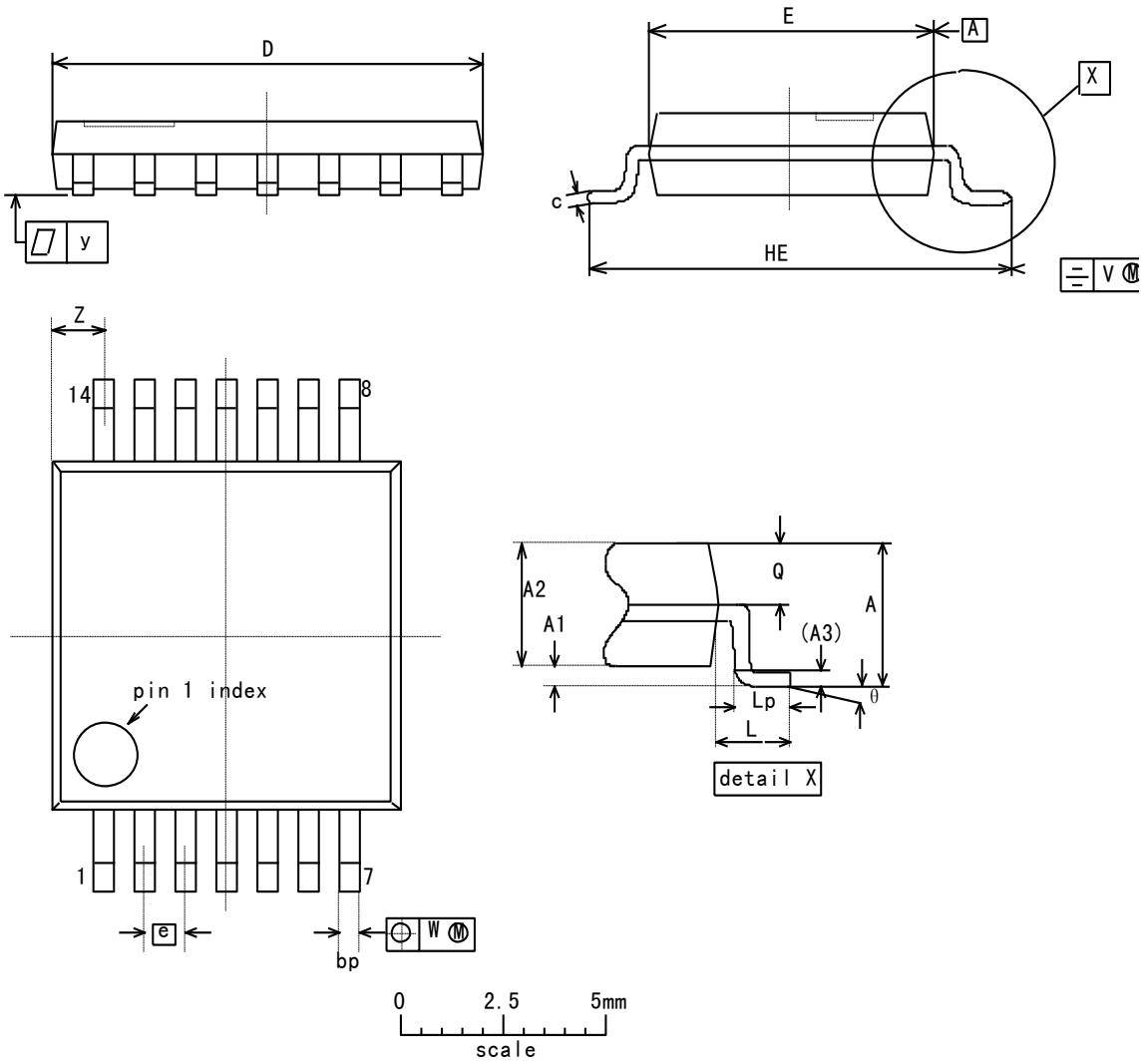
Note

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

74HC04/74HCT04(文件编号：S&CIC0463)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4mm **SOT402-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max	A1	A2	A3	bp	c	D(1)	E(1)	e	H_E	L	Lp	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

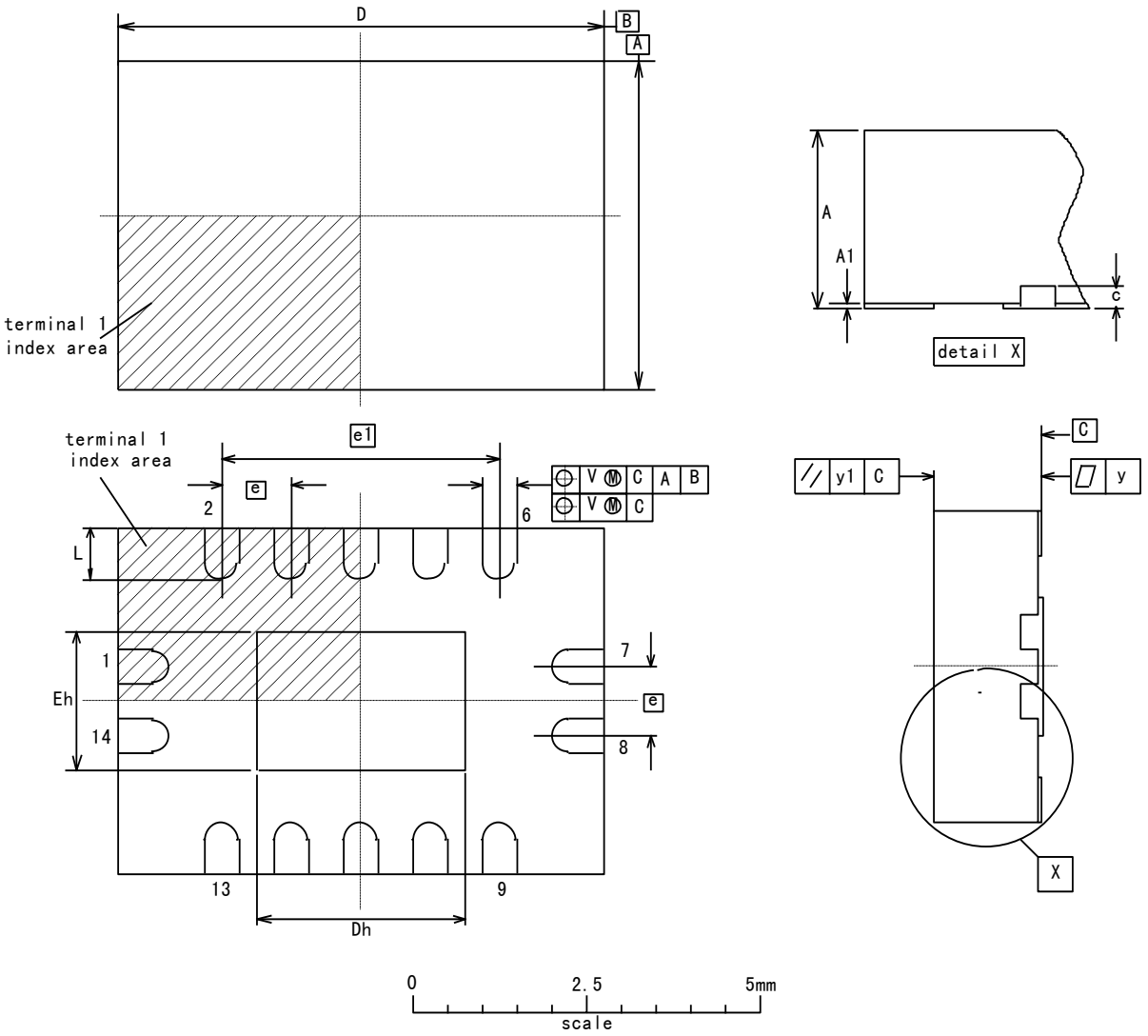
Note: 1. Plastic or metal protrusions of 0.15mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

74HC04/74HCT04(文件编号：S&CIC0463)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5×3×0.85mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e1	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38

Note: 1. Plastic or metal protrusions of 0.075mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			~~02-10-17~~ 03-01-27

74HC04/74HCT04(文件编号：S&CIC0463)

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product Development.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date.
III	Product data	Production	This data sheet contains data from the product specification.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

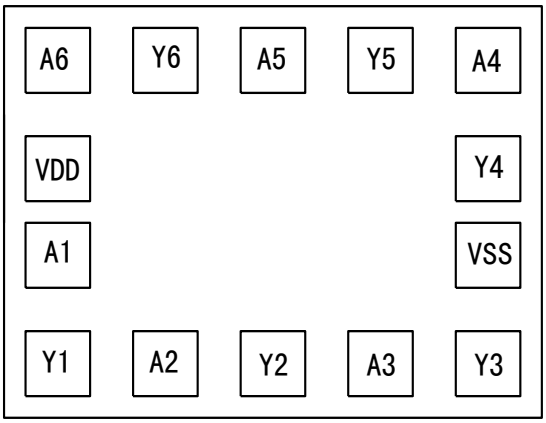
DEFINITIONS

Short-form specification-The data in a short-from specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook

Limiting values definition-Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information-Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

PAD ASSIGNMENT



Pad No	Pad Name	X	Y
1	A1	-243.00	-48.00
2	Y1	-243.00	-182.00
3	A2	-122.50	-182.00
4	Y2	7.50	-182.00
5	A3	112.50	-182.00
6	Y3	242.50	-182.00
7	VSS	230.50	-57.50
8	Y4	242.50	47.50
9	A4	242.50	181.50
10	Y5	122.00	181.50
11	A5	-8.00	181.50
12	Y6	-113.00	181.50
13	A6	-243.00	181.50
14	VDD	-243.00	57.00