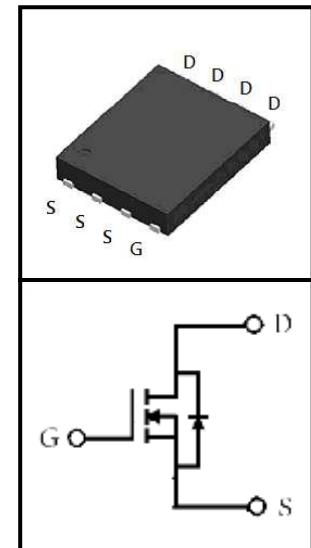


30V N-Channel Split Gate Trench MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



RoHS

APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

Device Marking and Package Information

Device	Package	Marking
CSN03N3P9	DFN5*6	CSN03N3P9

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	30	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	60	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		42	A
Pulsed Drain Current (note2)	I_{DM}	200	A
Gate Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note3)	E_{AS}	44	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	48	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-Case (note1)	$R_{\theta JC}$	2.6	$^\circ\text{C/W}$
Thermal Resistance, Junction-Ambient (note1)	$R_{\theta JA}$	62	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 25^\circ\text{C}$	--	--	1	uA
		$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 55^\circ\text{C}$	--	--	5	uA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.0	1.5	2.5	V
Drain-Source On-Resistance (note2)	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$	--	3.4	3.9	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$	--	4.7	6.1	$\text{m}\Omega$
Dynamic						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1.0\text{MHz}$	--	1320	--	pF
Output Capacitance	C_{oss}		--	610	--	
Reverse Transfer Capacitance	C_{rss}		--	56	--	
Gate Resistance	R_g	$f = 1.0\text{MHz}$	--	2.5	--	Ω
Total Gate Charge	Q_g	$V_{\text{DD}} = 24\text{V}, I_D = 30\text{A}, V_{\text{GS}} = 10\text{V}$	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	4	--	
Gate-Drain Charge	Q_{gd}		--	4.5	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DS}} = 15\text{V}, I_D = 30\text{A}, V_{\text{GS}} = 10\text{V}, R_G = 3.0\Omega$	--	9	--	ns
Turn-on Rise Time	t_r		--	4.5	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	29	--	
Turn-off Fall Time	t_f		--	12	--	
Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	60	A
Pulsed Diode Forward Current	I_{SM}		--	--	200	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 30\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 30\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$	--	16	--	nS
Reverse Recovery Charge	Q_{rr}		--	35	--	nC

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}} = 15\text{V}, V_{\text{GS}} = 10\text{V}, L = 0.5\text{mH}, R_g = 25\Omega$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

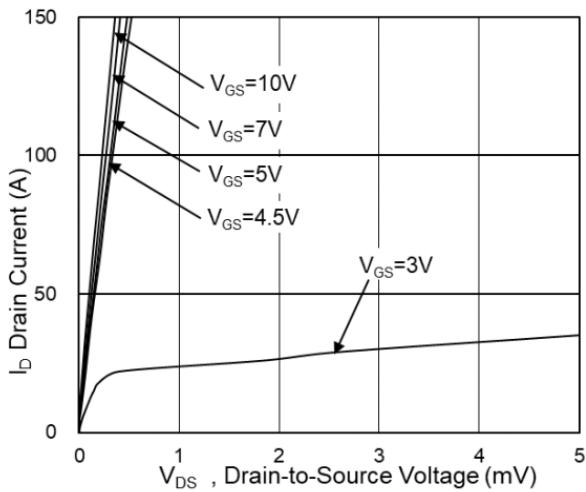


Fig.1 Typical Output Characteristics

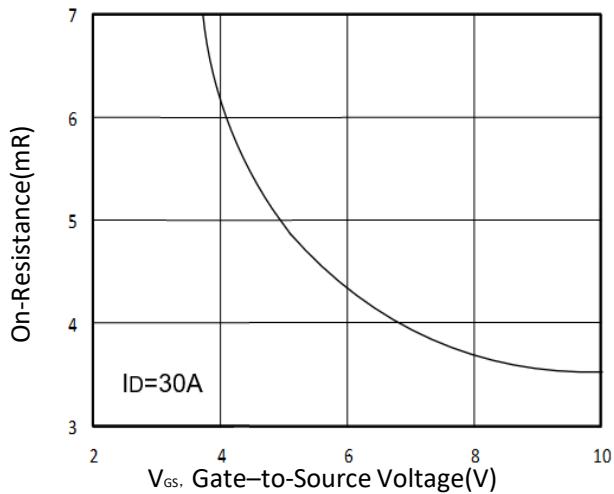


Fig.2 On-Resistance vs. G-S Voltage

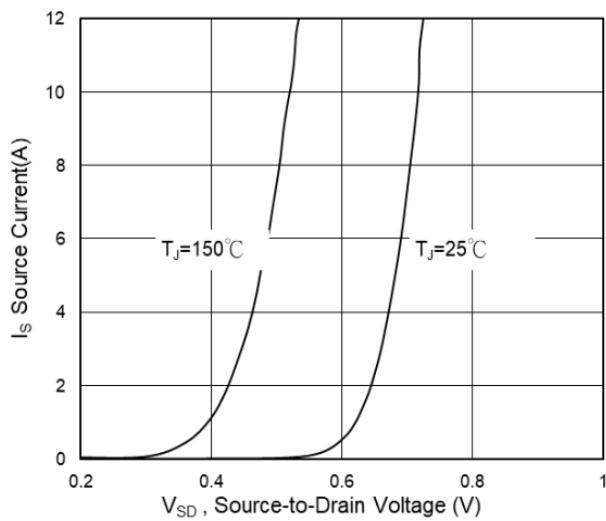


Fig.3 Source Drain Forward Characteristics

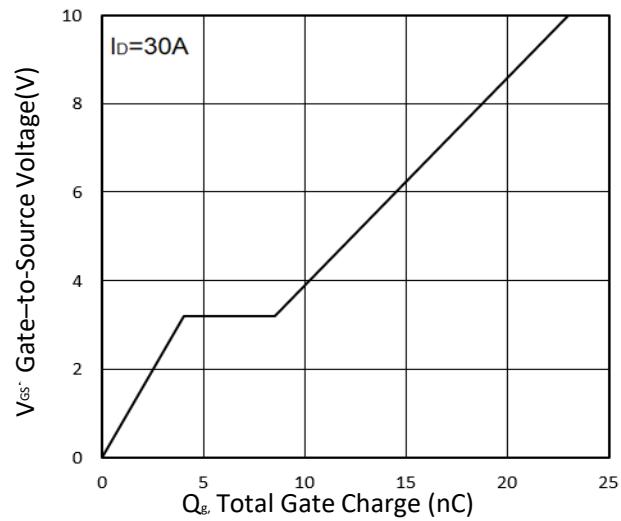


Fig.4 Gate-Charge Characteristics

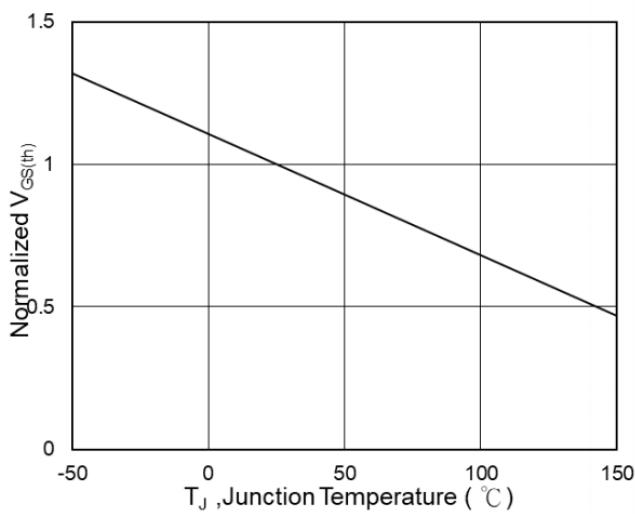


Fig.5 Normalized $V_{GS}(\text{th})$ vs. T_J

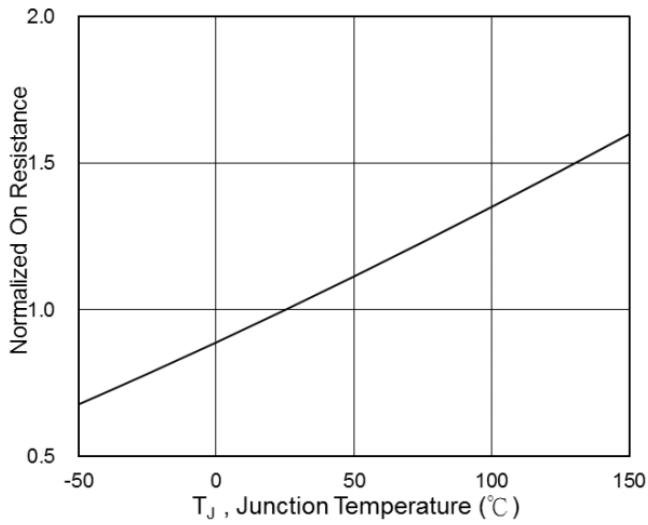


Fig.6 Normalized R_{DSON} vs. T_J

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

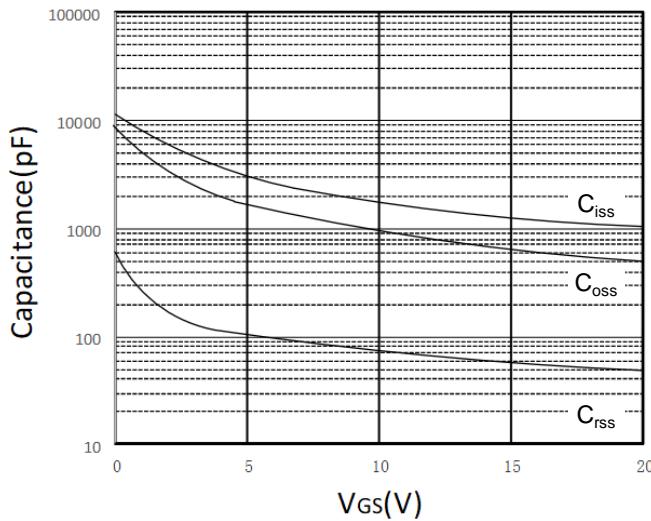


Fig.7 Capacitance

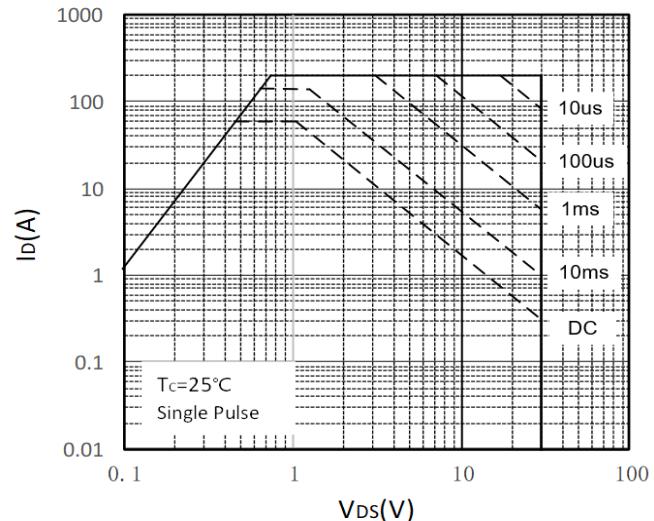


Fig.8 Safe Operating Area

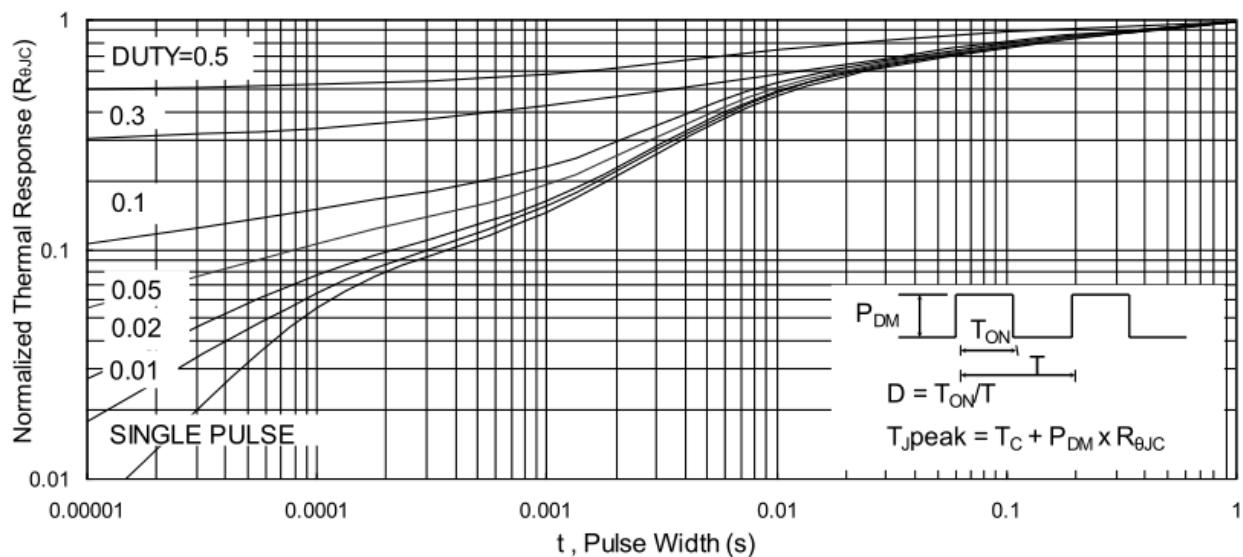
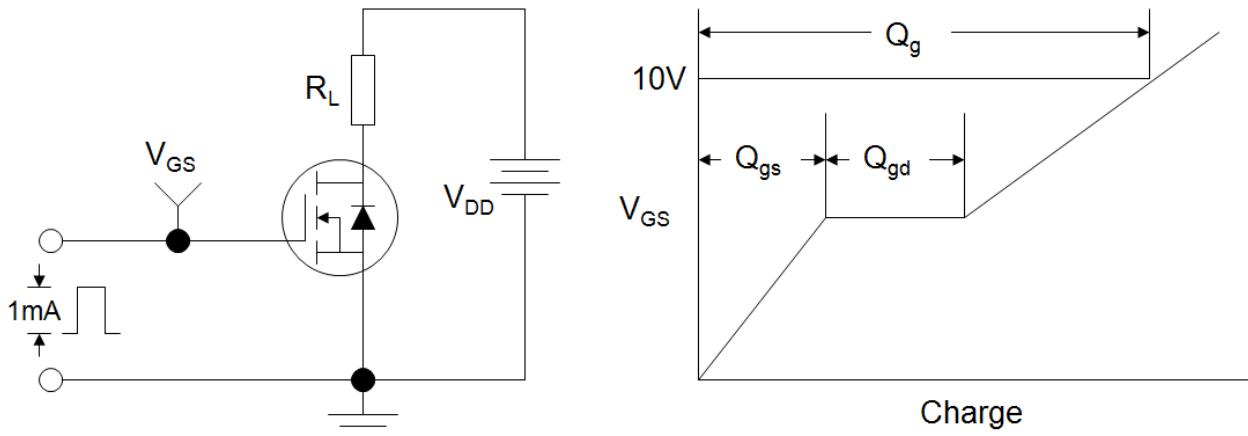
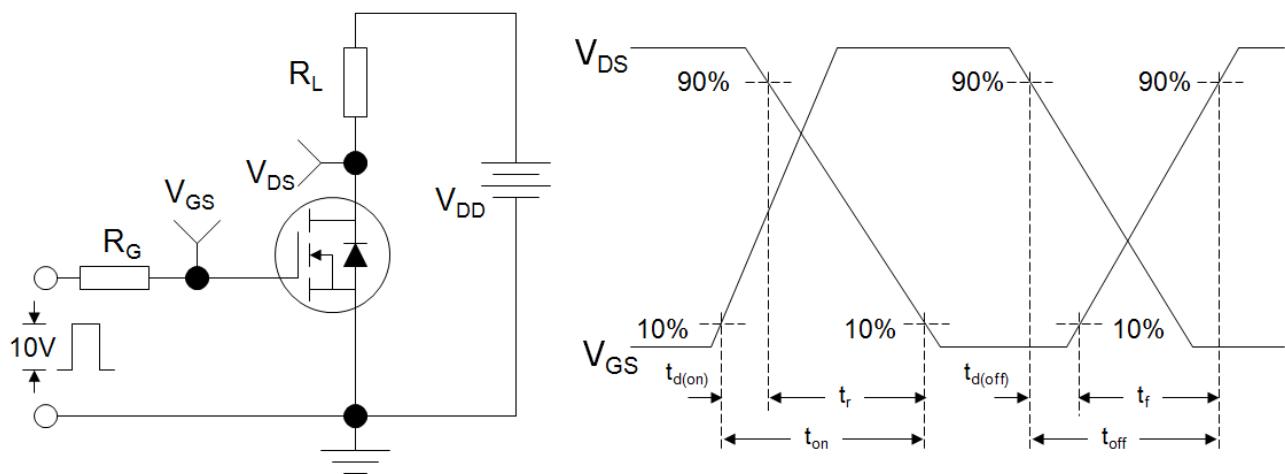
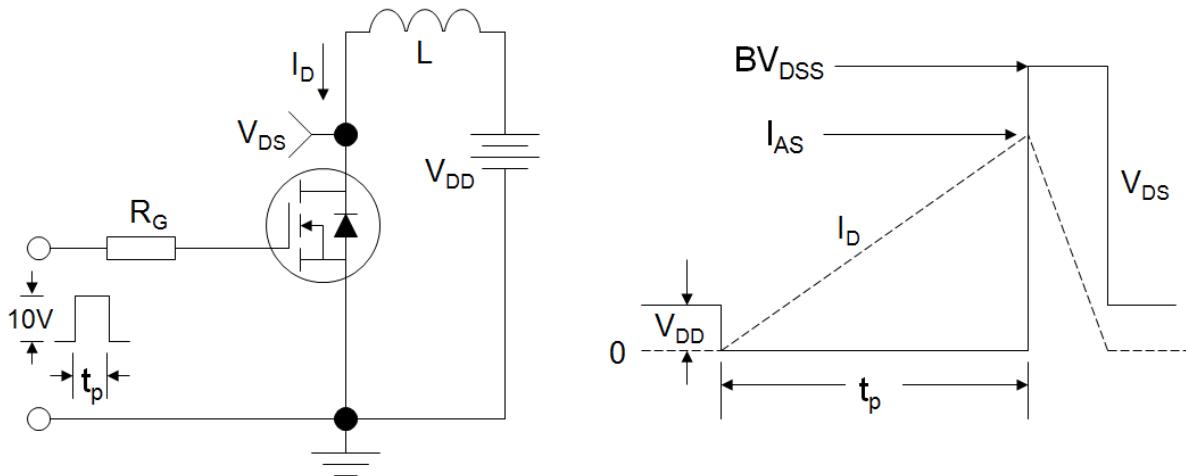
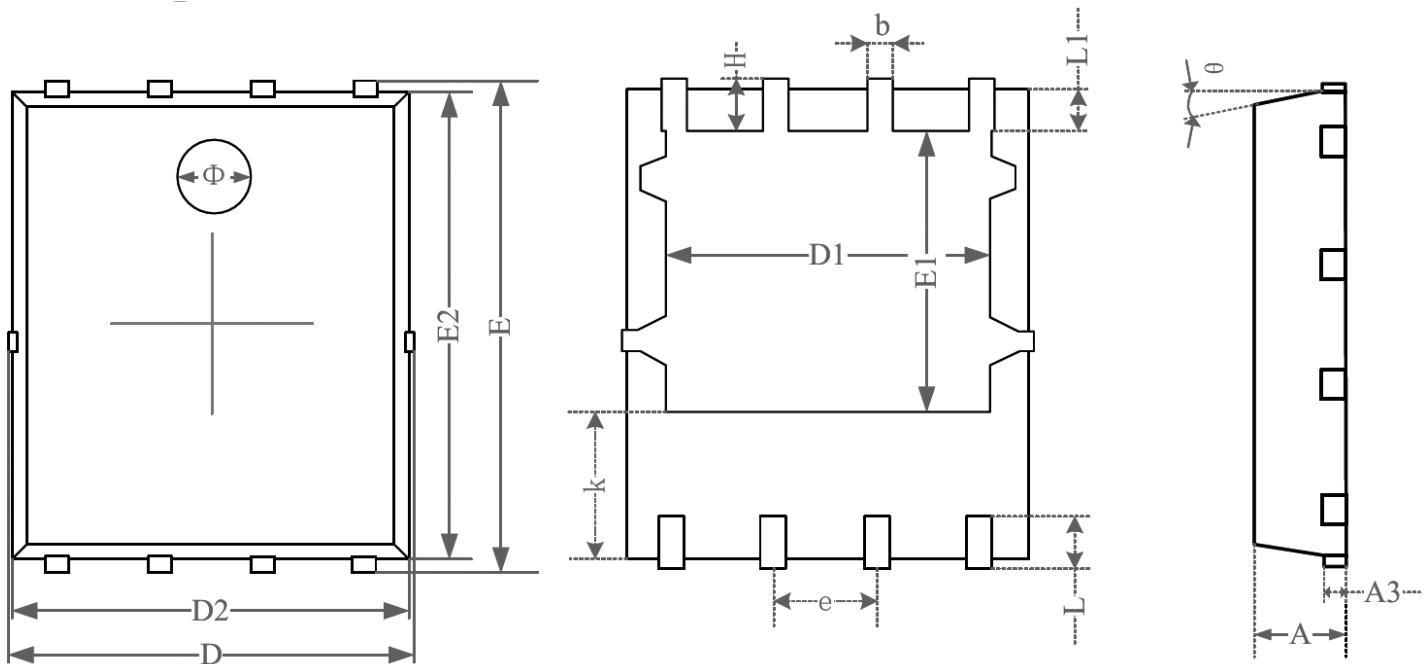


Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


DFN5*6



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.870	0.900	0.930	0.034	0.035	0.036	
A3	0.152REF.			0.006REF.			
D	4.944	5.020	5.096	0.195	0.198	0.201	
E	5.974	6.050	6.126	0.235	0.238	0.241	
D1	3.910	4.010	4.110	0.154	0.158	0.162	
E1	3.375	3.475	3.575	0.133	0.137	0.141	
D2	4.870	4.900	4.930	0.192	0.193	0.194	
E2	5.720	5.750	5.780	0.226	0.227	0.228	
k	1.190	1.290	1.390	0.047	0.051	0.055	
b	0.350	0.380	0.410	0.014	0.015	0.016	
e	1.270TYP.			0.050TYP.			
L	0.559	0.635	0.711	0.022	0.025	0.028	
L1	0.424	0.500	0.576	0.017	0.020	0.023	
H	0.574	0.650	0.726	0.023	0.026	0.029	
θ	10°	11°	12°	10°	11°	12°	
Φ	1.150	1.200	1.250	0.045	0.047	0.049	

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