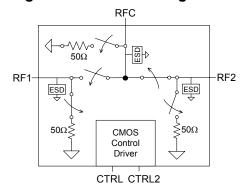


## **Product Description**

The PE4257 is a high-isolation UltraCMOS™ Switch designed for wireless applications, covering a broad frequency range from near DC up to 3000 MHz. This single-supply SPDT switch integrates a two-pin CMOS control interface. It also provides low insertion loss with extremely low bias requirements while operating on a single 3-volt supply. In a typical wireless application, the PE4257 provides unprecedented isolation and integration.

The PE4257 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram



# **Product Specification**

## PE4257

# 50 Ω SPDT Absorptive UltraCMOS™ DC – 3.0 GHz RF Switch

#### **Features**

- 50 Ω characteristic impedance
- Integrated 50 Ω 0.25 watt terminations
- High input IP3 > +55 dBm
- High isolation 64 dB at 1000 MHz
- Low insertion loss: typically 0.75 dB at 1000 MHz and 0.95 dB at 2000 MHz
- LV CMOS two-pin control
- Single +3 volt supply operation
- Low current consumption: 8 μA

Figure 2. Package Type

20-Lead 4x4 mm QFN



Table 1. Electrical Specifications @ +25 °C,  $V_{DD}$  = 3.0 V ( $Z_S$  =  $Z_L$  = 50  $\Omega$ )

Parameter	Condition	Minimum	Typical	Maximum	Units
Operating Frequency <sup>1</sup>		DC		3000	MHz
Insertion Loss	1000 MHz 2000 MHz 3000 MHz		0.75 0.95 1.2	0.95 1.15 1.4	dB
Isolation Input to Output	1000 MHz 2000 MHz 3000 MHz	61 46 40	64 50 44		dB
Isolation Output to Output	1000 MHz 2000 MHz 3000 MHz	57 54 42	63 60 48		dB
Input IP2	5 MHz - 1000 MHz		80		dBm
Input IP3	5 MHz - 1000 MHz	50	55		dBm
Input 1dB Compression <sup>2</sup>	1000 MHz	29	31		dBm
Switching Time	50% CTRL to 10 / 90 RF		2		μs
Video Feedthrough <sup>3</sup>	5 MHz - 1000 MHz			15	$mV_{pp}$

Notes: 1. Device linearity will begin to degrade below 5 MHz.

- 2. Note Absolute Maximum ratings in Table 3.
- 3. Measured with a 1 ns risetime, 0/3 V pulse and 500 MHz bandwidth

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Figure 3. Pin Configuration (Top View)

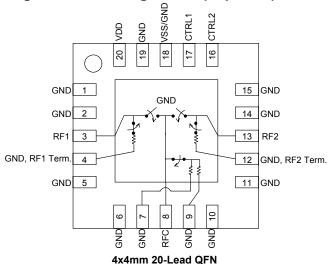


Table 2. Pin Descriptions

No.	Name	Description	
1	GND	RF Ground	
2	GND	RF Ground	
3 <sup>1</sup>	RF1	RF I/O	
4	GND	RF Ground	
5	GND	RF Ground	
6	GND	RF Ground	
7	GND	RF Ground	
8 <sup>1</sup>	RFC	RF Common	
9	GND	RF Ground	
10	GND	RF Ground	
11	GND	RF Ground	
12	GND	RF Ground	
13¹	RF2	RF I/O	
14	GND	RF Ground	
15	GND	RF Ground	
16 <sup>2</sup>	CTRL2	Control 2	
17 <sup>2</sup>	CTRL1	Control 1	
18³	VSS / GND	Negative Supply Option	
19	GND	Digital Ground	
20	VDD	Supply	
Pad	GND	RF Ground Pad	

Notes: 1. RF pins 3, 8, and 13 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

- 2. Pins 16 and 17 are the CMOS controls that set the four operating states.
- 3. Connect pin 18 to GND to enable the negative voltage generator. Connect pin 18 to Vss (-3 V) to bypass and disable internal -3 V supply generator. See paragraph "Switching Frequency."

**Table 3. Absolute Maximum Ratings** 

Symbol	Parameter/Condition	Min	Max	Units
$V_{DD}$	Power supply voltage	-0.3	4.0	V
Vı	Voltage on any DC input	-0.3	$V_{DD} + 0.3$	٧
$P_{RF}$	RF power on RFC, RF1, RF2 On Port/ Terminated Port		33/24	dBm
T <sub>ST</sub>	Storage temperature	-65	+150	°C
$T_OP$	Operating temperature	-40	+85	°C
V <sub>ESD</sub>	ESD voltage (Human Body Model)	1000		٧

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. Operating Ranges @ 25 °C

Parameter	Min	Тур	Max	Unit
V <sub>DD</sub> Power Supply	2.7	3.0	3.3	V
$I_{DD}$ Power Supply Current $(V_{DD} = 3V, V_{CNTL} = 3V)$		8	20	μΑ
Control Voltage High	0.70 V <sub>DD</sub>			V
Control Voltage Low	0		0.30 V <sub>DD</sub>	V

## Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

## **Electrostatic Discharge (ESD) Precautions**

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESDsensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

## **Switching Frequency**

The PE4257 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 18=GND). The rate at which the PE4257 can be switched is only limited to the switching time if an external -3 V supply is provided at (pin18=V<sub>SS</sub>).

Table 5. Truth Table

CTRL1	CTRL2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A <sup>1</sup>	N/A <sup>1</sup>

Notes: 1. The operation of the PE4257 is not supported or

characterized in the C1=V<sub>DD</sub> and C2=V<sub>DD</sub> state.



# Typical Performance Data @ 25°C (Unless Otherwise Noted) (50-ohm impedance)

Figure 4. Insertion Loss - Input - Output

-0.5 RFC>RF1 RFC>RF2

-1.5 -2 0 500 1000 1500 2000 2500 3000 Frequency (MHz)

Figure 5. RF1 to RF2 Isolation

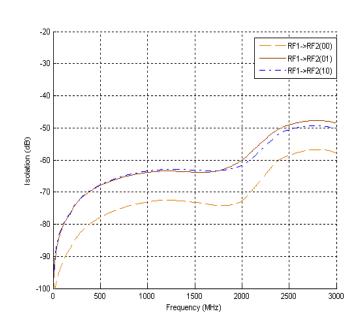


Figure 6. Isolation - RFC to RF1/RF2

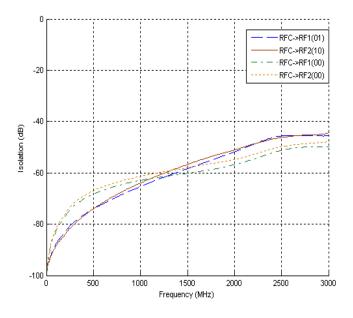
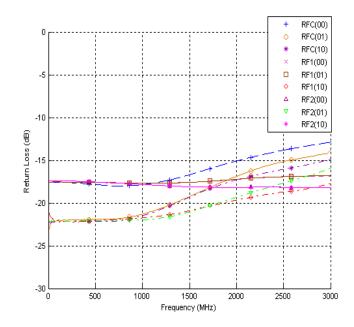


Figure 7. Return Loss





## **Evaluation Kit**

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4257 SPDT switch. The RF common port is connected through a 50  $\Omega$  transmission line to J2. Port 1 and Port 2 are connected through 50  $\Omega$  transmission lines to J1 and J3. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer FR4 material with a total thickness of 0.031". The transmission lines were designed using a coplanar waveguide with ground plane (28 mil core, 47.6 mil width, 30mil gap).

Note the number of vias surrounding the device in the layout shown in Figure 8. These vias are critical for obtaining the specified isolation performance for the device shown in this datasheet.

J6 provides a means for controlling DC and digital inputs to the device. The provided jumpers short the package pin to ground for logic low. When the jumper is removed, the pin is pulled up to VDD for logic high. When the jumper is in place, 3  $\mu A$  of current will flow through the 1  $M\Omega$  pull up resistor. This extra current should not be attributed to the requirements of the device.

## Figure 8. Evaluation Board Layouts

Peregrine Specification 101/0151

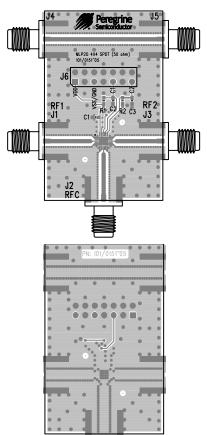
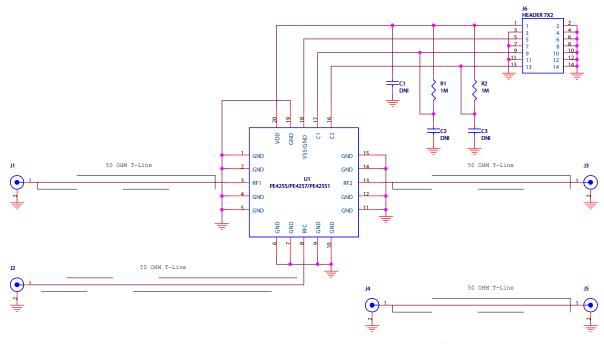


Figure 9. Evaluation Board Schematic

Peregrine Specification 102/0198



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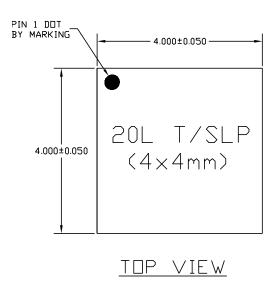
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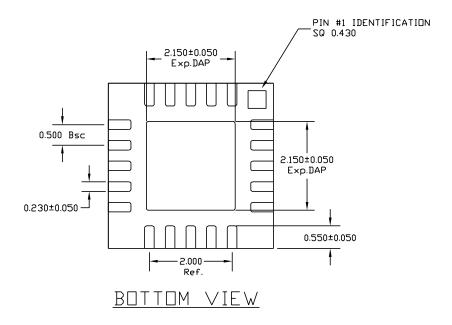
UltraCMOS™ RFIC Solutions



## Figure 10. Package Drawing

20-Lead 4x4 QFN





## NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE DUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
_	MAX.	0.800	0.900
ΙΑ	N□M.	0.750	0.850
	MIN.	0.700	0.800

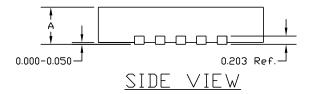
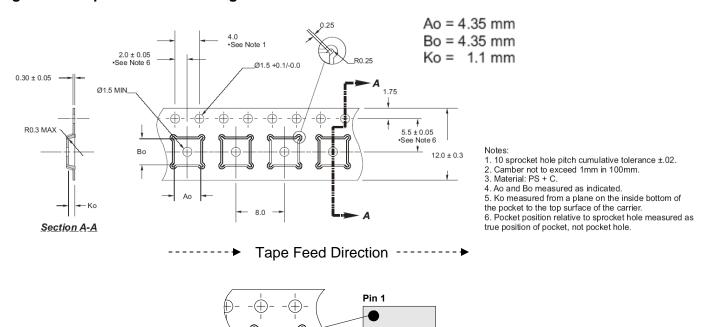




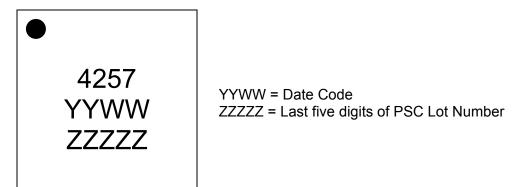
Figure 11. Tape and Reel Drawing



Top of **Device** 

**Device Orientation in Tape** 

Figure 12. Marking Specifications



**Table 6. Ordering Information** 

Order Code	Part Marking	Description	Package	Shipping Method
4257-00	PE4257-EK	PE4257-20QFN 4x4mm-EK	Evaluation Kit	1 / Box
4257-51	4257	PE4257G-20QFN 4x4mm-75A	Green 20-lead 4x4mm QFN	75 units / cut tape from reel
4257-52	4257	PE4257G-20QFN 4x4mm-3000C	Green 20-lead 4x4mm QFN	3000 units / T&R



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