3A/40V/150kHz Buck Converter with CC mode

General Description

The VP2140 is an efficiency and low-cost buck converter with integrated low $R_{DS(ON)}$ high-side 100mΩ MOSFET switch. It is capable of delivering 3A continuous output current with programmable current limit over a wide range of supplying voltage from 8V to 40V. With a simple voltage divider, the output voltage is easily adjustable from 1.22V to 24V.

Other features such as 150kHz PWM frequency, output over-voltage protection, total fault-free protection and low 35μA shutdown current/ 1.2mA quiescent current make VP2140 ideally to be used in application like automotive equipments and networking devices.

The VP2140 is available in popular SO-8P green package with exposed pad.

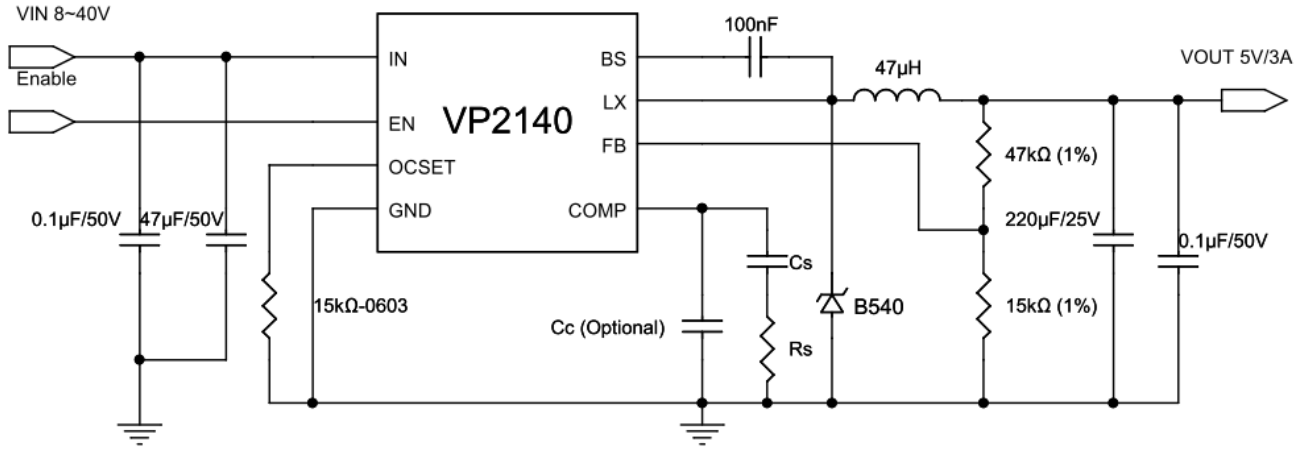
Features

- 8V to 40V Input Voltage Range
- Adjustable Output from 1.22V to 24V
- Continuous 3A Output Current
- Integrated 100mΩ MOSFET Switch
- 1.22V Voltage Reference with ±2% Accuracy
- Low 35μA Shutdown Current
- Fixed 1.2x Output Over Voltage Protection
- Fixed 150kHz Switching Frequency
- Programmable CV/CC mode
- Rapid Response Current Mode Operation
- Over Voltage and Current Limit
- Over Temperature Protection
- RoHS 2.0 compliant SO-8P Green Package with Exposed Pad

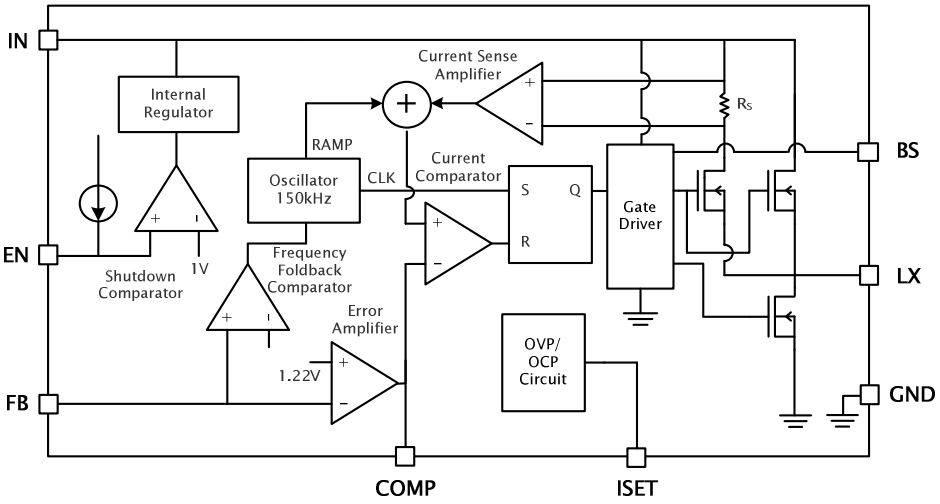
Applications

- Car Charger
- Wireless Communication Device
- Networking Device
- LCD Monitor/ LCD TV

Typical Application

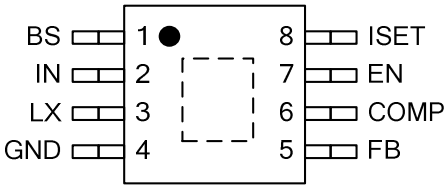


Functional Block Diagram



Pin Assignments And Descriptions

SO-8P
Top View



Pin No.	Pin	I/O/P	Function Description
1	BS	-	High-side MOSFET switch gate drive boost input. Connect at least 100nF capacitor from LX to BS to control the High-Side switch. Place the capacitor close to this pin.
2	IN	P	Power Input. Drive IN with an 8V to 40V power source to activate the converter.
3	LX	O	Switch Output. LX is the switching node that generate PWM waveforms to the output.
4	GND	P	Power ground.
5	FB	I	Feedback Input. FB pin monitors the voltage offset from output to regulate output voltage. Use a voltage divider feedback from the output to drive FB pin.
6	COMP	-	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop.
7	EN	I	Chip Enable. Pull EN high to enable the regulator, pull it low to turn it off. Pull up with a 100kΩ resistor to start it up automatically.
8	ISET	-	Current Limit Setting. Connect a resistor from ISET to GND to set the peak switching current. Leave it floating for internal current limit.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{IN}	Supply voltage range	-0.3 to 42	V
V_{LX}	Switch voltage range	-1 to V_{IN}+1	V
V_{BS}	High-side MOSFET switch gate drive voltage range	V_{LX}-0.3 to V_{LX}+6	V
V_{IN}(COMP, EN, FB, SS)	Low voltage input range	-0.3 to 6	V
T_J	Operating junction temperature range	-40 to +160	°C
T_{STG}	Storage temperature range	-65 to 150	°C
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V
θ_{JC}	Thermal Resistance (Junction to Case)	10	°C/W
θ_{JA}	Thermal Resistance (Junction to Air)	50	°C/W

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Symbol	Parameter	Specification		Unit
		Min	Max	
V_{IN}	Supply voltage	8	40	V
V_{OUT}	Output voltage	1.22	24	V
T_A	Operating free-air temperature range	-40	85	°C

Electrical Characteristics

T_A = 25℃, V_{IN} = 24V, unless otherwise noted

Symbol	Parameter	Test Condition	Specification			Unit
			Min	Typ	Max	
I_{SD}	Shutdown supply current	V_{EN}=0V		35	60	μA
I_Q	Supply current	V_{EN}=2.0V, Non-Switching		1.2	1.4	mA
V_{REF}	Reference voltage	8V≤V_{IN}≤40V	1.2	1.22	1.24	V
$R_{DS(ON)H}$	High-Side switch $R_{DS(ON)}$			100		mΩ
$R_{DS(ON)L}$	Low-Side switch $R_{DS(ON)}$			10		Ω
	Internal current Limit			4.3		A
A_{EA}	Error amplifier voltage gain			400		V/V
G_{EA}	Error amplifier transconductance			500		μ℧
G_{CS}	COMP to current sense transcondutance			3.3		℧
f_{OSC}	Oscillation frequency			150		kHz
	Short circuit oscillation frequency	V_{FB}=0V		80		kHz
D_{MAX}	Maximum duty cycle	V_{FB}=1.0V		85		%
$t_{ON(MIN)}$	Minimum ON time				120	ns
	EN shutdown threshold voltage	V_{EN} rising	0.8	1	1.2	V
	EN pin leakage current	V_{EN} =0V		6		μA
	Soft-start bias current			4		μA
	Over temperature shutdown			150		℃
	Over temperature shutdown hystersis			20		℃

Functional Descriptions

The VP2140 is a fixed frequency, current mode asynchronous buck converter. During normal operation, the internal MOSFET switch is controlled by the gate driver and dominates the duty cycle of the PWM waveform. While the switch is turned off, the inductor current flows through the external diode.

PWM Oscillation

The frequency of the internal oscillator is fixed at 150kHz. In case of short circuit (output/feedback voltage is zero), the frequency will be down to 85kHz to reduce the heat and minimize the power consumption.

Error Amplifier

The error amplifier compares the voltage of FB pin with the internal voltage reference V_{REF}. When the output current increases, the voltage of FB pin decreases and the error amplifier output will start to increase. This will force the gate driver to increase the duty cycle of the PWM waveform and raise the inductor current to compensate the output voltage drop.

Adjusting Peak Switching Current

To adjust the peak switching current is easy by connecting a resistor R_{ISET} from ISET pin to GND.

Chip Enable

The VP2140 has an EN pin to perform chip enable control. The regulator can be enabled and disabled by simply applying state logic values on EN pin. The precision values of the rising threshold is 1V and the falling threshold is 0.8V. Never leave the EN pin floating and make sure the value of the logic away from the voltage region of rising threshold and falling threshold.

Under-voltage Lockout

Under-voltage lockout (UVLO) is implemented to protect the internal gate driver away from uncertain state and lose the control of the MOSFET switch. UVLO threshold voltage is 6.5V typically.

Thermal Protection

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, it forces the whole chip entering shutdown state. When the temperature is lower than its lower threshold, it resumes the normal operation.

Output Voltage

In Figure 1, the output voltage can be set by the resistor network connected to the output voltage terminal and FB pin. The resistor network divides the output voltage down to the feedback voltage by the follow ratio:

$$V_{FB} = V_{OUT} \frac{R_2}{R_1 + R_2}$$

where V_{FB} is the feedback voltage, V_{OUT} is the output voltage.

Thus the output voltage can be obtained by the following equation:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$$

Functional Descriptions (cont.)

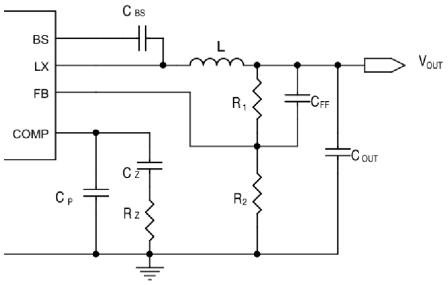


Figure 1. Output network of VP2140

Application Information

The VP2140 is an asynchronous high voltage buck converter that can support the input voltage range from 7V to 40V and the output current can be up to 3A.

Inductor Selection

The value of the inductor affects the ripples of output voltage and must be carefully selected. In the same working condition, larger inductance value results in lower output ripple voltage but such inductor will be oversized, higher series resistance and lower saturation current.

In most cases, it would be a good rule to keep peak-to-peak switching current ΔI_L to be approximate 30% of the maximum switching current. And it is necessary to assure the peak inductor current is under maximum switch current limit. Thus, the inductance can be calculated by the following equation:

$$L = \frac{V_{OUT}}{f \times \Delta I_L}(1 - \frac{V_{OUT}}{V_{IN}})$$

where f is the switch frequency, L is the inductance.

Hence the maximum peak current limit of the inductor $I_{L(PEAK)}$ can be obtained by:

$$I_{L(PEAK)} = I_{LOAD} + \Delta I_L = \frac{V_{OUT}}{2f \times L}(1 - \frac{V_{OUT}}{V_{IN}})$$

where I_{LOAD} is the maximum load current.

With the equations listed above, the inductance of inductor can be calculated easily. Actually, the selection of the inductor is the compromise of the cost, size, electrical specification and desired electro-magnetic compatibility.

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, it is recommended to use a Schottky diode. Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Input Capacitor Selection

The VP2140 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. The use of low ESR capacitors can give the benefits of better performance and less ripple voltage.

The input capacitor should be considered with the RMS current rating. The following equation shows how t could be estimated:

$$I_{RMS(CIN)} = I_{LOAD(MAX)} \times \sqrt{Duty \times (1 - Duty)}$$

where Duty is the PWM duty cycle, $I_{LOAD(MAX)}$ is the maximum load current.

Therefore, select input capacitor with ripple current rating larger than half of the maximum load current.

The input ripple voltage ΔVIN depends on the ESR and capacitance of input capacitor. The value of the input capacitor can be determined as the followings:

$$C_{IN} = \frac{I_{LOAD(MAX)} \times Duty \times (1 - Duty)}{f \times (\Delta V_{IN} - I_{LOAD(MAX)} \times ESR)}$$

Input capacitor could cause significant conduction loss if the input current is large enough. Its power dissipation is listed below:

Application Information (cont.)

$$P_{D(CIN)} = I_{RMS(CIN)}^{2} \times ESR$$

When selecting input capacitor, make sure the capacitance is enough to prevent the excessive input ripple current. If using aluminum electrolytic input capacitors, parallel connecting 0.1μF speed-up capacitor as close to the regulator as possible.

Output Capacitor Selection

The output capacitor is to maintain output voltage and reduce output ripple voltage ΔV_{OUT} and the low ESR capacitor is preferred. The output ripple voltage can be obtained by the following equation:

$$\Delta V_{OUT} = \Delta I_L \times (ESR + \frac{1}{8 \times f \times C_{OUT}})$$

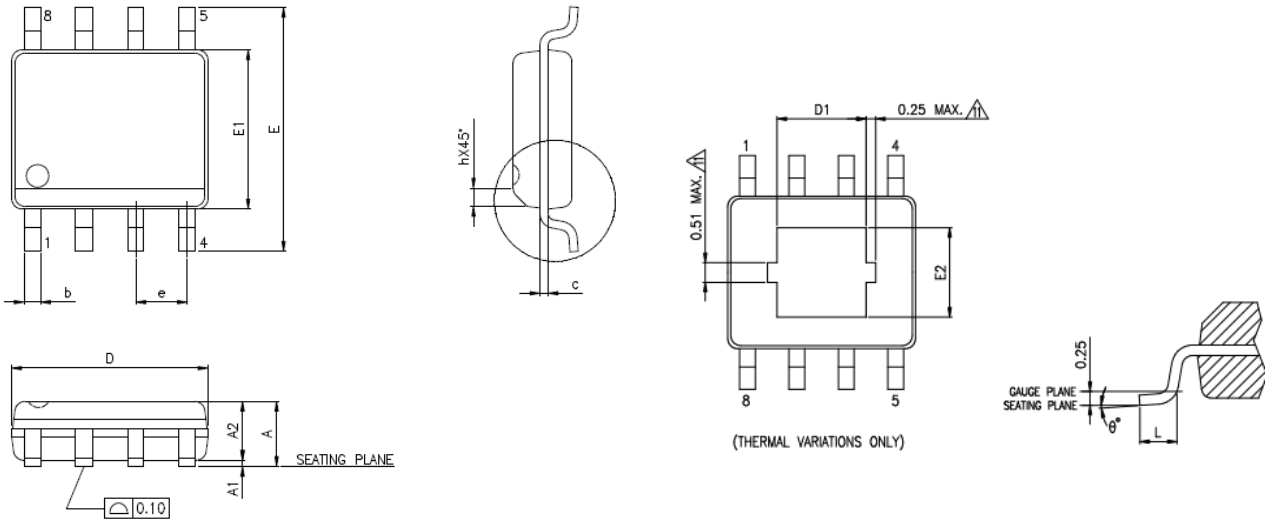
Boot-Strap Capacitor Selection

A 100nF ceramic capacitor must be connected between the BS pin to LX pin for proper operation. It is recommended to use a ceramic capacitor.

Application Information (cont.)

Package Information

SO-8P



Sym-bols	Standard		Thermal	
	Min.	Max.	Min.	Max.
A	-	1.75	-	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	-	1.25	-
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	4.90 BSC		4.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

Thermal Enhanced Dimensions

Pad Size	E2		D1	
	Min.	Max.	Min.	Max.
90x90E	1.94	2.29	1.94	2.29
95x13E	2.05	2.41	2.81	3.30

Notes:
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP: Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. JEDEC Outline : MS-012 AA Rev. F (Standard), MS-012 BA Rev. F (Thermal)
4. Dimensions “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.51mm per side.
5. Dimensions “E1” does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm per side.

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