

8-Bit CMOS Microcontrollers with A/D Converter

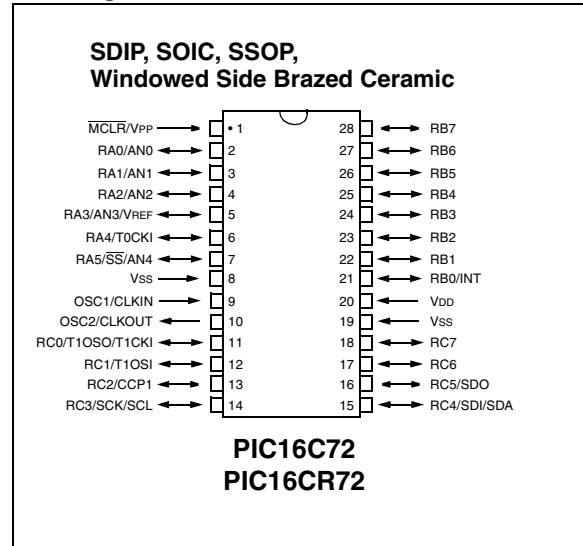
Devices included:

- PIC16C72
- PIC16CR72

Microcontroller Core Features:

- High-performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
- 2K x 14 words of Program Memory,
128 x 8 bytes of Data Memory (RAM)
- Interrupt capability
- Eight level deep hardware stack
- Direct, indirect, and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and
Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC
oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low-power, high-speed CMOS technology
- Fully static design
- Wide operating voltage range:
 - 2.5V to 6.0V (PIC16C72)
 - 2.5V to 5.5V (PIC16CR72)
- High Sink/Source Current 25/25 mA
- Commercial, Industrial and Extended temperature
ranges
- Low-power consumption:
 - < 2 mA @ 5V, 4 MHz
 - 15 μ A typical @ 3V, 32 kHz
 - < 1 μ A typical standby current

Pin Diagrams



Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler,
can be incremented during sleep via external
crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period
register, prescaler and postscaler
- Capture, Compare, PWM (CCP) module
 - Capture is 16-bit, max. resolution is 12.5 ns
 - Compare is 16-bit, max. resolution is 200 ns
 - PWM max. resolution is 10-bit
- 8-bit 5-channel analog-to-digital converter
- Synchronous Serial Port (SSP) with
SPI and I²C™
- Brown-out detection circuitry for
Brown-out Reset (BOR)

PIC16C72 Series

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| Key Reference Manual Features | PIC16C72 | PIC16CR72 |
|---------------------------------------|------------------------|------------------------|
| Operating Frequency | DC - 20MHz | DC - 20MHz |
| Resets | POR, PWRT, OST, BOR | POR, PWRT, OST, BOR |
| Program Memory - (14-bit words) | 2K (EPROM) | 2K (ROM) |
| Data Memory - RAM (8-bit bytes) | 128 | 128 |
| Interrupts | 8 | 8 |
| I/O Ports | PortA, PortB, PortC | PortA, PortB, PortC |
| Timers | Timer0, Timer1, Timer2 | Timer0, Timer1, Timer2 |
| Capture/Compare/PWM Modules | 1 | 1 |
| Serial Communications | Basic SSP | SSP |
| 8-Bit A/D Converter | 5 channels | 5 channels |
| Instruction Set (No. of Instructions) | 35 | 35 |

1.0 DEVICE OVERVIEW

This document contains device-specific information for the operation of the PIC16C72 device. Additional information may be found in the PIC® Mid-Range MCU Reference Manual (DS33023) which may be downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16C72 belongs to the Mid-Range family of the PIC devices. A block diagram of the device is shown in Figure 1-1.

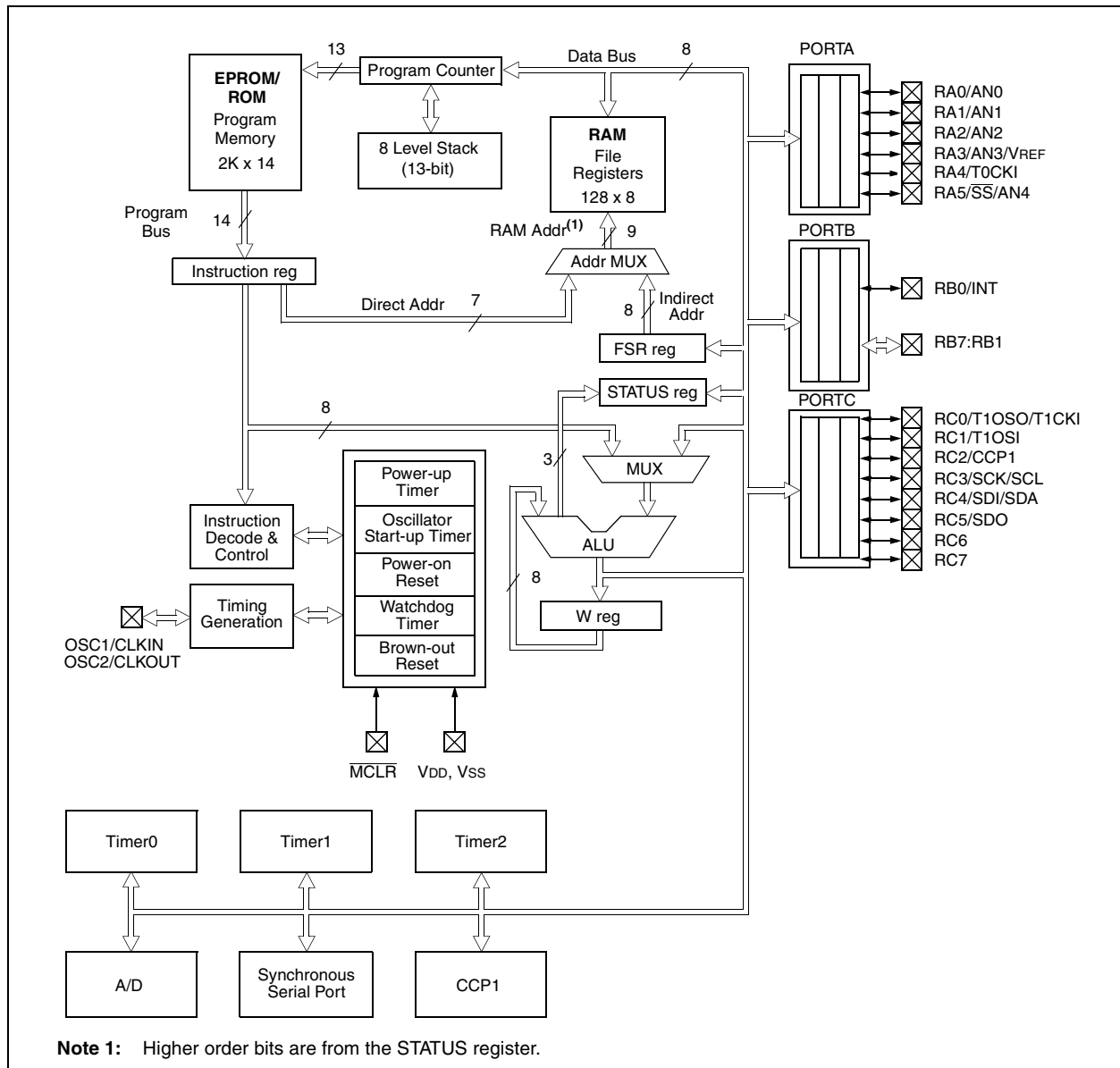
The program memory contains 2K words which translate to 2048 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 128 bytes.

There are also 22 I/O pins that are user-configurable on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External interrupt
- Change on PORTB interrupt
- Timer0 clock input
- Timer1 clock/oscillator
- Capture/Compare/PWM
- A/D converter
- SPI/I²C

Table 1-1 details the pinout of the device with descriptions and details for each pin.

FIGURE 1-1: PIC16C72/CR72 BLOCK DIAGRAM



PIC16C72 Series

TABLE 1-1 PIC16C72/CR72 PINOUT DESCRIPTION

| Pin Name | Pin# | I/O/P Type | Buffer Type | Description |
|-----------------|-------|------------|------------------------|---|
| OSC1/CLKIN | 9 | I | ST/CMOS ⁽³⁾ | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 10 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| MCLR/VPP | 1 | I/P | ST | Master clear (reset) input or programming voltage input. This pin is an active low reset to the device. |
| RA0/AN0 | 2 | I/O | TTL | <p>PORTA is a bi-directional I/O port.</p> <p>RA0 can also be analog input0.</p> <p>RA1 can also be analog input1.</p> <p>RA2 can also be analog input2.</p> <p>RA3 can also be analog input3 or analog reference voltage</p> <p>RA4 can also be the clock input to the Timer0 module. Output is open drain type.</p> <p>RA5 can also be analog input4 or the slave select for the synchronous serial port.</p> |
| RA1/AN1 | 3 | I/O | TTL | |
| RA2/AN2 | 4 | I/O | TTL | |
| RA3/AN3/VREF | 5 | I/O | TTL | |
| RA4/T0CKI | 6 | I/O | ST | |
| RA5/SS/AN4 | 7 | I/O | TTL | |
| RB0/INT | 21 | I/O | TTL/ST ⁽¹⁾ | <p>PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.</p> <p>RB0 can also be the external interrupt pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin. Serial programming clock.</p> <p>Interrupt on change pin. Serial programming data.</p> |
| RB1 | 22 | I/O | TTL | |
| RB2 | 23 | I/O | TTL | |
| RB3 | 24 | I/O | TTL | |
| RB4 | 25 | I/O | TTL | |
| RB5 | 26 | I/O | TTL | |
| RB6 | 27 | I/O | TTL/ST ⁽²⁾ | |
| RB7 | 28 | I/O | TTL/ST ⁽²⁾ | |
| RC0/T1OSO/T1CKI | 11 | I/O | ST | <p>PORTC is a bi-directional I/O port.</p> <p>RC0 can also be the Timer1 oscillator output or Timer1 clock input.</p> <p>RC1 can also be the Timer1 oscillator input.</p> <p>RC2 can also be the Capture1 input/Compare1 output/PWM1 output.</p> <p>RC3 can also be the synchronous serial clock input/output for both SPI and I²C modes.</p> <p>RC4 can also be the SPI Data In (SPI mode) or data I/O (I²C mode).</p> <p>RC5 can also be the SPI Data Out (SPI mode).</p> |
| RC1/T1OSI | 12 | I/O | ST | |
| RC2/CCP1 | 13 | I/O | ST | |
| RC3/SCK/SCL | 14 | I/O | ST | |
| RC4/SDI/SDA | 15 | I/O | ST | |
| RC5/SDO | 16 | I/O | ST | |
| RC6 | 17 | I/O | ST | |
| RC7 | 18 | I/O | ST | |
| Vss | 8, 19 | P | — | Ground reference for logic and I/O pins. |
| VDD | 20 | P | — | Positive supply for logic and I/O pins. |

Legend: I = input O = output I/O = input/output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

- Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in serial programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

2.0 MEMORY ORGANIZATION

There are two memory blocks in PIC16C72 Series devices. These are the program memory and the data memory. Each block has its own bus, so that access to both blocks can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

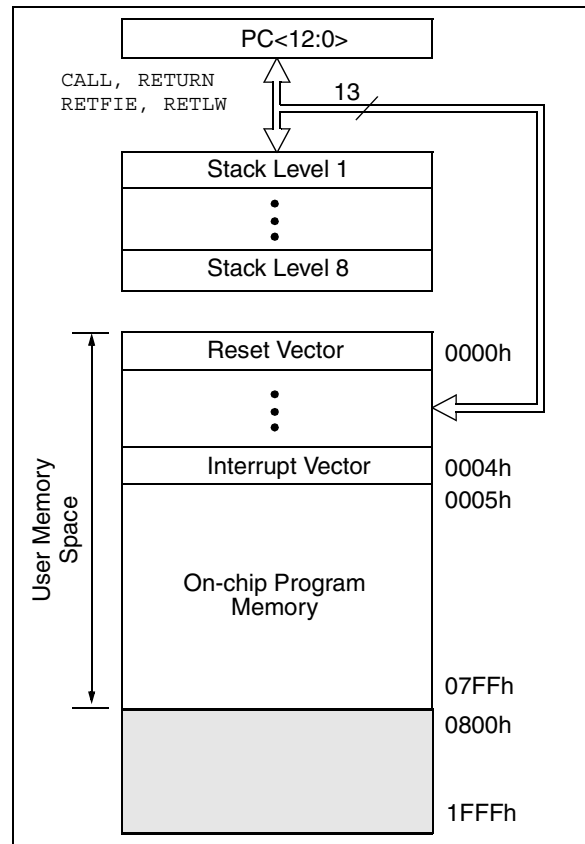
Additional information on device memory may be found in the PIC® Mid-Range Reference Manual, DS33023.

2.1 Program Memory Organization

PIC16C72 Series devices have a 13-bit program counter capable of addressing a 2K x 14 program memory space. The address range for this program memory is 0000h - 07FFh. Accessing a location above the physically implemented address will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK



PIC16C72 Series

2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

RP1* RP0 (STATUS<6:5>)

- = 00 → Bank0
- = 01 → Bank1
- = 10 → Bank2 (not implemented)
- = 11 → Bank3 (not implemented)

* Maintain this bit clear to ensure upward compatibility with future products.

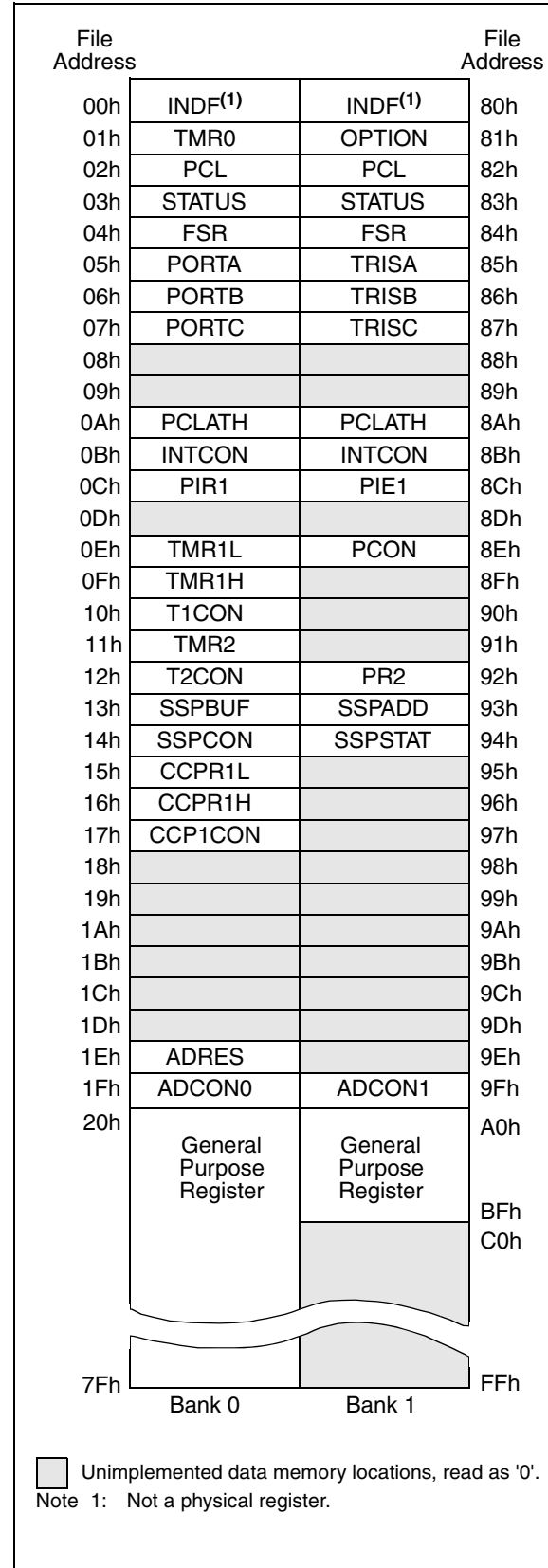
Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM.

All implemented banks contain special function registers. Some “high use” special function registers from one bank may be mirrored in another bank for code reduction and quicker access (ex; the STATUS register is in Bank 0 and Bank 1).

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly or indirectly through the File Select Register FSR (Section 2.5).

FIGURE 2-2: REGISTER FILE MAP



2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

sets (core and peripheral). Those registers associated with the “core” functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

The special function registers can be classified into two

TABLE 2-1 SPECIAL FUNCTION REGISTER SUMMARY

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets (3) |
|----------------------|---------|--|--------------------|---|--|-----------------|---------------------|---------|---------|--------------------|-------------------------------|
| Bank 0 | | | | | | | | | | | |
| 00h ⁽¹⁾ | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 01h | TMR0 | Timer0 module's register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 02h ⁽¹⁾ | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 03h ⁽¹⁾ | STATUS | IRP ⁽⁴⁾ | RP1 ⁽⁴⁾ | RP0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx | 000q quuu |
| 04h ⁽¹⁾ | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 05h | PORTA | — | — | PORTA Data Latch when written: PORTA pins when read | | | | | | --0x 0000 | --0u 0000 |
| 06h | PORTB | PORTB Data Latch when written: PORTB pins when read | | | | | | | | xxxx xxxx | uuuu uuuu |
| 07h | PORTC | PORTC Data Latch when written: PORTC pins when read | | | | | | | | xxxx xxxx | uuuu uuuu |
| 08h | — | Unimplemented | | | | | | | | — | — |
| 09h | — | Unimplemented | | | | | | | | — | — |
| 0Ah ^(1,2) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the Program Counter | | | | | ---0 0000 | ---0 0000 |
| 0Bh ⁽¹⁾ | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | — | ADIF | — | — | SSPIF | CCP1IF | TMR2IF | TMR1IF | -0-- 0000 | -0-- 0000 |
| 0Dh | — | Unimplemented | | | | | | | | — | — |
| 0Eh | TMR1L | Holding register for the Least Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Fh | TMR1H | Holding register for the Most Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10h | T1CON | — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON | --00 0000 | --uu uuuu |
| 11h | TMR2 | Timer2 module's register | | | | | | | | 0000 0000 | 0000 0000 |
| 12h | T2CON | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| 13h | SSPBUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 14h | SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 0000 0000 |
| 15h | CCPR1L | Capture/Compare/PWM Register (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 16h | CCPR1H | Capture/Compare/PWM Register (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 17h | CCP1CON | — | — | CCP1X | CCP1Y | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | --00 0000 | --00 0000 |
| 18h-1Dh | — | Unimplemented | | | | | | | | — | — |
| 1Eh | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 1Fh | ADCON0 | ADCS1 | ADCS0 | CHS2 | CHS1 | CHS0 | GO/DONE | — | ADON | 0000 00-0 | 0000 00-0 |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.

Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through \overline{MCLR} and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C72/CR72. Always maintain these bits clear.

5: SSPSTAT<7:6> are not implemented on the PIC16C72, read as '0'.

PIC16C72 Series

TABLE 2-1 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets (3) |
|----------------------|------------|--|--------------------|-------------------------------|---|-----------------|--------|--------|--------|--------------------------|-------------------------------------|
| Bank 1 | | | | | | | | | | | |
| 80h ⁽¹⁾ | INDF | Addressing this location uses contents of FSR to address data memory (not a physical register) | | | | | | | | 0000 0000 | 0000 0000 |
| 81h | OPTION_REG | RBPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 82h ⁽¹⁾ | PCL | Program Counter's (PC) Least Significant Byte | | | | | | | | 0000 0000 | 0000 0000 |
| 83h ⁽¹⁾ | STATUS | IRP ⁽⁴⁾ | RP1 ⁽⁴⁾ | RP0 | \overline{TO} | \overline{PD} | Z | DC | C | 0001 1xxx | 000q quuu |
| 84h ⁽¹⁾ | FSR | Indirect data memory address pointer | | | | | | | | xxxx xxxx | uuuu uuuu |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |
| 86h | TRISB | PORTB Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 88h | — | Unimplemented | | | | | | | | — | — |
| 89h | — | Unimplemented | | | | | | | | — | — |
| 8Ah ^(1,2) | PCLATH | — | — | — | Write Buffer for the upper 5 bits of the PC | | | | | ---0 0000 | ---0 0000 |
| 8Bh ⁽¹⁾ | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 8Ch | PIE1 | — | ADIE | — | — | SSPIE | CCP1IE | TMR2IE | TMR1IE | -0-- 0000 | -0-- 0000 |
| 8Dh | — | Unimplemented | | | | | | | | — | — |
| 8Eh | PCON | — | — | — | — | — | — | POR | BOR | ---- --qq | ---- --uu |
| 8Fh | — | Unimplemented | | | | | | | | — | — |
| 90h | — | Unimplemented | | | | | | | | — | — |
| 91h | — | Unimplemented | | | | | | | | — | — |
| 92h | PR2 | Timer2 Period Register | | | | | | | | 1111 1111 | 1111 1111 |
| 93h | SSPADD | Synchronous Serial Port (I ² C mode) Address Register | | | | | | | | 0000 0000 | 0000 0000 |
| 94h | SSPSTAT | SMP ⁽⁵⁾ | CKE ⁽⁵⁾ | D/A | P | S | R/W | UA | BF | 0000 0000 | 0000 0000 |
| 95h | — | Unimplemented | | | | | | | | — | — |
| 96h | — | Unimplemented | | | | | | | | — | — |
| 97h | — | Unimplemented | | | | | | | | — | — |
| 98h | — | Unimplemented | | | | | | | | — | — |
| 99h | — | Unimplemented | | | | | | | | — | — |
| 9Ah | — | Unimplemented | | | | | | | | — | — |
| 9Bh | — | Unimplemented | | | | | | | | — | — |
| 9Ch | — | Unimplemented | | | | | | | | — | — |
| 9Dh | — | Unimplemented | | | | | | | | — | — |
| 9Eh | — | Unimplemented | | | | | | | | — | — |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | ---- -000 | ---- -000 |

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC16C72/CR72. Always maintain these bits clear.

5: SSPSTAT<7:6> are not implemented on the PIC16C72, read as '0'.

2.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 2-3, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

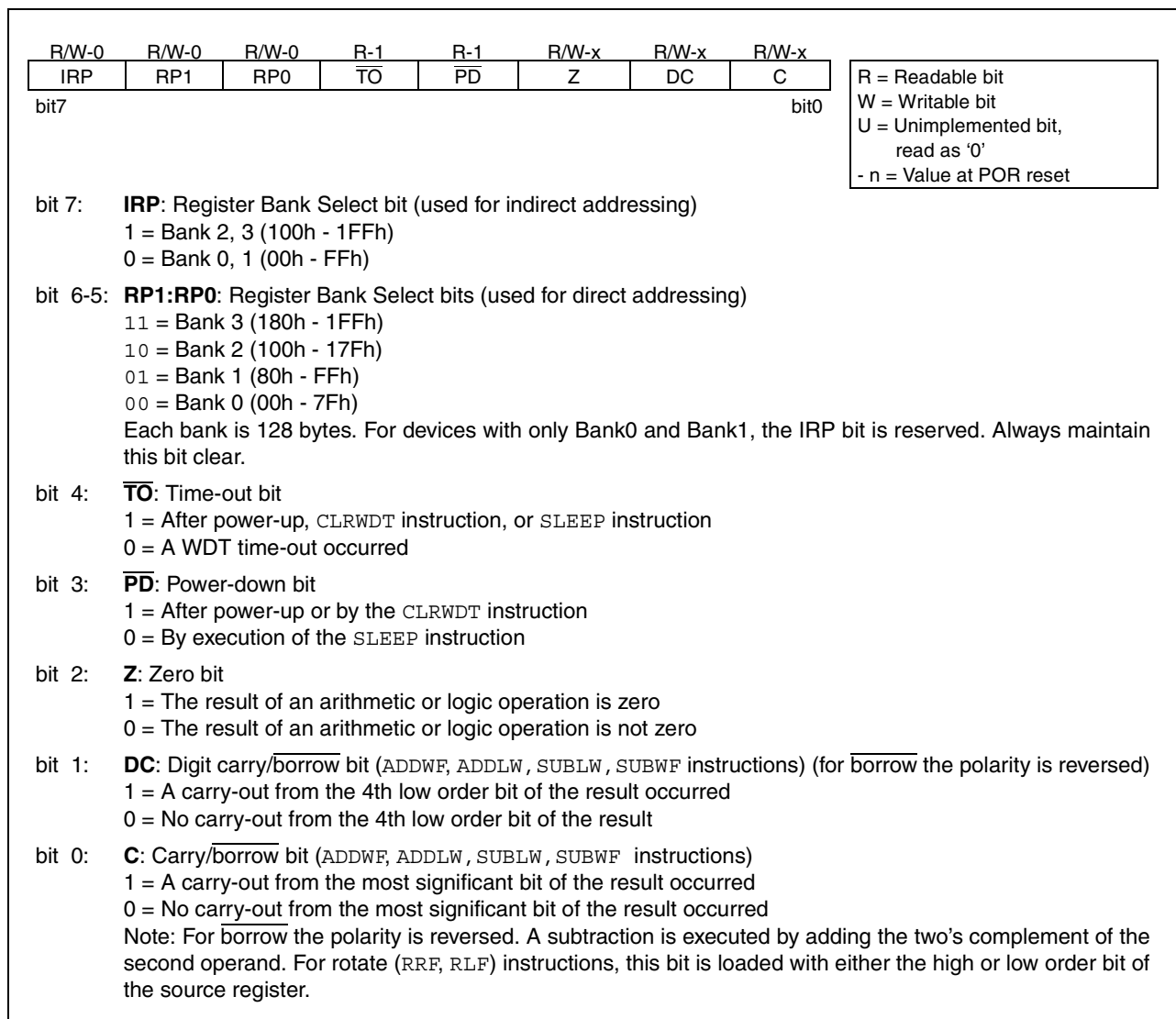
For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: These devices do not use bits IRP and RP1 (STATUS<7:6>). Maintain these bits clear to ensure upward compatibility with future products.

Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 2-3: STATUS REGISTER (ADDRESS 03h, 83h)



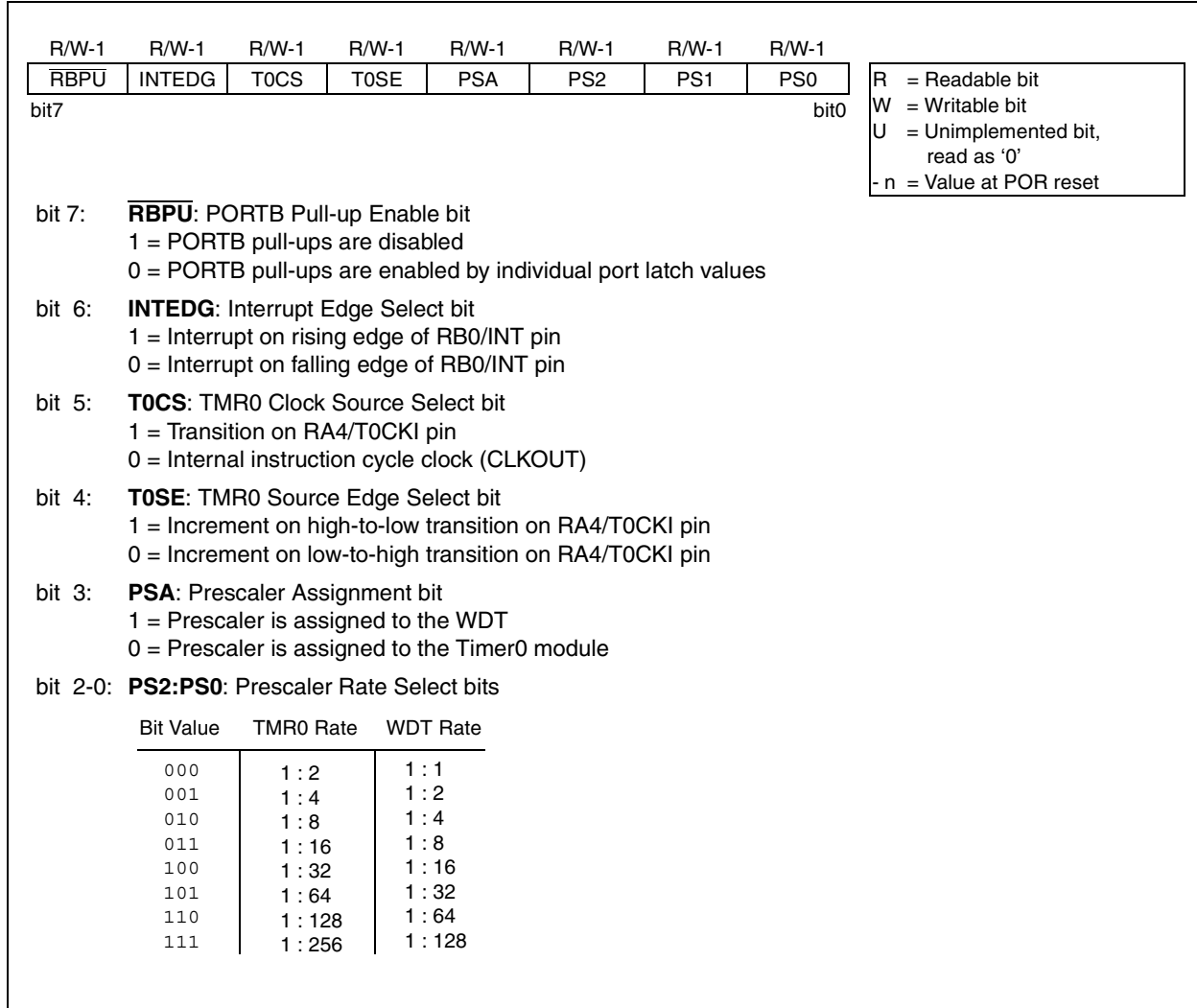
PIC16C72 Series

2.2.2.2 OPTION_REG REGISTER

The OPTION_REG register is a readable and writable register which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

FIGURE 2-4: OPTION_REG REGISTER (ADDRESS 81h)

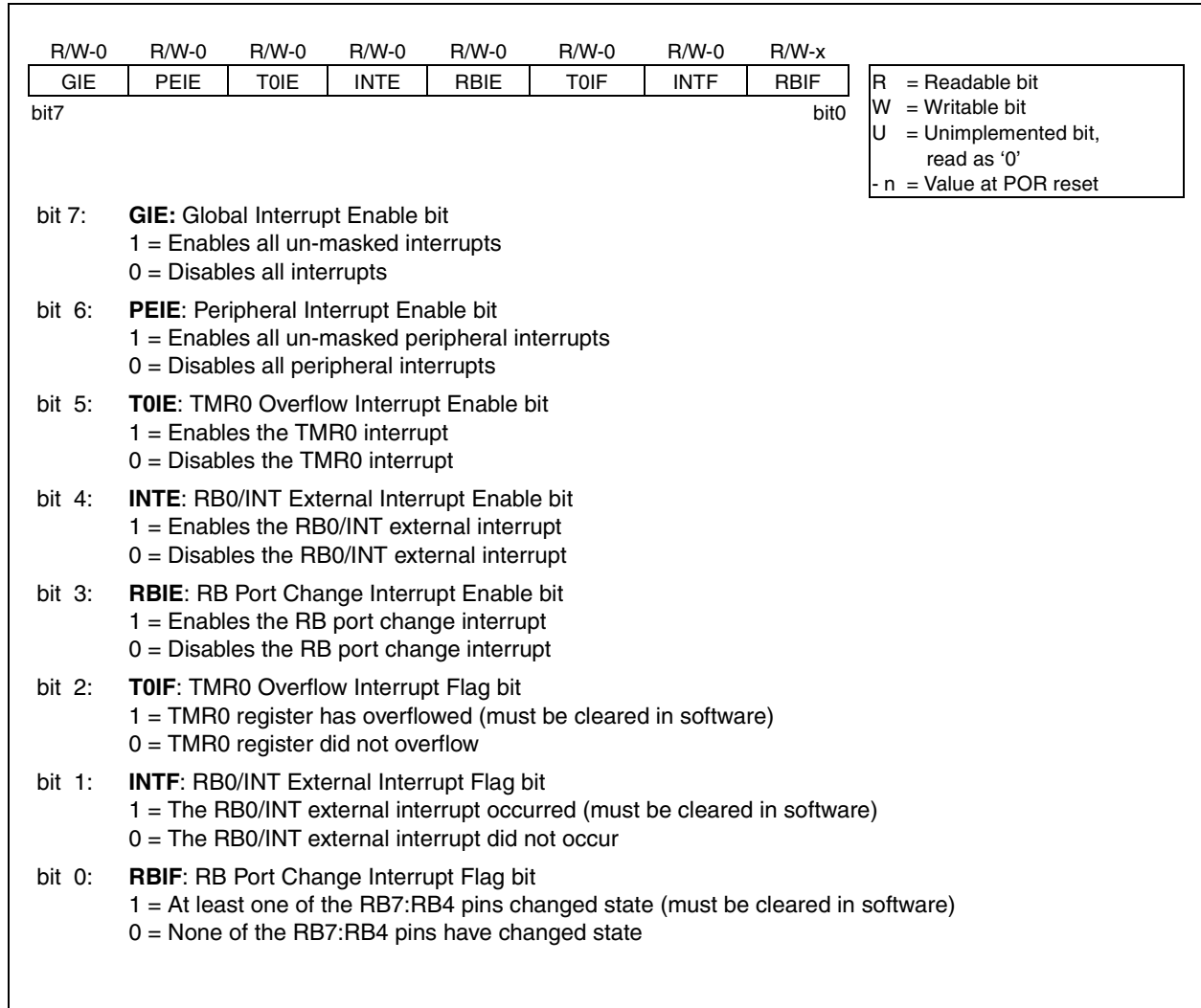


2.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 2-5: INTCON REGISTER (ADDRESS 0Bh, 8Bh)



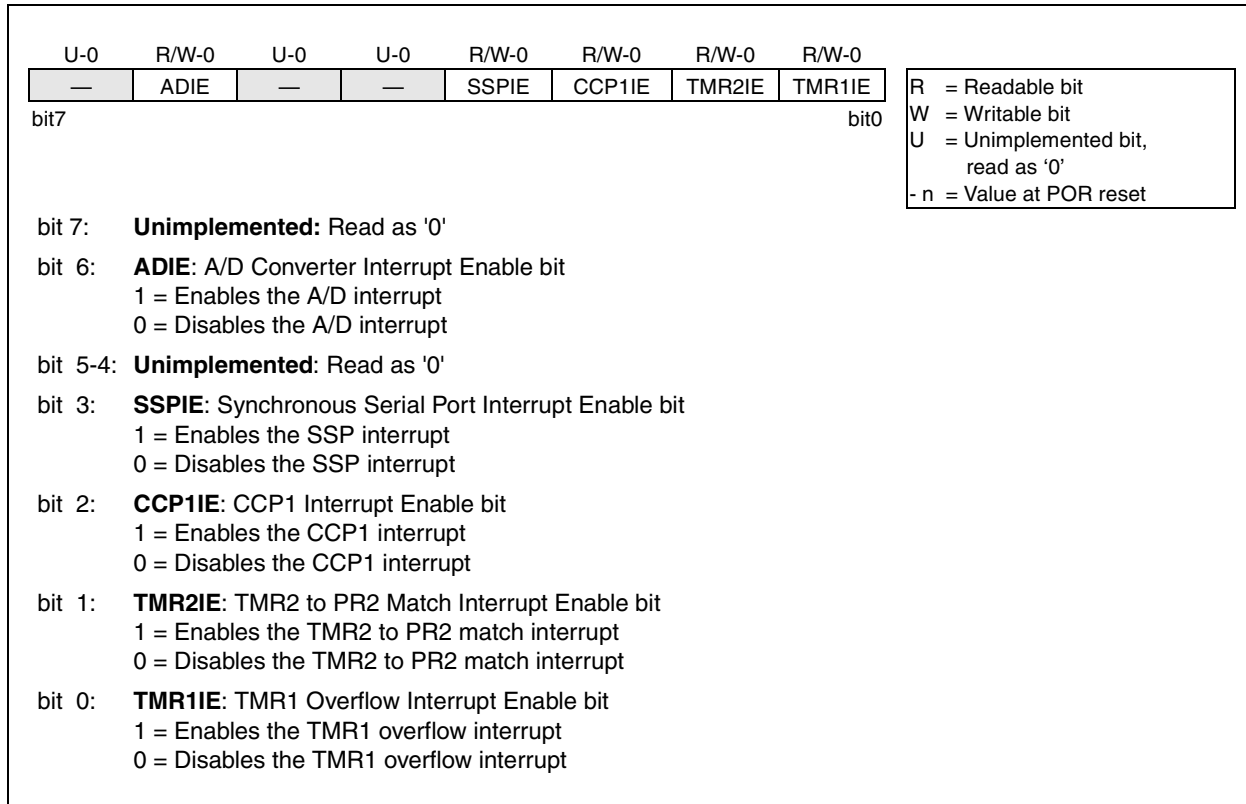
PIC16C72 Series

2.2.2.4 PIE1 REGISTER

This register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

FIGURE 2-6: PIE1 REGISTER (ADDRESS 8Ch)

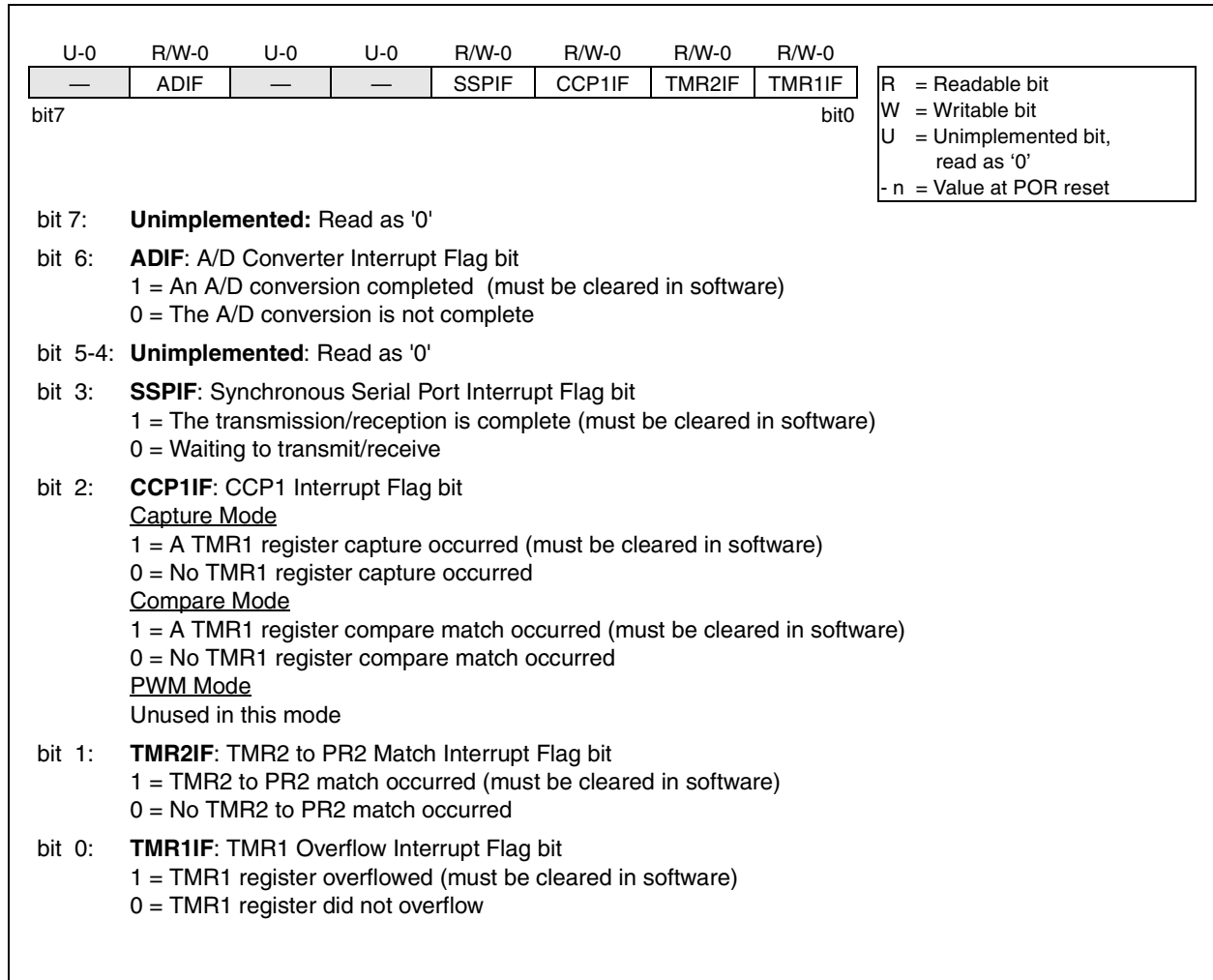


2.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the Peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 2-7: PIR1 REGISTER (ADDRESS 0Ch)



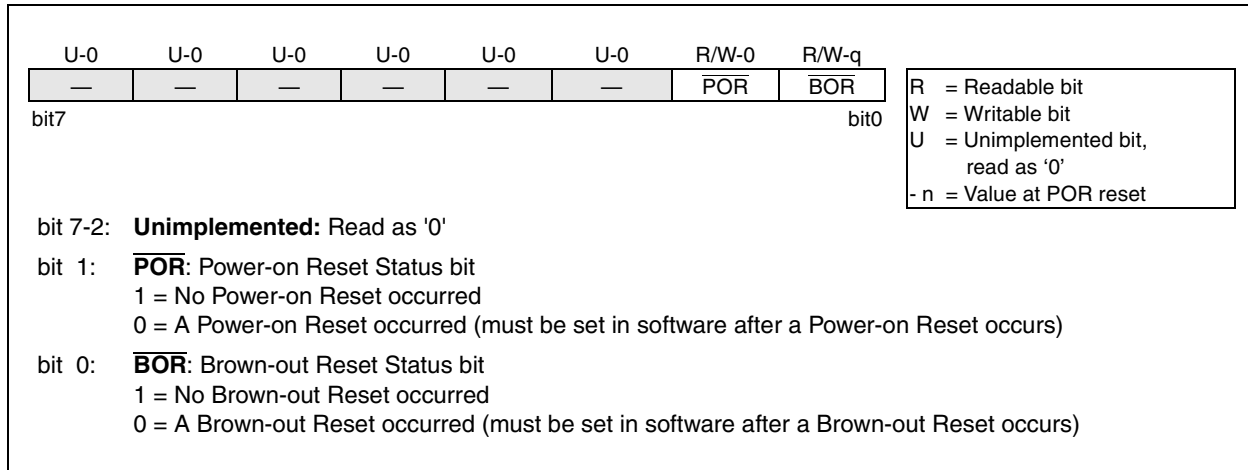
PIC16C72 Series

2.2.2.6 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR) to an external $\overline{\text{MCLR}}$ Reset or WDT Reset. Those devices with brown-out detection circuitry contain an additional bit to differentiate a Brown-out Reset condition from a Power-on Reset condition.

Note: $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent resets to see if $\overline{\text{BOR}}$ is clear, indicating a brown-out has occurred. The $\overline{\text{BOR}}$ status bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the Configuration word).

FIGURE 2-8: PCON REGISTER (ADDRESS 8Eh)

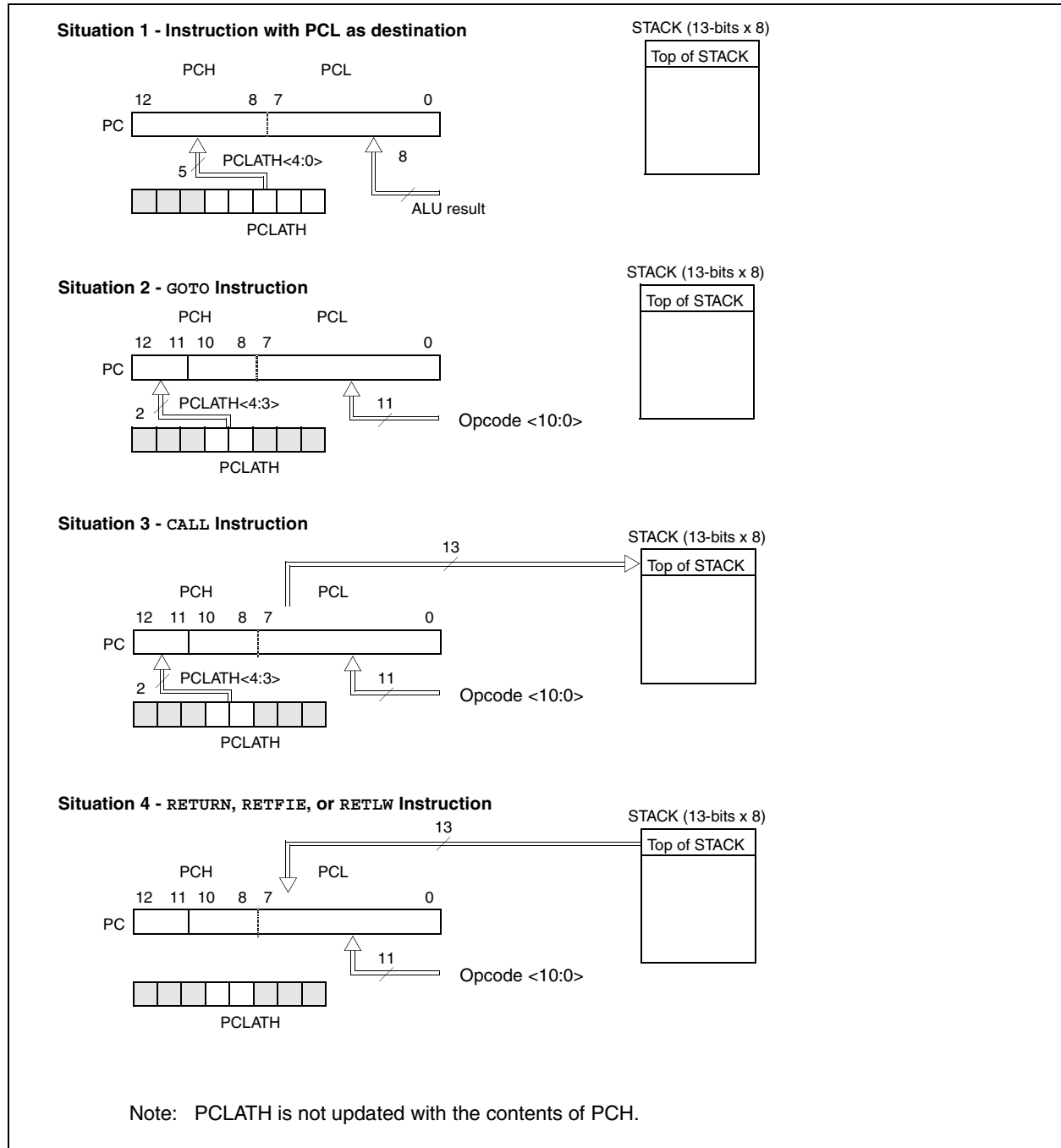


2.3 PCL and PCLATH

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 13 bits wide. The low byte is called the PCL register. This register is readable and writable. The high byte is called the PCH register. This register contains the PC<12:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCLATH register.

Figure 2-9 shows the four situations for the loading of the PC. Example 1 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). Example 2 shows how the PC is loaded during a GOTO instruction (PCLATH<4:3> → PCH). Example 3 shows how the PC is loaded during a CALL instruction (PCLATH<4:3> → PCH), with the PC loaded (PUSHed) onto the Top of Stack. Finally, example 4 shows how the PC is loaded during one of the return instructions where the PC is loaded (POPped) from the Top of Stack.

FIGURE 2-9: LOADING OF PC IN DIFFERENT SITUATIONS



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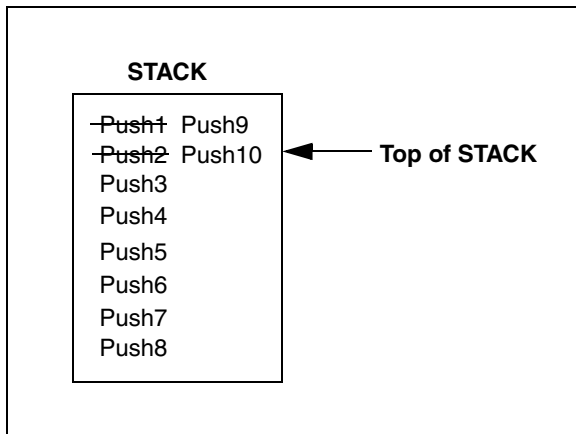
2.3.1 STACK

The stack allows a combination of up to 8 program calls and interrupts to occur. The stack contains the return address from this branch in program execution.

Midrange devices have an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not modified when the stack is PUSHed or POPed.

After the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on). An example of the overwriting of the stack is shown in Figure 2-10.

FIGURE 2-10: STACK MODIFICATION



2.4 Program Memory Paging

The CALL and GOTO instructions provide 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is pushed onto the stack. Therefore, manipulation of the PCLATH<4:3> bits are not required for the return instructions (which POPs the address from the stack).

Note: PIC16C72 Series devices ignore paging bit PCLATH<4>. The use of PCLATH<4> as a general purpose read/write bit is not recommended since this may affect upward compatibility with future products.

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 2-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

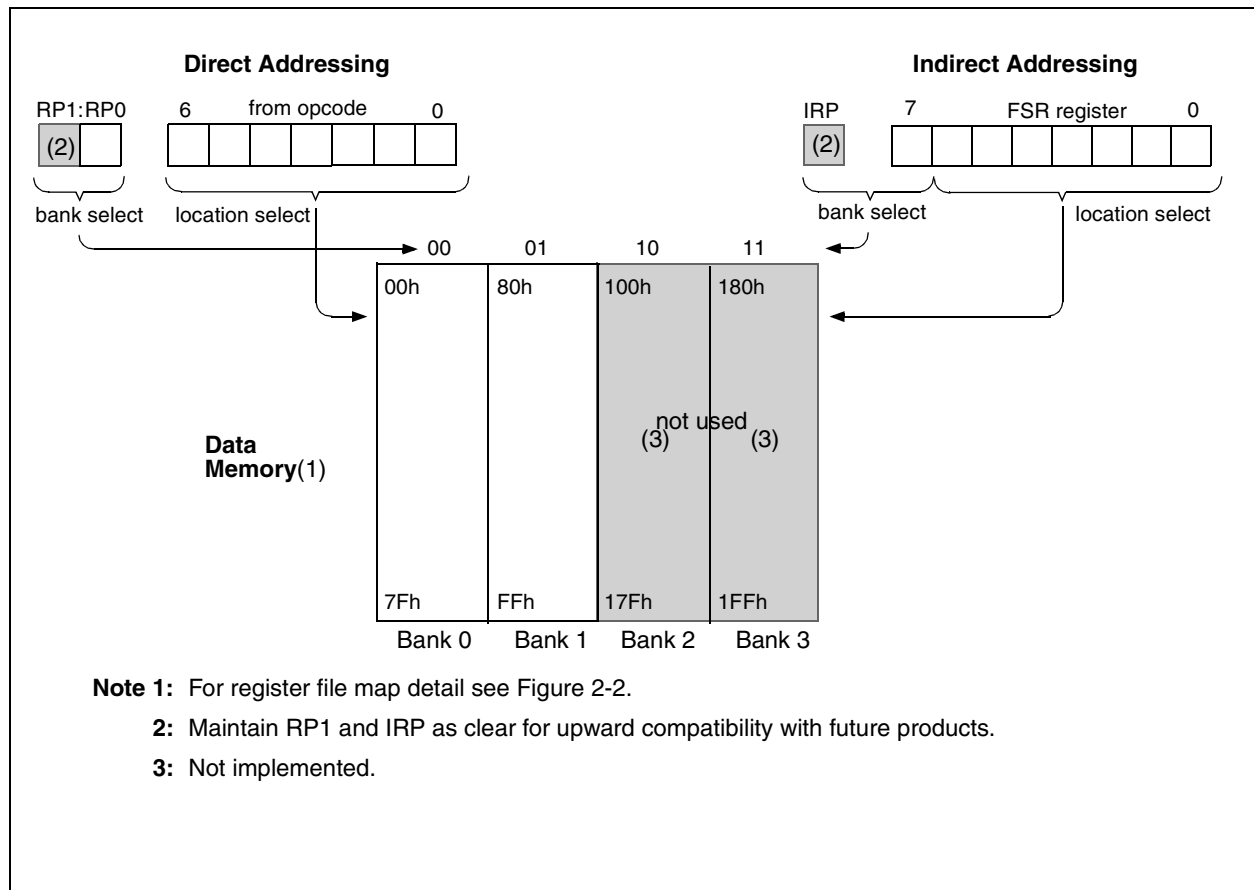
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```

movlw 0x20 ;initialize pointer
movwf FSR ; to RAM
NEXT   clrf INDF ;clear INDF register
       incf FSR ;inc pointer
       btfss FSR,4 ;all done?
       goto NEXT ;NO, clear next
CONTINUE
       : ;YES, continue
    
```

FIGURE 2-11: DIRECT/INDIRECT ADDRESSING



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NOTES:

3.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the PIC® Mid-Range MCU Reference Manual, DS33023.

3.1 PORTA and the TRISA Register

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, these pins are configured as analog inputs and read as '0'.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 3-1: INITIALIZING PORTA

```
BCF STATUS, RP0 ;
CLRF PORTA      ; Initialize PORTA by
                 ; clearing output
                 ; data latches
BSF STATUS, RP0 ; Select Bank 1
MOVLW 0xCF      ; Value used to
                 ; initialize data
                 ; direction
MOVWF TRISA     ; Set RA<3:0> as inputs
                 ; RA<5:4> as outputs
                 ; TRISA<7:6> are always
                 ; read as '0'.
```

FIGURE 3-1: BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS

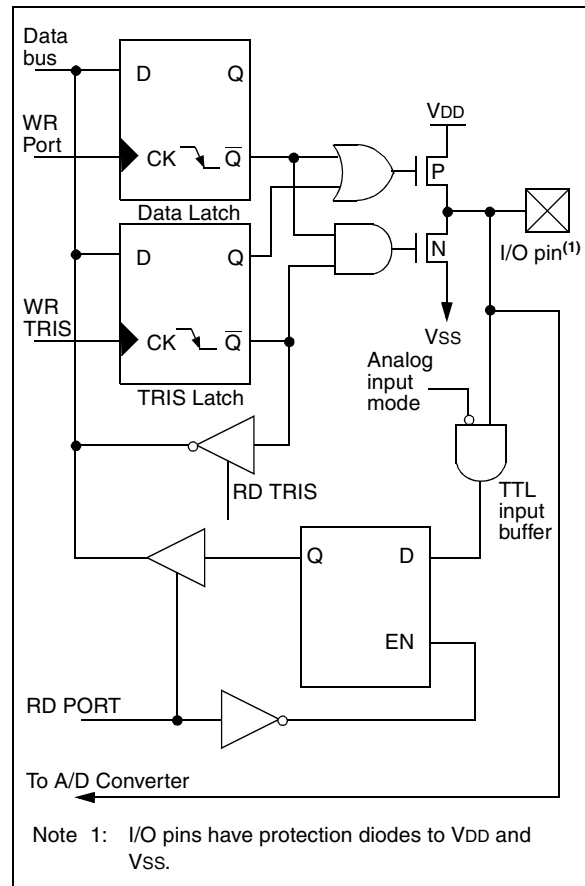
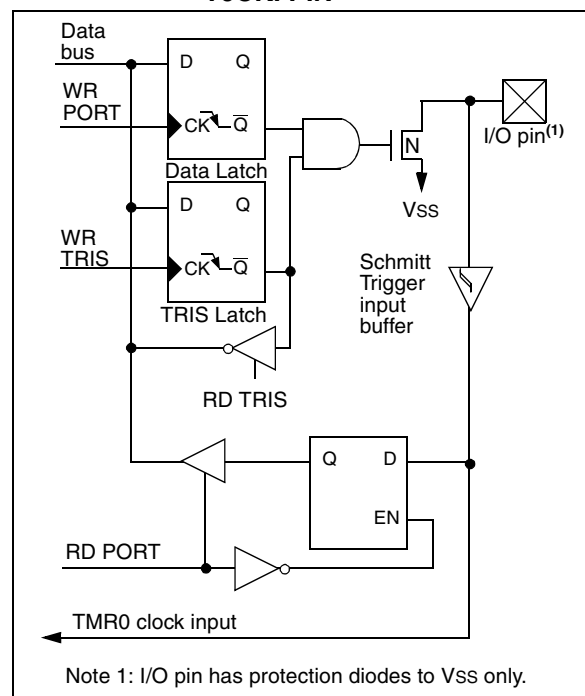


FIGURE 3-2: BLOCK DIAGRAM OF RA4/T0CKI PIN



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TABLE 3-1 PORTA FUNCTIONS

| Name | Bit# | Buffer | Function |
|---------------------------|------|--------|--|
| RA0/AN0 | bit0 | TTL | Input/output or analog input |
| RA1/AN1 | bit1 | TTL | Input/output or analog input |
| RA2/AN2 | bit2 | TTL | Input/output or analog input |
| RA3/AN3/VREF | bit3 | TTL | Input/output or analog input or VREF |
| RA4/T0CKI | bit4 | ST | Input/output or external clock input for Timer0 Output is open drain type |
| RA5/ \overline{SS} /AN4 | bit5 | TTL | Input/output or slave select input for synchronous serial port or analog input |

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2 SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|--------|-------|-------|-------------------------------|-------|-------|-------|-------|-------|--------------------------|------------------------------|
| 05h | PORTA | — | — | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --0x 0000 | --0u 0000 |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | ---- -000 | ---- -000 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

3.2 PORTB and the TRISB Register

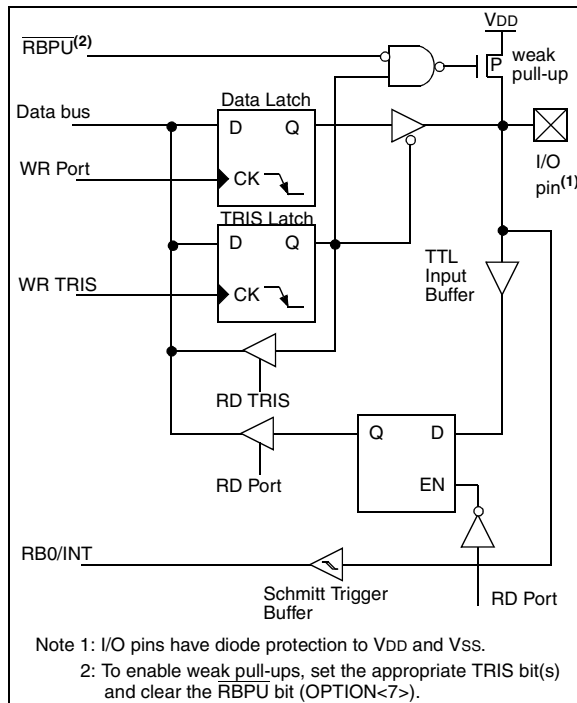
PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, i.e., put the contents of the output latch on the selected pin.

EXAMPLE 3-1: INITIALIZING PORTB

```
BCF    STATUS, RP0 ;
CLRF   PORTB      ; Initialize PORTB by
                  ; clearing output
                  ; data latches
BSF    STATUS, RP0 ; Select Bank 1
MOVLW  0xCF       ; Value used to
                  ; initialize data
                  ; direction
MOVWF  TRISB      ; Set RB<3:0> as inputs
                  ; RB<5:4> as outputs
                  ; RB<7:6> as outputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBP}}\text{U}$ (OPTION<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

FIGURE 3-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

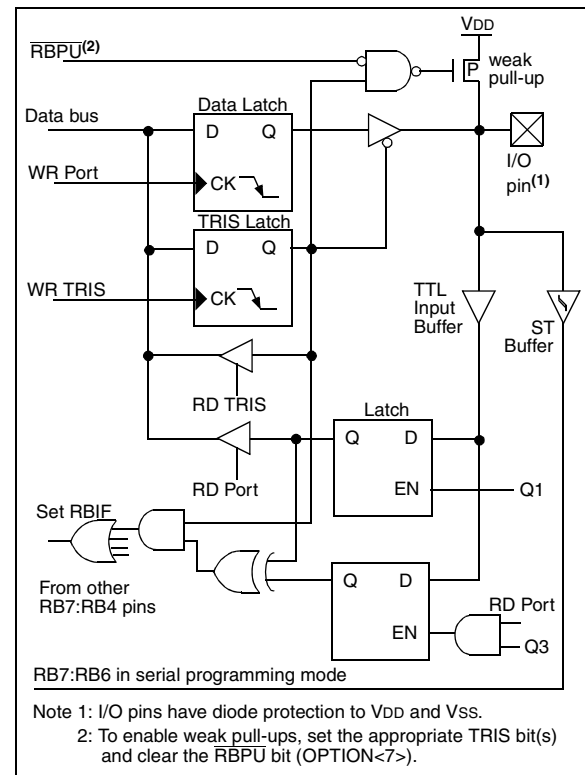
This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Any read or write of PORTB. This will end the mismatch condition.
- Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition, and allow flag bit RBIF to be cleared.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 3-4: BLOCK DIAGRAM OF RB7:RB4 PINS



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TABLE 3-3 PORTB FUNCTIONS

| Name | Bit# | Buffer | Function |
|---------|------|-----------------------|---|
| RB0/INT | bit0 | TTL/ST ⁽¹⁾ | Input/output pin or external interrupt input. Internal software programmable weak pull-up. |
| RB1 | bit1 | TTL | Input/output pin. Internal software programmable weak pull-up. |
| RB2 | bit2 | TTL | Input/output pin. Internal software programmable weak pull-up. |
| RB3 | bit3 | TTL | Input/output pin. Internal software programmable weak pull-up. |
| RB4 | bit4 | TTL | Input/output pin (with interrupt on change). Internal software programmable weak pull-up. |
| RB5 | bit5 | TTL | Input/output pin (with interrupt on change). Internal software programmable weak pull-up. |
| RB6 | bit6 | TTL/ST ⁽²⁾ | Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock. |
| RB7 | bit7 | TTL/ST ⁽²⁾ | Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data. |

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 3-4 SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|-----------|--------|-------------------------------|--------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------------|
| 06h, 106h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | uuuu uuuu |
| 86h, 186h | TRISB | PORTB Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 81h, 181h | OPTION | RBP \bar{U} | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

3.3 PORTC and the TRISC Register

PORTC is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (=1) will make the corresponding PORTC pin an input, i.e., put the corresponding output driver in a hi-impedance mode. Clearing a TRISC bit (=0) will make the corresponding PORTC pin an output, i.e., put the contents of the output latch on the selected pin.

PORTC is multiplexed with several peripheral functions (Table 3-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (*BSF*, *BCF*, *XORWF*) with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

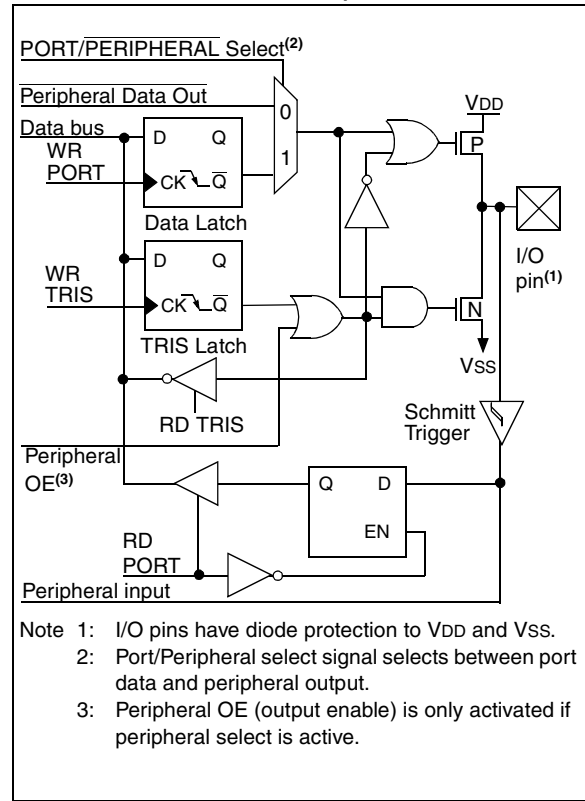
EXAMPLE 3-1: INITIALIZING PORTC

```
BCF    STATUS, RP0    ; Select Bank 0
CLRF  PORTC          ; Initialize PORTC by
                    ; clearing output
                    ; data latches

BSF    STATUS, RP0    ; Select Bank 1
MOVLW 0xCF           ; Value used to
                    ; initialize data
                    ; direction

MOVWF  TRISC         ; Set RC<3:0> as inputs
                    ; RC<5:4> as outputs
                    ; RC<7:6> as inputs
```

FIGURE 3-5: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



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TABLE 3-5 PORTC FUNCTIONS

| Name | Bit# | Buffer Type | Function |
|-----------------|------|-------------|---|
| RC0/T1OSO/T1CKI | bit0 | ST | Input/output port pin or Timer1 oscillator output/Timer1 clock input |
| RC1/T1OSI | bit1 | ST | Input/output port pin or Timer1 oscillator input |
| RC2/CCP1 | bit2 | ST | Input/output port pin or Capture1 input/Compare1 output/PWM1 output |
| RC3/SCK/SCL | bit3 | ST | RC3 can also be the synchronous serial clock for both SPI and I ² C modes. |
| RC4/SDI/SDA | bit4 | ST | RC4 can also be the SPI Data In (SPI mode) or data I/O (I ² C mode). |
| RC5/SDO | bit5 | ST | Input/output port pin or Synchronous Serial Port data output |
| RC6 | bit6 | ST | Input/output port pin |
| RC7 | bit7 | ST | Input/output port pin |

Legend: ST = Schmitt Trigger input

TABLE 3-6 SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|-------|-------------------------------|-------|-------|-------|-------|-------|-------|-------|--------------------------|------------------------------|
| 07h | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | uuuu uuuu |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged.

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- Internal or external clock select
- Edge select for external clock
- 8-bit software programmable prescaler
- Interrupt on overflow from FFh to 00h

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC® Mid-Range MCU Reference Manual, DS33023.

4.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

Additional information on external clock requirements is available in the PIC® Mid-Range MCU Reference Manual, DS33023.

4.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

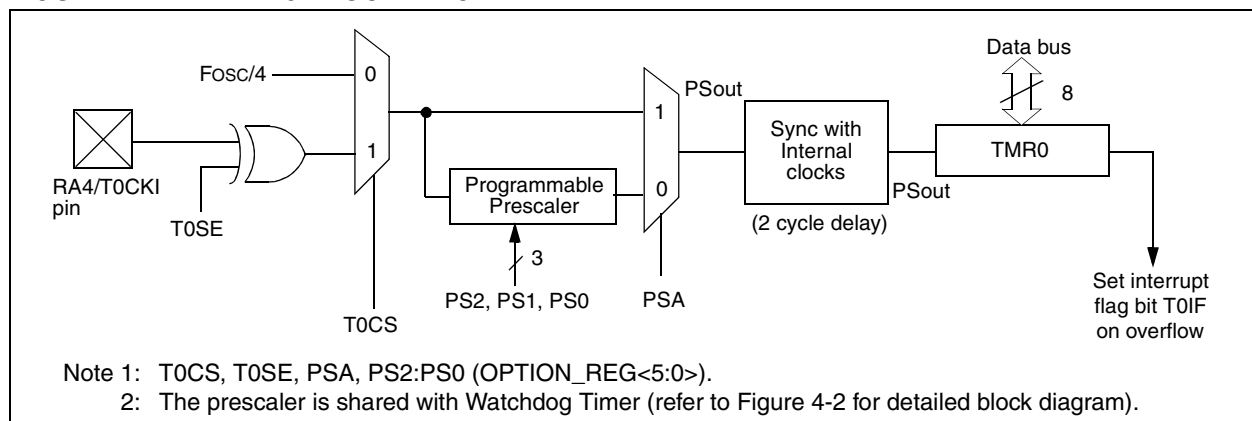
Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

FIGURE 4-1: TIMER0 BLOCK DIAGRAM



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4.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, a specific instruction sequence (shown in the PIC® Mid-Range MCU Reference Manual, DS3023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

4.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 4-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER

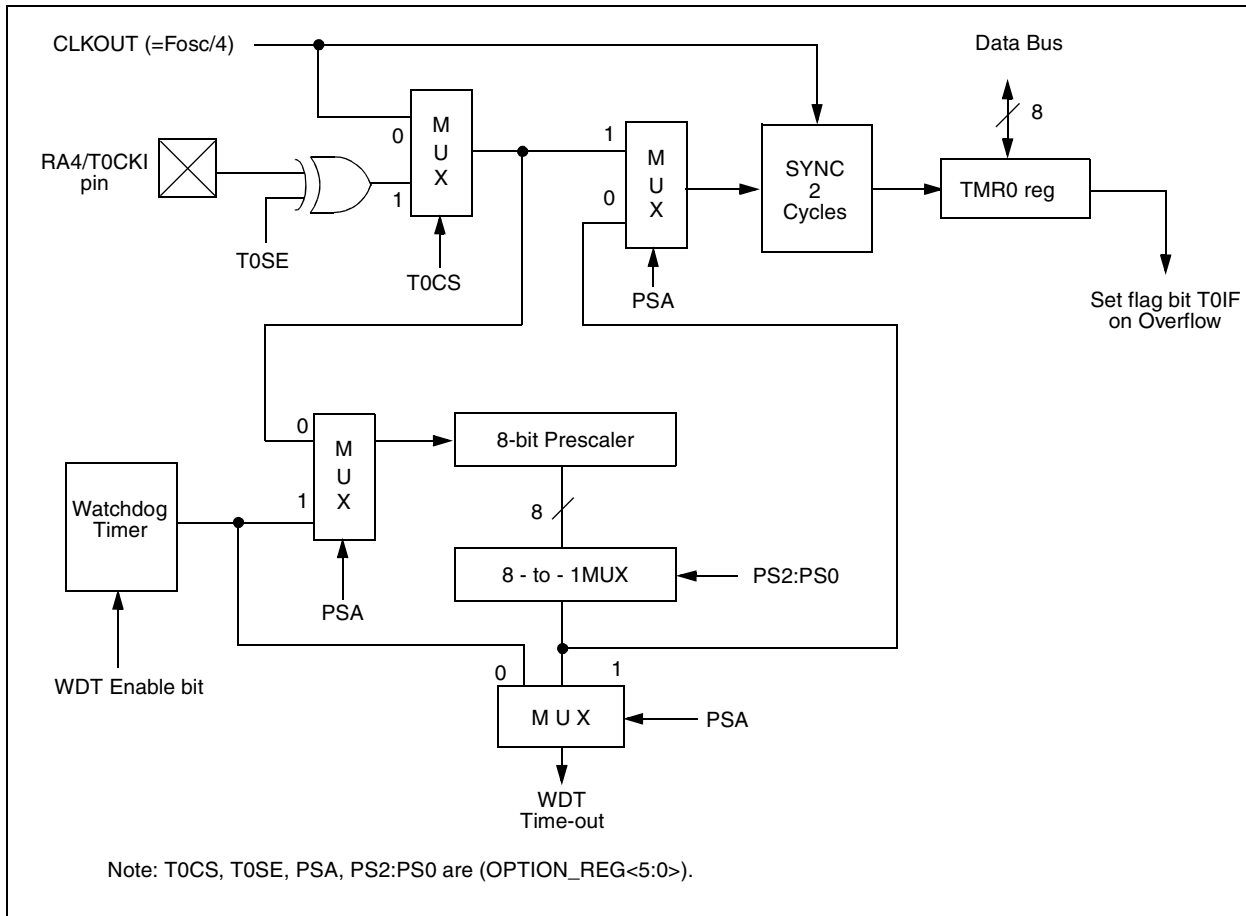


TABLE 4-1 REGISTERS ASSOCIATED WITH TIMER0

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|--------------------|------------|--------------------------|--------|-------------------------------|-------|-------|-------|-------|-------|--------------------|---------------------------|
| 01h,101h | TMR0 | Timer0 module's register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Bh,8Bh, 10Bh,18Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 81h,181h | OPTION_REG | RBPU | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

5.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
(Two 8-bit registers; TMR1H and TMR1L)
- Readable and writable (Both registers)
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- Reset from CCP module trigger

Timer1 has a control register, shown in Figure 5-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 5-2 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PIC® Mid-Range MCU Reference Manual, DS33023.

5.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored.

Timer1 also has an internal “reset input”. This reset can be generated by the CCP module (Section 7.0).

FIGURE 5-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

| | | | | | | | |
|------|-----|---------|---------|---------|---------------------|--------|--------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | $\overline{T1SYNC}$ | TMR1CS | TMR1ON |
| bit7 | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3: **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off
Note: The oscillator inverter and feedback resistor are turned off to eliminate power drain

bit 2: **$\overline{T1SYNC}$:** Timer1 External Clock Input Synchronization Control bit

TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input

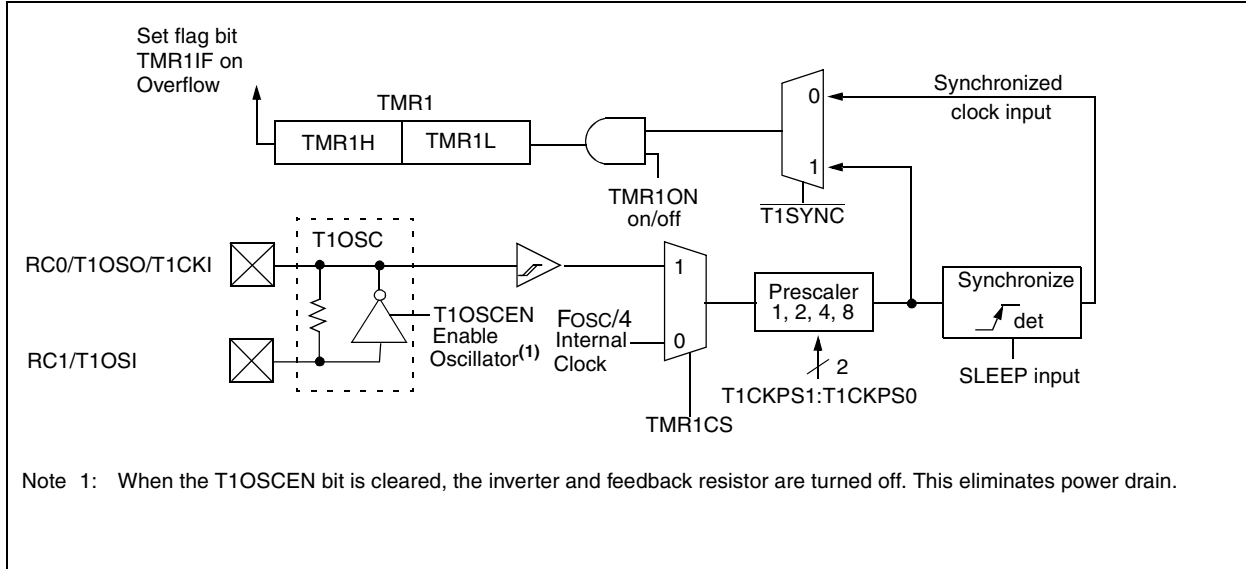
TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0: **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

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FIGURE 5-2: TIMER1 BLOCK DIAGRAM



5.2 Timer1 Oscillator

A crystal oscillator circuit is built in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 5-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

TABLE 5-1 CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

| Osc Type | Freq | C1 | C2 |
|--|-----------------------|----------|-------|
| LP | 32 kHz | 33 pF | 33 pF |
| | 100 kHz | 15 pF | 15 pF |
| | 200 kHz | 15 pF | 15 pF |
| These values are for design guidance only. | | | |
| Crystals Tested: | | | |
| 32.768 kHz | Epson C-001R32.768K-A | ± 20 PPM | |
| 100 kHz | Epson C-2 100.00 KC-P | ± 20 PPM | |
| 200 kHz | STD XTL 200.000 kHz | ± 20 PPM | |
| Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time. 2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components. | | | |

5.3 Timer1 Interrupt

The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit TMR1IE (PIE1<0>).

5.4 Resetting Timer1 using a CCP Trigger Output

If the CCP module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note: The special event triggers from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

TABLE 5-2 REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|--------|---|-------|---------|---------|---------|--------|--------|--------|--------------------|---------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | TOIE | INTE | RBIE | TOIF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 0Eh | TMR1L | Holding register for the Least Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Fh | TMR1H | Holding register for the Most Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10h | T1CON | — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | TMR1CS | TMR1ON | --00 0000 | --uu uuuu |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: These bits are unimplemented, read as '0'.

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NOTES:

6.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (Both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match of PR2
- SSP module optional use of TMR2 output to generate clock shift

Timer2 has a control register, shown in Figure 6-2. Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 6-1 is a simplified block diagram of the Timer2 module.

Additional information on timer modules is available in the PIC® Mid-Range MCU Reference Manual, DS33023.

6.1 Timer2 Operation

Timer2 can be used as the PWM time-base for PWM mode of the CCP module.

The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset, \overline{MCLR} reset, Watchdog Timer reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

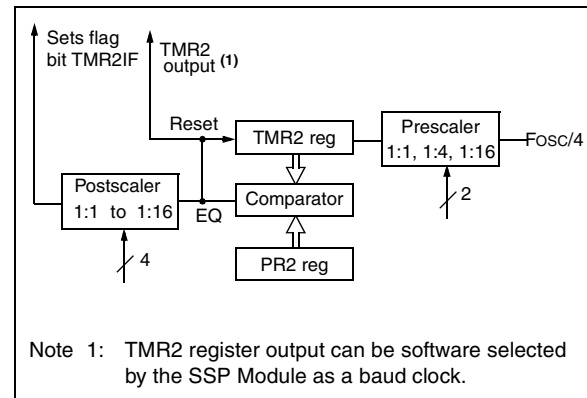
6.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

6.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module which optionally uses it to generate shift clock.

FIGURE 6-1: TIMER2 BLOCK DIAGRAM



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FIGURE 6-2: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

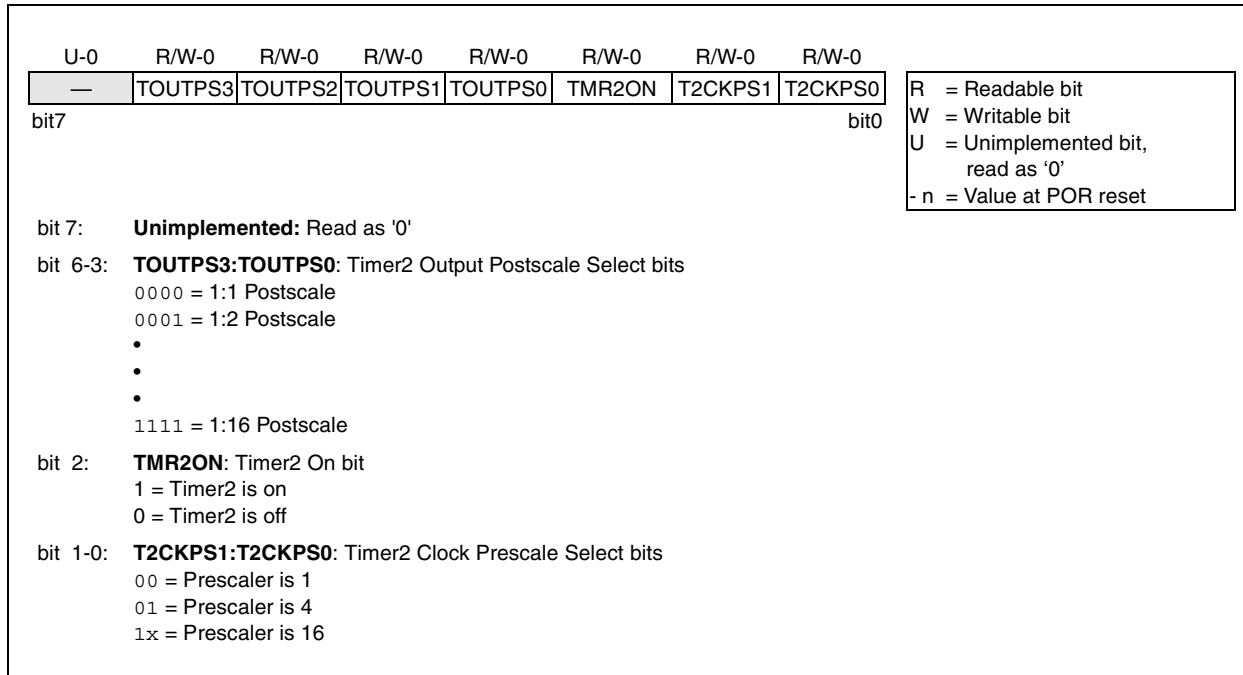


TABLE 6-1 REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|--------|--------------------------|---------|---------|---------|---------|--------|---------|---------|--------------------|---------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 11h | TMR2 | Timer2 module's register | | | | | | | | 0000 0000 | 0000 0000 |
| 12h | T2CON | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| 92h | PR2 | Timer2 Period Register | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.
 2: These bits are unimplemented, read as '0'.

7.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The CCP (Capture/Compare/PWM) module contains a 16-bit register which can operate as a 16-bit capture register, as a 16-bit compare register or as a PWM master/slave Duty Cycle register. Table 7-1 shows the timer resources of the CCP module modes.

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. All are readable and writable.

Additional information on the CCP module is available in the PIC[®] Mid-Range MCU Reference Manual, DS33023.

TABLE 7-1 CCP MODE - TIMER RESOURCE

| CCP Mode | Timer Resource |
|----------|----------------|
| Capture | Timer1 |
| Compare | Timer1 |
| PWM | Timer2 |

FIGURE 7-1: CCP1CON REGISTER (ADDRESS 17h)

| | | | | | | | | |
|------|-----|-------|-------|--------|--------|--------|--------|------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
| — | — | CCP1X | CCP1Y | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | |
| bit7 | | | | | | | | bit0 |

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **CCP1X:CCP1Y:** PWM Least Significant bits
 Capture Mode: Unused
 Compare Mode: Unused
 PWM Mode: These bits are the two LSBs of the PWM duty cycle. The eight MSBs are found in CCPR1L.

bit 3-0: **CCP1M3:CCP1M0:** CCP1 Mode Select bits
 0000 = Capture/Compare/PWM off (resets CCP1 module)
 0100 = Capture mode, every falling edge
 0101 = Capture mode, every rising edge
 0110 = Capture mode, every 4th rising edge
 0111 = Capture mode, every 16th rising edge
 1000 = Compare mode, set output on match (CCP1IF bit is set)
 1001 = Compare mode, clear output on match (CCP1IF bit is set)
 1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
 1011 = Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 and starts an A/D conversion (if A/D module is enabled))
 11xx = PWM mode

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7.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

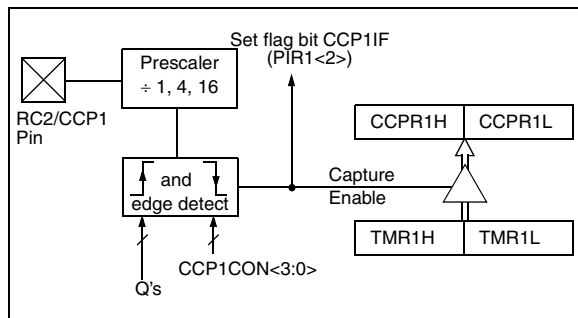
An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. It must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value will be lost.

7.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

FIGURE 7-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode, the capture operation may not work.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF following any such change in operating mode.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF   CCP1CON      ;Turn CCP module off
MOVLW  NEW_CAPT_PS  ;Load the W reg with
                                ; the new prescaler
                                ; mode value and CCP ON
MOVWF  CCP1CON      ;Load CCP1CON with this
                                ; value
```

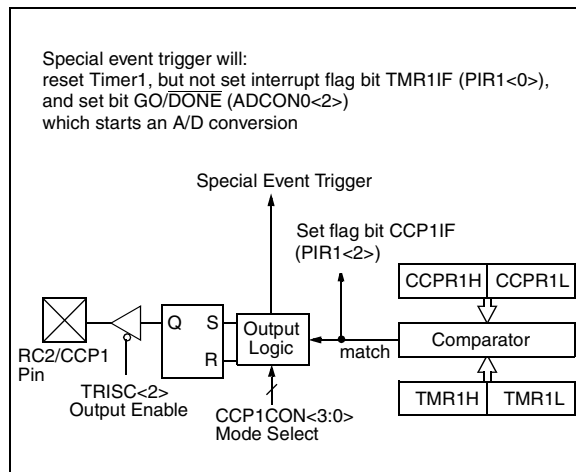
7.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- driven High
- driven Low
- remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 7-3: COMPARE MODE OPERATION BLOCK DIAGRAM



7.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

7.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

7.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

7.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCP1 resets the TMR1 register pair, and starts an A/D conversion (if the A/D module is enabled).

Note: The special event trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

TABLE 7-2 REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|---------|---|-------|---------|---------|---------|--------|--------|--------|--------------------------|---------------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | TOIE | INTE | RBIE | TOIF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 0Eh | TMR1L | Holding register for the Least Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 0Fh | TMR1H | Holding register for the Most Significant Byte of the 16-bit TMR1 register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 10h | T1CON | — | — | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNĀ | TMR1CS | TMR1ON | --00 0000 | --uu uuuu |
| 15h | CCPR1L | Capture/Compare/PWM register1 (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 16h | CCPR1H | Capture/Compare/PWM register1 (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 17h | CCP1CON | — | — | CCP1X | CCP1Y | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | --00 0000 | --00 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

Note 1: These bits/registers are unimplemented, read as '0'.

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7.3 PWM Mode

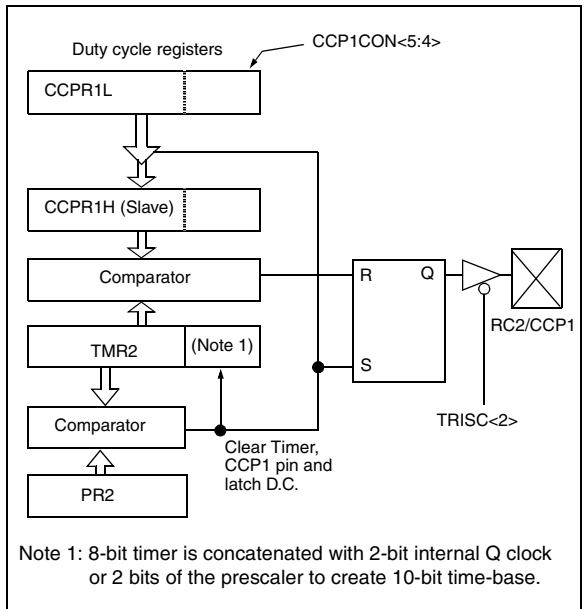
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 7-4 shows a simplified block diagram of the CCP module in PWM mode.

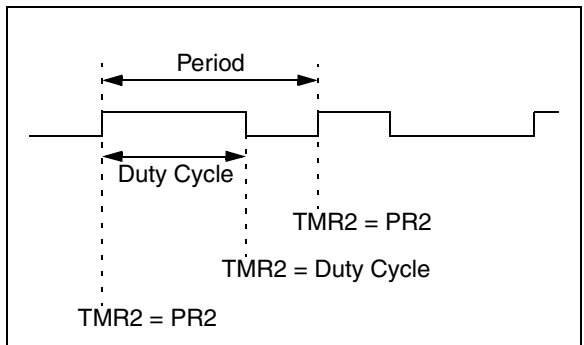
For a step by step procedure on how to set up the CCP module for PWM operation, see Section 7.3.3.

FIGURE 7-4: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 7-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 7-5: PWM OUTPUT



7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as $1 / [\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 6.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

7.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available: the CCPR1L contains the eight MSBs and the CCP1CON<5:4> contains the two LSBs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log\left(\frac{F_{osc}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period the CCP1 pin will not be cleared.

For an example PWM period and duty cycle calculation, see the PIC[®] Mid-Range MCU Reference Manual (DS33023).

7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.

3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 7-3 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

| PWM Frequency | 1.22 kHz | 4.88 kHz | 19.53 kHz | 78.12 kHz | 156.3 kHz | 208.3 kHz |
|----------------------------|----------|----------|-----------|-----------|-----------|-----------|
| Timer Prescaler (1, 4, 16) | 16 | 4 | 1 | 1 | 1 | 1 |
| PR2 Value | 0xFF | 0xFF | 0xFF | 0x3F | 0x1F | 0x17 |
| Maximum Resolution (bits) | 10 | 10 | 10 | 8 | 7 | 5.5 |

TABLE 7-4 REGISTERS ASSOCIATED WITH PWM AND TIMER2

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|---------|-------------------------------------|-------------|-------------|-------------|-------------|------------|-------------|-------------|--------------------------|---------------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | TOIE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 11h | TMR2 | Timer2 module's register | | | | | | | | 0000 0000 | 0000 0000 |
| 92h | PR2 | Timer2 module's period register | | | | | | | | 1111 1111 | 1111 1111 |
| 12h | T2CON | — | TOUTPS 3 | TOUTPS 2 | TOUTPS 1 | TOUTPS 0 | TMR2O N | T2CKPS 1 | T2CKPS 0 | -000 0000 | -000 0000 |
| 15h | CCPR1L | Capture/Compare/PWM register1 (LSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 16h | CCPR1H | Capture/Compare/PWM register1 (MSB) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 17h | CCP1CON | — | — | CCP1X | CCP1Y | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | --00 0000 | --00 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: These bits/registers are unimplemented, read as '0'.

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NOTES:

8.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

8.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

The SSP module in I²C mode works the same in all PIC16C72 series devices that have an SSP module. However the SSP Module in SPI mode has differences between the PIC16C72 and the PIC16CR72 device.

The register definitions and operational description of SPI mode has been split into two sections because of the differences between the PIC16C72 and the PIC16CR72 device. The default reset values of both the SPI modules is the same regardless of the device:

| | | |
|-----|--------------------------------------|----|
| 8.2 | SPI Mode for PIC16C72 | 40 |
| 8.3 | SPI Mode for PIC16CR72 | 43 |
| 8.4 | SSP I ² C Operation | 47 |

For an I²C Overview, refer to the PIC[®] Mid-Range MCU Reference Manual (DS33023). Also, refer to Application Note AN578, "Use of the SSP Module in the I²C Multi-Master Environment."

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8.2 SPI Mode for PIC16C72

This section contains register definitions and operational characteristics of the SPI module on the PIC16C72 device only.

Additional information on SPI operation may be found in the PIC[®] Mid-Range MCU Reference Manual, DS33023.

FIGURE 8-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h) (PIC16C72)

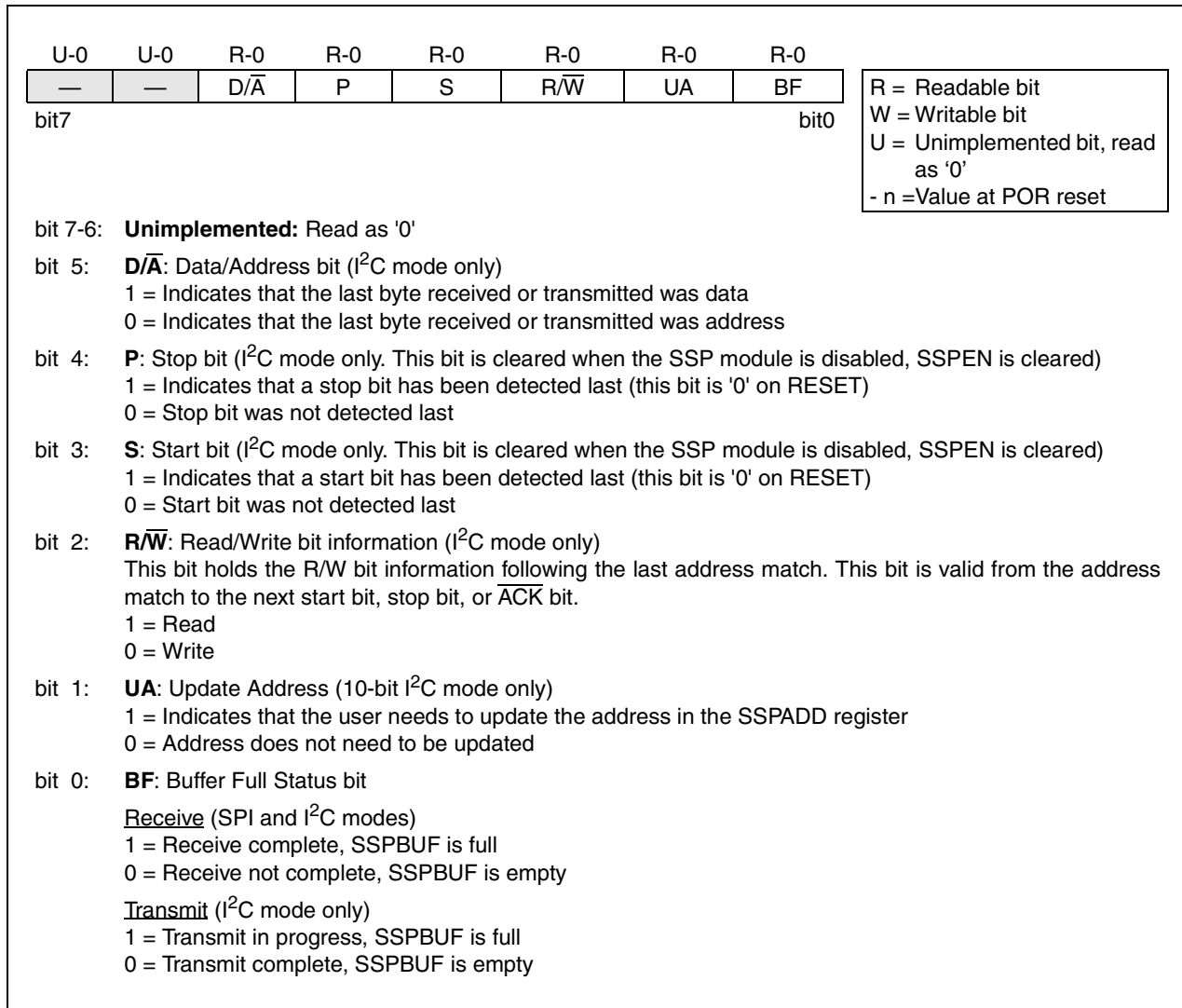


FIGURE 8-2: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h) (PIC16C72)

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
|-------|-------|-------|-------|-------|-------|-------|-------|------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | |
| bit7 | | | | | | | | bit0 |

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **WCOL**: Write Collision Detect bit
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6: **SSPOV**: Receive Overflow Detect bit
In SPI mode
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR register is lost. Overflow can only occur in slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In master operation, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
0 = No overflow
In I²C mode
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in transmit mode. SSPOV must be cleared in software in either mode.
0 = No overflow

bit 5: **SSPEN**: Synchronous Serial Port Enable bit
In SPI mode
1 = Enables serial port and configures SCK, SDO, and SDI as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In I²C mode
1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
0 = Disables serial port and configures these pins as I/O port pins
In both modes, when enabled, these pins must be properly configured as input or output.

bit 4: **CKP**: Clock Polarity Select bit
In SPI mode
1 = Idle state for clock is a high level. Transmit happens on falling edge, receive on rising edge.
0 = Idle state for clock is a low level. Transmit happens on rising edge, receive on falling edge.
In I²C mode
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch) (Used to ensure data setup time)

bit 3-0: **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits
0000 = SPI master operation, clock = Fosc/4
0001 = SPI master operation, clock = Fosc/16
0010 = SPI master operation, clock = Fosc/64
0011 = SPI master operation, clock = TMR2 output/2
0100 = SPI slave mode, clock = SCK pin. \overline{SS} pin control enabled.
0101 = SPI slave mode, clock = SCK pin. \overline{SS} pin control disabled. \overline{SS} can be used as I/O pin.
0110 = I²C slave mode, 7-bit address
0111 = I²C slave mode, 10-bit address
1011 = I²C firmware controlled master operation (slave idle)
1110 = I²C slave mode, 7-bit address with start and stop bit interrupts enabled
1111 = I²C slave mode, 10-bit address with start and stop bit interrupts enabled

8.2.1 OPERATION OF SSP MODULE IN SPI MODE - PIC16C72

A block diagram of the SSP Module in SPI Mode is shown in Figure 8-3.

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The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select (\overline{SS}) RA5/ \overline{SS} /AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>). These control bits allow the following to be specified:

- Master Operation (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Output/Input data on the Rising/Falling edge of SCK)
- Clock Rate (master operation only)
- Slave Select Mode (Slave mode only)

To enable the serial port, SSP enable bit SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear enable bit SSPEN, re-initialize SSPCON register, and then set enable bit SSPEN. This configures the SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (master operation) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- \overline{SS} must have TRISA<5> set (if implemented)

FIGURE 8-3: SSP BLOCK DIAGRAM (SPI MODE)

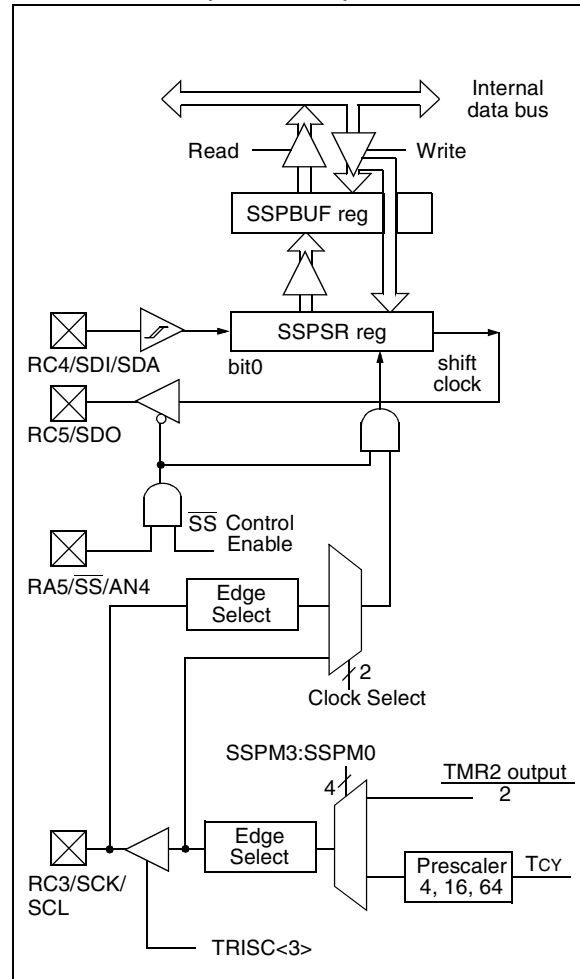


TABLE 8-1 REGISTERS ASSOCIATED WITH SPI OPERATION

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|---------|--|-------|-------------------|-------|-------|-------------------|--------|--------|--------------------|---------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 13h | SSPBUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 14h | SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 0000 0000 |
| 85h | TRISA | PORTA Data Direction Register | | | | | | | | --11 1111 | --11 1111 |
| 94h | SSPSTAT | — | — | D/ \overline{A} | P | S | R/ \overline{W} | UA | BF | --00 0000 | --00 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: These bits are unimplemented, read as '0'.

8.3 SPI Mode for PIC16CR72

This section contains register definitions and operational characteristics of the SPI module on the PIC16CR72 device only.

Additional information on SPI operation may be found in the PIC[®] Mid-Range MCU Reference Manual, DS33023.

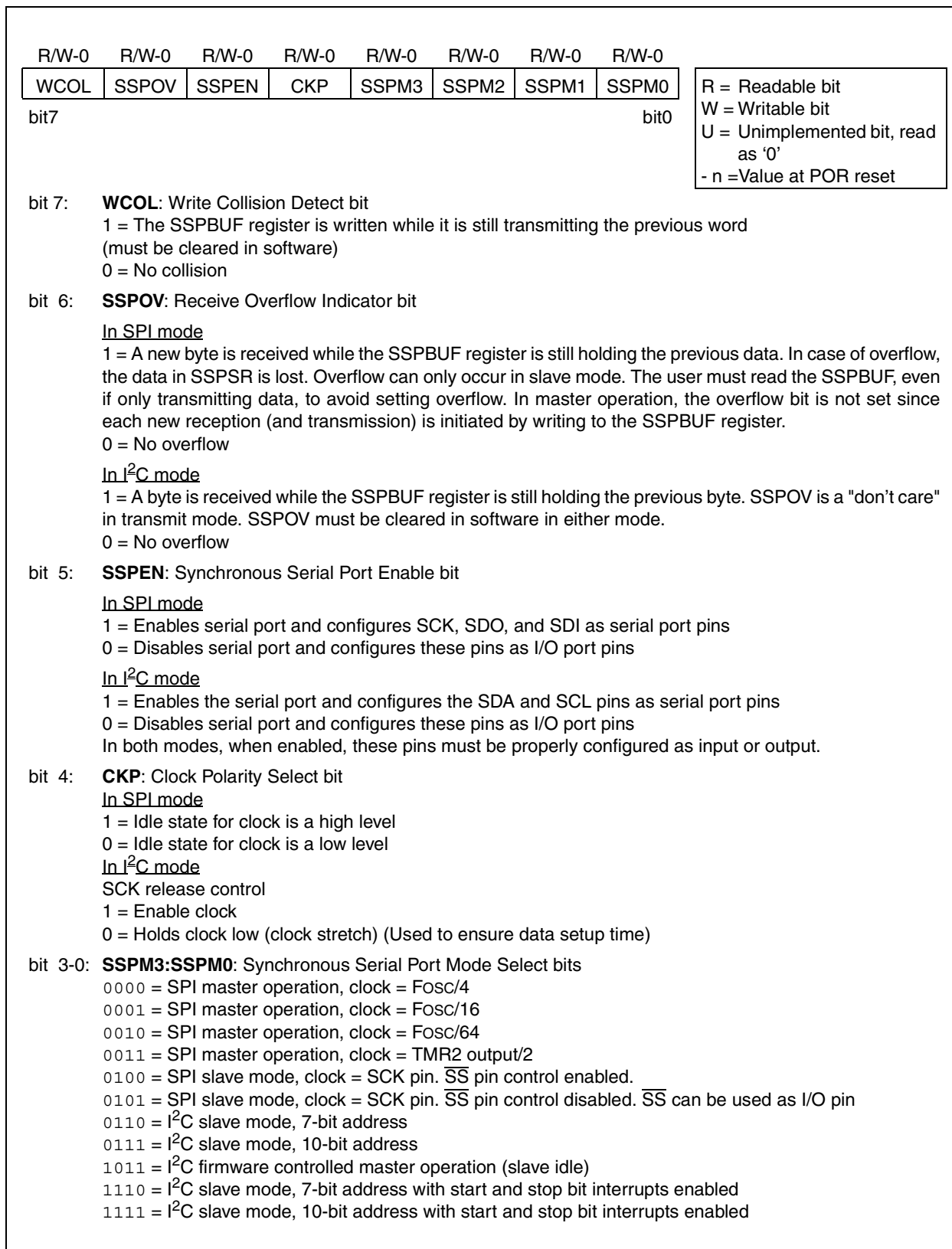
FIGURE 8-4: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h) (PIC16CR72)

| R/W-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|--|-------|--------------|-----|-----|--------------|-----|------|
| SMP | CKE | D/ \bar{A} | P | S | R/ \bar{W} | UA | BF |
| | | | | | | | bit0 |
| <p>bit 7: SMP: SPI data input sample phase <u>SPI Master Operation</u> 1 = Input data sampled at end of data output time 0 = Input data sampled at middle of data output time <u>SPI Slave Mode</u> SMP must be cleared when SPI is used in slave mode</p> <p>bit 6: CKE: SPI Clock Edge Select <u>CKP = 0</u> 1 = Data transmitted on rising edge of SCK 0 = Data transmitted on falling edge of SCK <u>CKP = 1</u> 1 = Data transmitted on falling edge of SCK 0 = Data transmitted on rising edge of SCK</p> <p>bit 5: D/\bar{A}: Data/\bar{A} Address bit (I²C mode only) 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address</p> <p>bit 4: P: Stop bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Start bit is detected last, SSPEN is cleared) 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET) 0 = Stop bit was not detected last</p> <p>bit 3: S: Start bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Stop bit is detected last, SSPEN is cleared) 1 = Indicates that a start bit has been detected last (this bit is '0' on RESET) 0 = Start bit was not detected last</p> <p>bit 2: R/\bar{W}: Read/Write bit information (I²C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or \bar{A}CK bit. 1 = Read 0 = Write</p> <p>bit 1: UA: Update Address (10-bit I²C mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated</p> <p>bit 0: BF: Buffer Full Status bit <u>Receive</u> (SPI and I²C modes) 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty <u>Transmit</u> (I²C mode only) 1 = Transmit in progress, SSPBUF is full 0 = Transmit complete, SSPBUF is empty</p> | | | | | | | |

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

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FIGURE 8-5: SSPCON: SYNC SERIAL PORT CONTROL REGISTER (ADDRESS 14h) (PIC16CR72)



8.3.1 OPERATION OF SSP MODULE IN SPI MODE - PIC16CR72

A block diagram of the SSP Module in SPI Mode is shown in Figure 8-6.

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally a fourth pin may be used when in a slave mode of operation:

- Slave Select (\overline{SS}) RA5/ \overline{SS} /AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Operation (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock Edge (Output data on rising/falling edge of SCK)
- Clock Rate (master operation only)
- Slave Select Mode (Slave mode only)

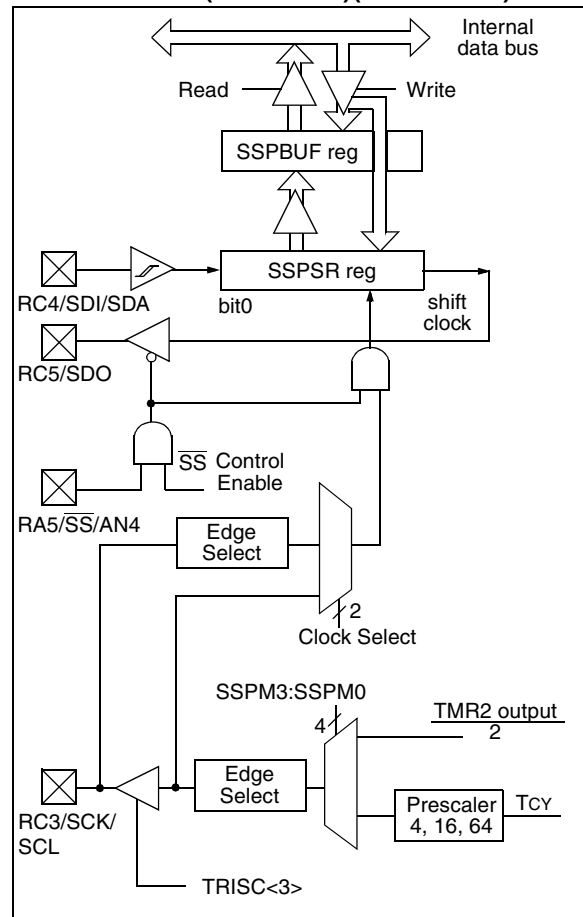
To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON register, and then set bit SSPEN. This configures the SDI, SDO, SCK, and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (master operation) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- \overline{SS} must have TRISA<5> set

Note: When the SPI is in Slave Mode with \overline{SS} pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the \overline{SS} pin is set to V_{DD}.

Note: If the SPI is used in Slave Mode with CKE = '1', then the \overline{SS} pin control must be enabled.

FIGURE 8-6: SSP BLOCK DIAGRAM (SPI MODE)(PIC16CR72)



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TABLE 8-2 REGISTERS ASSOCIATED WITH SPI OPERATION (PIC16CR72)

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other resets |
|---------|---------|--|-------|-------------------------------|-------|-------|--------------|--------|--------|--------------------------|---------------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | TOIE | INTE | RBIE | TOIF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 87h | TRISC | PORTC Data Direction Register | | | | | | | | 1111 1111 | 1111 1111 |
| 13h | SSPBUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 14h | SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 0000 0000 |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |
| 94h | SSPSTAT | SMP | CKE | D/ \bar{A} | P | S | R/ \bar{W} | UA | BF | 0000 0000 | 0000 0000 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: Always maintain these bits clear.

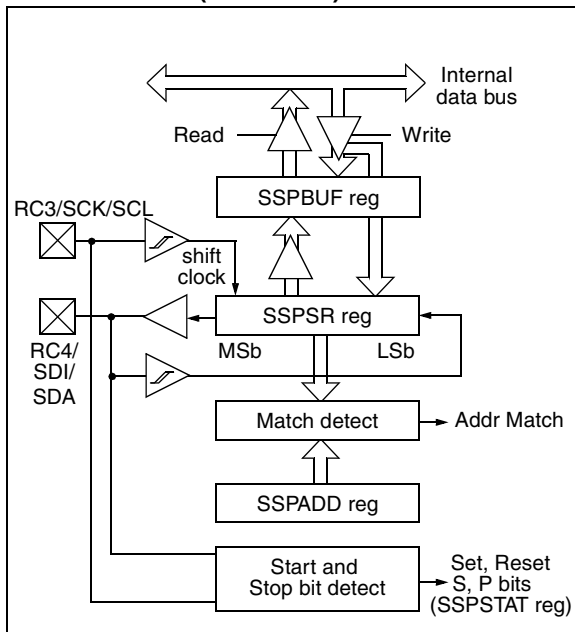
8.4 SSP I²C Operation

The SSP module in I²C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 8-7: SSP BLOCK DIAGRAM (I²C MODE)



The SSP module has five registers for I²C operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) - Not directly accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with start and stop bit interrupts enabled
- I²C Slave mode (10-bit address), with start and stop bit interrupts enabled
- I²C Firmware controlled master operation, slave is idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

Additional information on SSP I²C operation may be found in the PIC[®] Mid-Range MCU Reference Manual, DS33023.

8.4.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge (\overline{ACK}) pulse, and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this \overline{ACK} pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 8-3 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I²C specification as well as the requirement of the SSP module is shown in timing parameter #100 and parameter #101.

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8.4.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An $\overline{\text{ACK}}$ pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated if enabled) - on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit $\text{R}/\overline{\text{W}}$ (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address the first byte would equal

'1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address. The sequence of events for 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address, if match releases SCL line, this will clear bit UA.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

TABLE 8-3 DATA TRANSFER RECEIVED BYTE ACTIONS

| Status Bits as Data Transfer is Received | | SSPSR → SSPBUF | Generate $\overline{\text{ACK}}$ Pulse | Set bit SSPIF (SSP Interrupt occurs if enabled) |
|--|-------|----------------|--|---|
| BF | SSPOV | | | |
| 0 | 0 | Yes | Yes | Yes |
| 1 | 0 | No | No | Yes |
| 1 | 1 | No | No | Yes |
| 0 | 1 | No | No | Yes |

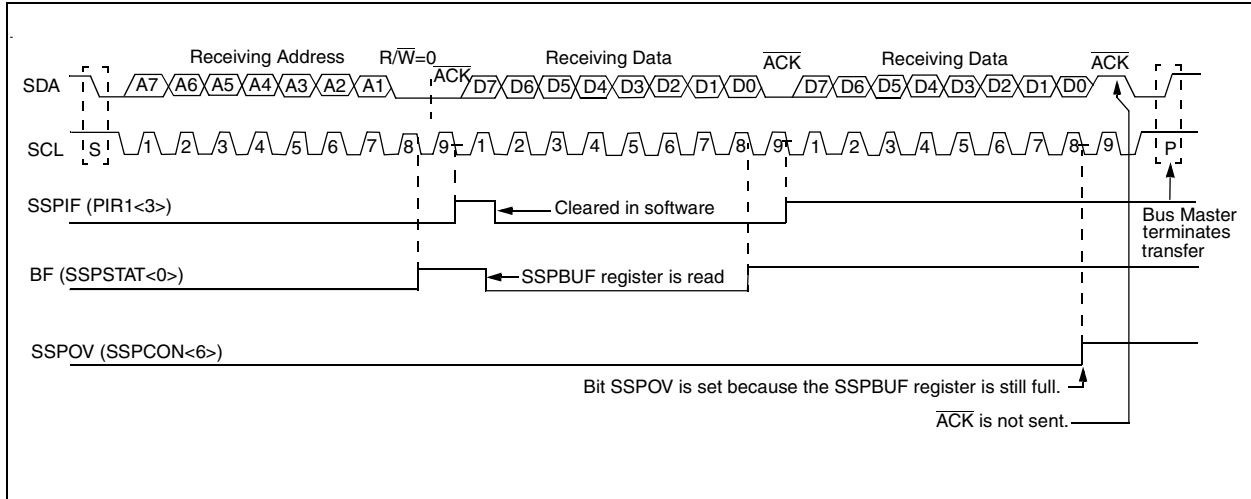
8.4.1.2 RECEPTION

When the $\overline{R/W}$ bit of the address byte is clear and an address match occurs, the $\overline{R/W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge (\overline{ACK}) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

FIGURE 8-8: I²C WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



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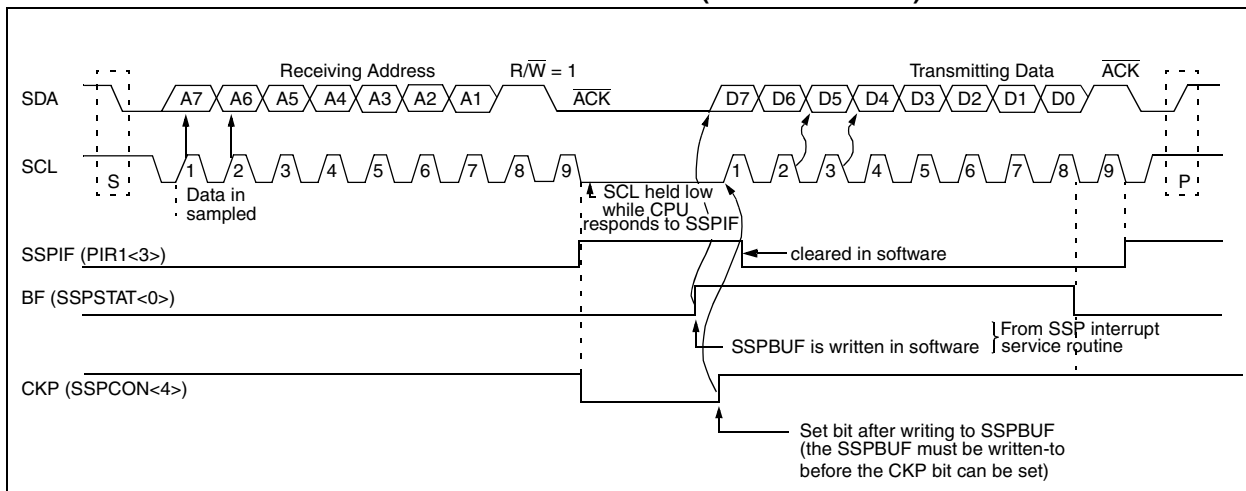
8.4.1.3 TRANSMISSION

When the R/\overline{W} bit of the incoming address byte is set and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The \overline{ACK} pulse will be sent on the ninth bit, and pin RC3/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 8-9).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the \overline{ACK} pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not \overline{ACK}), then the data transfer is complete. When the \overline{ACK} is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave then monitors for another occurrence of the START bit. If the SDA line was low (\overline{ACK}), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP.

FIGURE 8-9: I²C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



8.4.2 MASTER OPERATION

Master operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master operation, the SCL and SDA lines are manipulated in firmware by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received

Master operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master operation and slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on master operation, see AN554 - Software Implementation of I²C Bus Master.

8.4.3 MULTI-MASTER OPERATION

In multi-master operation, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

For more information on master operation, see AN578 - Use of the SSP Module in the of I²C Multi-Master Environment.

TABLE 8-4 REGISTERS ASSOCIATED WITH I²C OPERATION

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other resets |
|----------------------|---------|--|--------------------|-------|-------|-------|--------|--------|--------|-------------------|---------------------------|
| 0Bh, 8Bh, 10Bh, 18Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | (1) | ADIF | (1) | (1) | SSPIF | CCP1IF | TMR2IF | TMR1IF | 0000 0000 | 0000 0000 |
| 8Ch | PIE1 | (1) | ADIE | (1) | (1) | SSPIE | CCP1IE | TMR2IE | TMR1IE | 0000 0000 | 0000 0000 |
| 13h | SSPBUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 93h | SSPADD | Synchronous Serial Port (I ² C mode) Address Register | | | | | | | | 0000 0000 | 0000 0000 |
| 14h | SSPCON | WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 | 0000 0000 | 0000 0000 |
| 94h | SSPSTAT | SMP ⁽²⁾ | CKE ⁽²⁾ | D/Ā | P | S | R/W | UA | BF | 0000 0000 | 0000 0000 |
| 87h | TRISC | PORTC Data Direction register | | | | | | | | 1111 1111 | 1111 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by SSP module in SPI mode.

Note 1: These bits are unimplemented, read as '0'.

Note 2: The SMP and CKE bits are implemented on the PIC16CR72 only. On the PIC16C72, these two bits are unimplemented, read as '0'.

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NOTES:

9.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has five inputs for the PIC16C72/R72.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

Additional information on the A/D module is available in the PIC[®] Mid-Range MCU Reference Manual, DS33023.

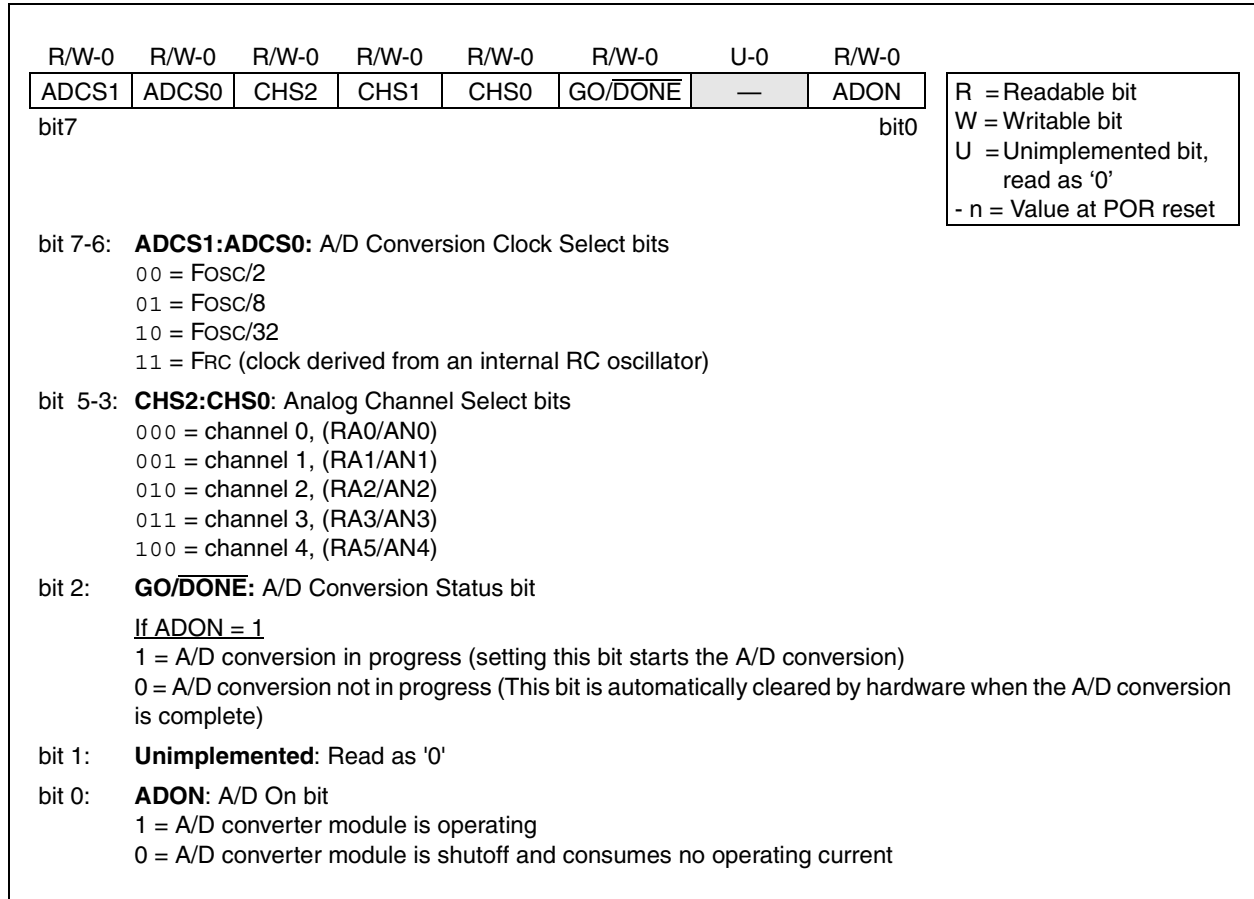
The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted.

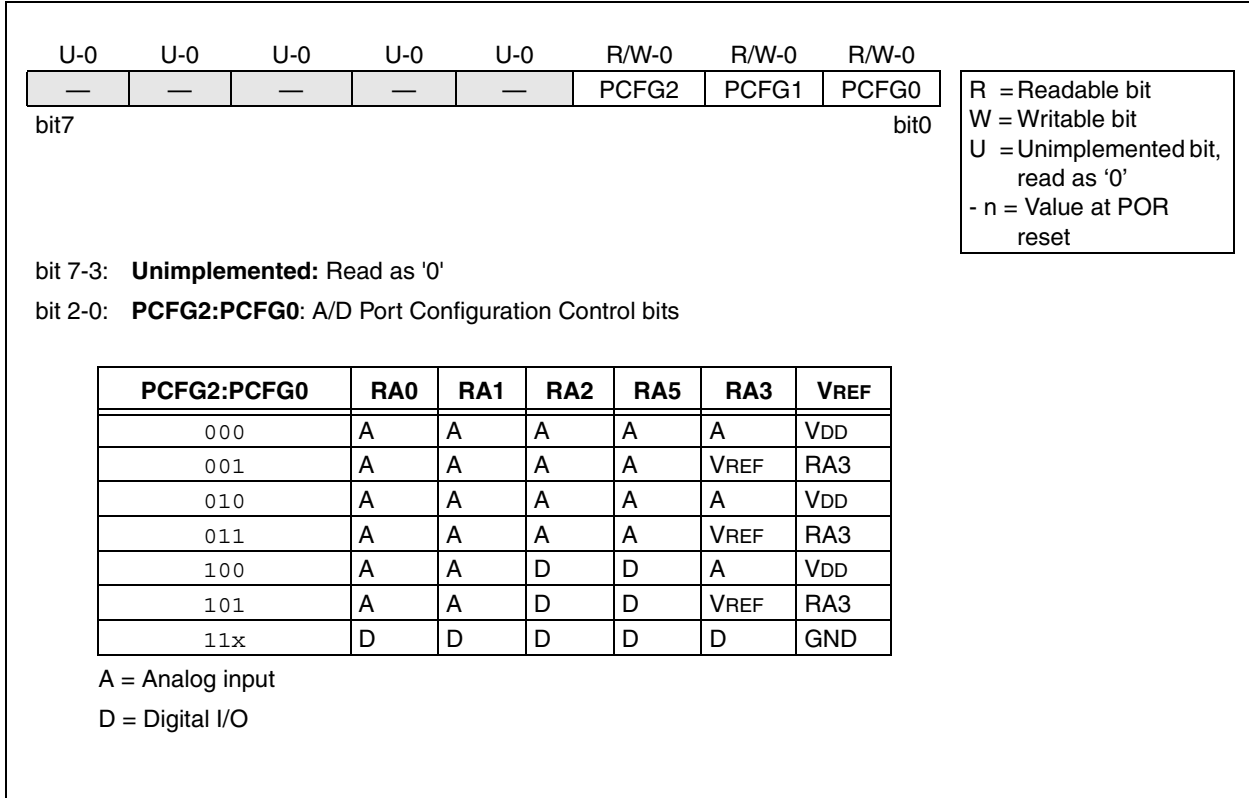
The ADCON0 register, shown in Figure 9-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 9-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

FIGURE 9-1: ADCON0 REGISTER (ADDRESS 1Fh)



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FIGURE 9-2: ADCON1 REGISTER (ADDRESS 9Fh)



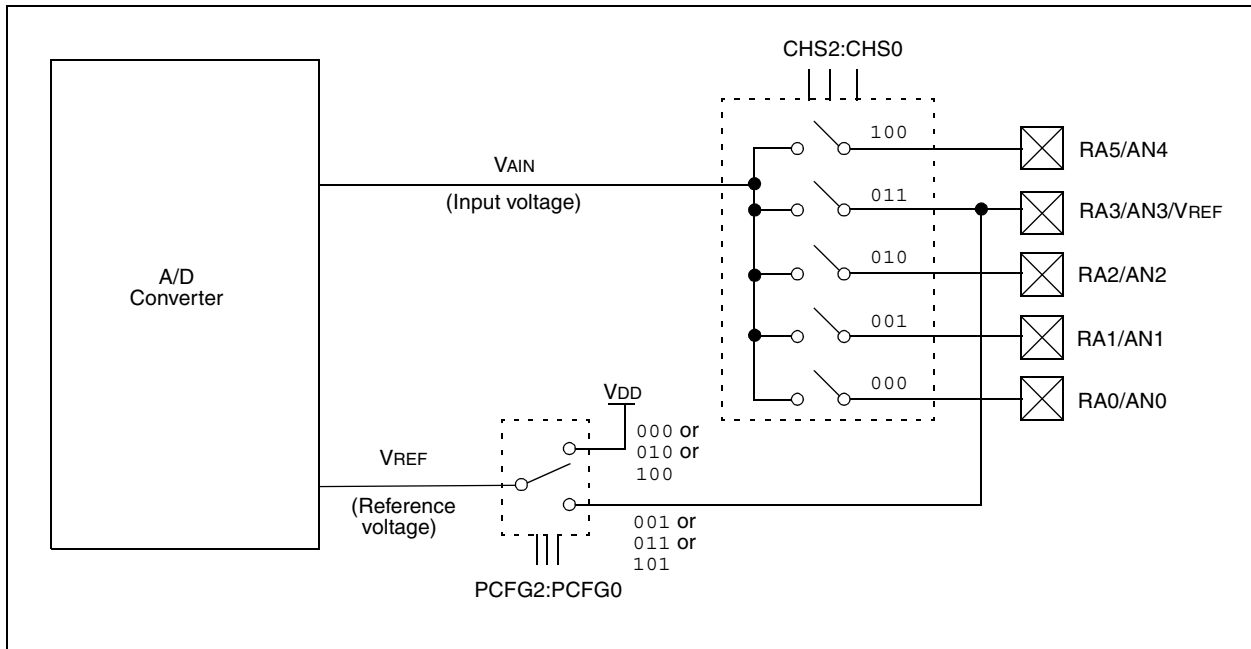
The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 9-3.

The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 9.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins / voltage reference / and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
 - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

FIGURE 9-3: A/D BLOCK DIAGRAM



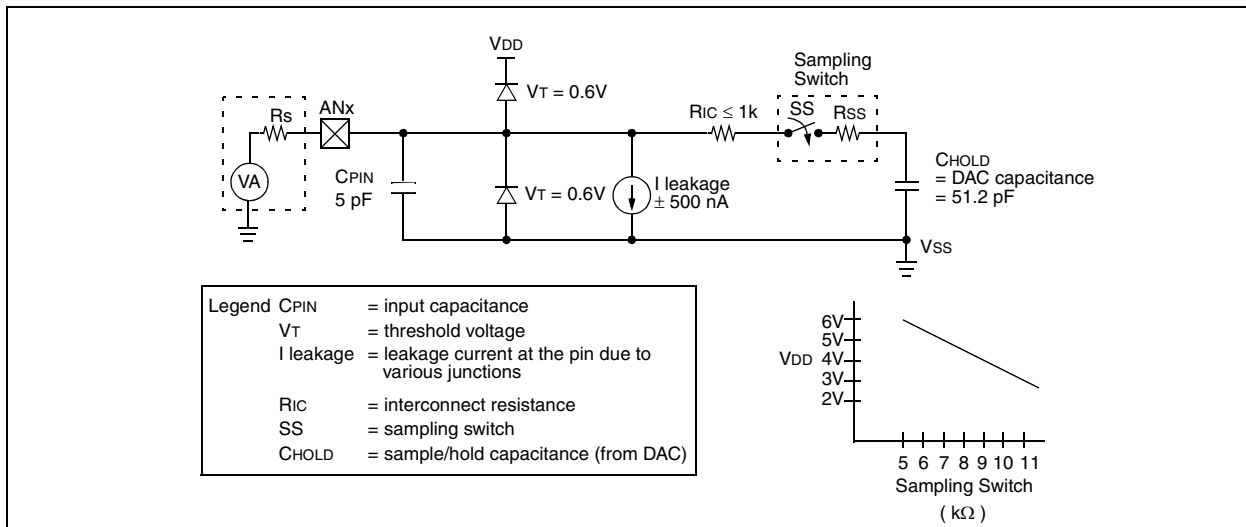
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9.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 9-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 10 kΩ.** After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, TACQ, see the PIC[®] Mid-Range MCU Reference Manual, DS33023. This equation calculates the acquisition time to within 1/2 LSb error (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

FIGURE 9-4: ANALOG INPUT MODEL



9.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5TAD per 8-bit conversion. The source of the A/D conversion clock is software selectable. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μ s.

Table 9-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

9.3 Configuring Analog Port Pins

The ADCON1, TRISA, and TRISE registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN4:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

TABLE 9-1 TAD vs. DEVICE OPERATING FREQUENCIES

| AD Clock Source (TAD) | | Device Frequency | | | |
|-----------------------|-------------|--------------------------------|--------------------------------|--------------------------------|------------------------------|
| Operation | ADCS1:ADCS0 | 20 MHz | 5 MHz | 1.25 MHz | 333.33 kHz |
| 2TOSC | 00 | 100 ns ⁽²⁾ | 400 ns ⁽²⁾ | 1.6 μ s | 6 μ s |
| 8TOSC | 01 | 400 ns ⁽²⁾ | 1.6 μ s | 6.4 μ s | 24 μ s ⁽³⁾ |
| 32TOSC | 10 | 1.6 μ s | 6.4 μ s | 25.6 μ s ⁽³⁾ | 96 μ s ⁽³⁾ |
| RC ⁽⁵⁾ | 11 | 2 - 6 μ s ^(1,4) | 2 - 6 μ s ^(1,4) | 2 - 6 μ s ^(1,4) | 2 - 6 μ s ⁽¹⁾ |

Legend: Shaded cells are outside of recommended range.

Note 1: The RC source has a typical TAD time of 4 μ s.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When device frequency is greater than 1 MHz, the RC A/D conversion clock source is recommended for sleep operation only.

5: For extended voltage devices (LC), please refer to Electrical Specifications section.

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9.4 A/D Conversions

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

9.5 Use of the CCP Trigger

An A/D conversion can be started by the “special event trigger” of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the

GO/DONE bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRES to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the “special event trigger” sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the “special event trigger” will be ignored by the A/D module, but will still reset the Timer1 counter.

TABLE 9-2 REGISTERS/BITS ASSOCIATED WITH A/D

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---------|--------|---------------------|-------|-------------------------------|-------|-------|---------|--------|--------|--------------------------|------------------------------|
| 0Bh,8Bh | INTCON | GIE | PEIE | T0IE | INTE | RBIE | T0IF | INTF | RBIF | 0000 000x | 0000 000u |
| 0Ch | PIR1 | — | ADIF | — | — | SSPIF | CCP1IF | TMR2IF | TMR1IF | -0-- 0000 | -0-- 0000 |
| 8Ch | PIE1 | — | ADIE | — | — | SSPIE | CCP1IE | TMR2IE | TMR1IE | -0-- 0000 | -0-- 0000 |
| 1Eh | ADRES | A/D Result Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 1Fh | ADCON0 | ADCS1 | ADCS0 | CHS2 | CHS1 | CHS0 | GO/DONE | — | ADON | 0000 00-0 | 0000 00-0 |
| 9Fh | ADCON1 | — | — | — | — | — | PCFG2 | PCFG1 | PCFG0 | ---- -000 | ---- -000 |
| 05h | PORTA | — | — | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --0x 0000 | --0u 0000 |
| 85h | TRISA | — | — | PORTA Data Direction Register | | | | | | --11 1111 | --11 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

10.0 SPECIAL FEATURES OF THE CPU

The PIC16C72 series has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-Circuit Serial Programming™

The PIC16CXXX family has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is sta-

ble. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

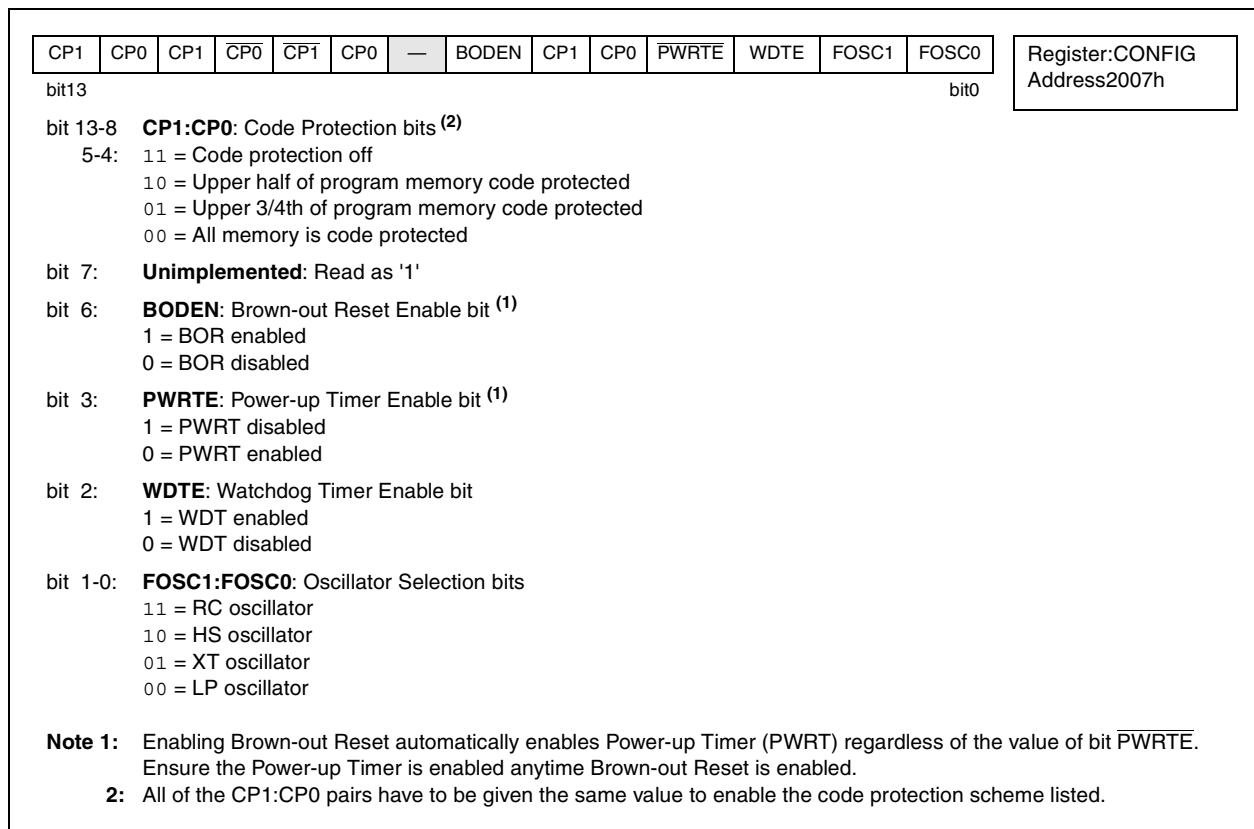
Additional information on special features is available in the PIC® Mid-Range MCU Family Reference Manual, DS33023.

10.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h - 3FFFh), which can be accessed only during programming.

FIGURE 10-1: CONFIGURATION WORD FOR PIC16C72/R72



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10.2 Oscillator Configurations

10.2.1 OSCILLATOR TYPES

The PIC16CXXX family can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

10.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 10-2). The PIC16CXXX family oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 10-3).

FIGURE 10-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)

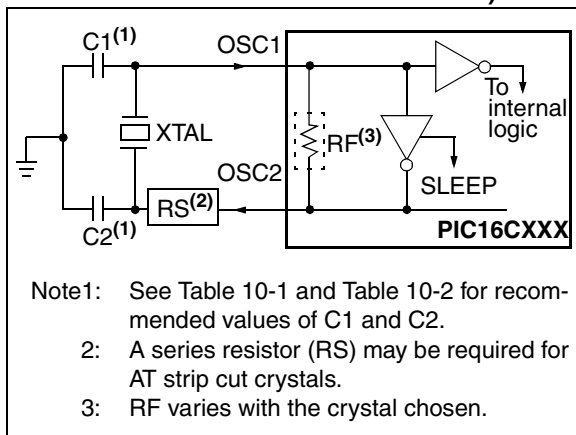


FIGURE 10-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

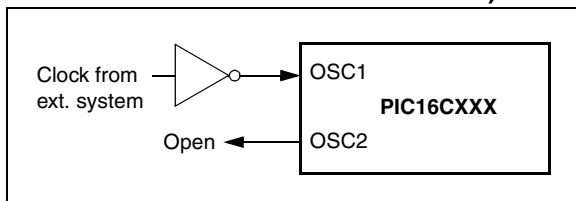


TABLE 10-1 CERAMIC RESONATORS

| Ranges Tested: | | | |
|---|------------------------|-------------|-------------|
| Mode | Freq | OSC1 | OSC2 |
| XT | 455 kHz | 68 - 100 pF | 68 - 100 pF |
| | 2.0 MHz | 15 - 68 pF | 15 - 68 pF |
| | 4.0 MHz | 15 - 68 pF | 15 - 68 pF |
| HS | 8.0 MHz | 10 - 68 pF | 10 - 68 pF |
| | 16.0 MHz | 10 - 22 pF | 10 - 22 pF |
| These values are for design guidance only. See notes at bottom of page. | | | |
| Resonators Used: | | | |
| 455 kHz | Panasonic EFO-A455K04B | ± 0.3% | |
| 2.0 MHz | Murata Erie CSA2.00MG | ± 0.5% | |
| 4.0 MHz | Murata Erie CSA4.00MG | ± 0.5% | |
| 8.0 MHz | Murata Erie CSA8.00MT | ± 0.5% | |
| 16.0 MHz | Murata Erie CSA16.00MX | ± 0.5% | |
| All resonators used did not have built-in capacitors. | | | |

TABLE 10-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

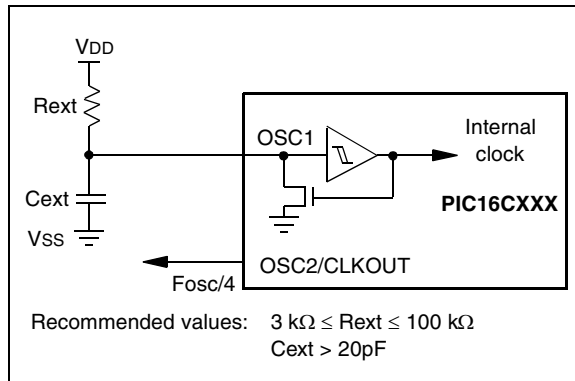
| Osc Type | Crystal Freq | Cap. Range C1 | Cap. Range C2 |
|---|------------------------|---------------|---------------|
| LP | 32 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15-33 pF | 15-33 pF |
| | 20 MHz | 15-33 pF | 15-33 pF |
| These values are for design guidance only. See notes at bottom of page. | | | |
| Crystals Used | | | |
| 32 kHz | Epson C-001R32.768K-A | ± 20 PPM | |
| 200 kHz | STD XTL 200.000KHz | ± 20 PPM | |
| 1 MHz | ECS ECS-10-13-1 | ± 50 PPM | |
| 4 MHz | ECS ECS-40-20-1 | ± 50 PPM | |
| 8 MHz | EPSON CA-301 8.000M-C | ± 30 PPM | |
| 20 MHz | EPSON CA-301 20.000M-C | ± 30 PPM | |

- Note 1: Recommended values of C1 and C2 are identical to the ranges tested (Table 10-1).
 2: Higher capacitance increases the stability of oscillator but also increases the start-up time.
 3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 4: Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification.

10.2.3 RC OSCILLATOR

For timing insensitive applications the “RC” device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 10-4 shows how the R/C combination is connected to the PIC16CXXX family.

FIGURE 10-4: RC OSCILLATOR MODE



10.3 Reset

The PIC16CXXX family differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ reset during normal operation
- $\overline{\text{MCLR}}$ reset during SLEEP
- WDT Reset (normal operation)
- Brown-out Reset (BOR)

Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a “reset state” on Power-on Reset (POR), on the $\overline{\text{MCLR}}$ and WDT Reset, on $\overline{\text{MCLR}}$ reset during SLEEP, and Brown-out Reset (BOR). They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations as indicated in Table 10-4. These bits are used in software to determine the nature of the reset. See Table 10-6 for a full description of reset states of all registers.

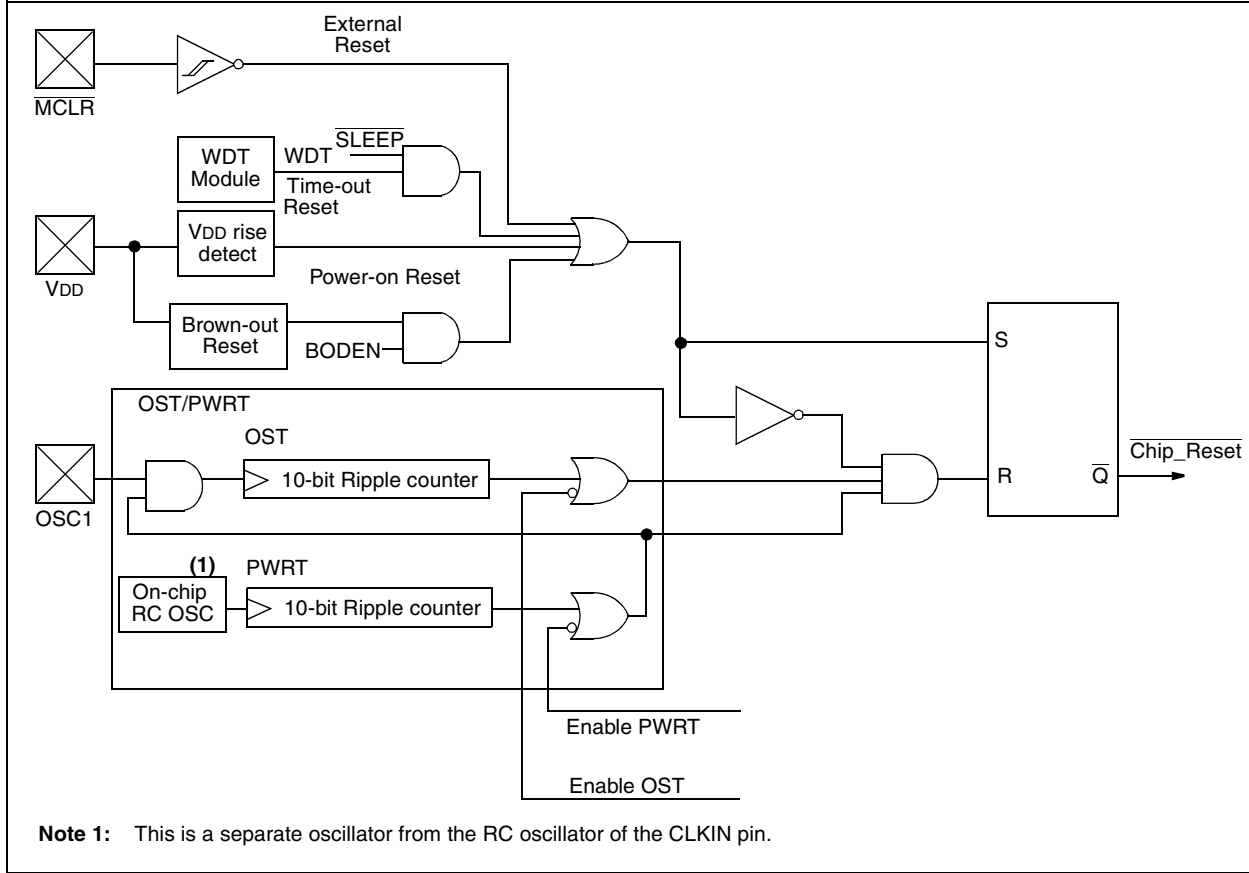
A simplified block diagram of the on-chip reset circuit is shown in Figure 10-5.

The PIC16C72/CR72 have a $\overline{\text{MCLR}}$ noise filter in the $\overline{\text{MCLR}}$ reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

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FIGURE 10-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

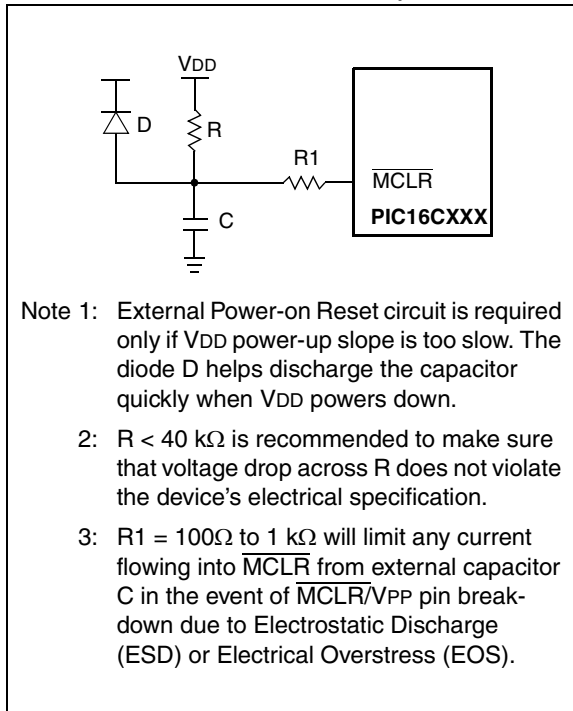


10.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details. For a slow rise time, see Figure 10-6.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the startup conditions.

FIGURE 10-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



10.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

10.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

10.7 Brown-Out Reset (BOR)

A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below 4.0V (3.8V - 4.2V range) for greater than parameter #35, the brown-out situation will reset the chip. A reset may not occur if VDD falls below 4.0V for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer will now be invoked and will keep the chip in RESET an additional 72 ms. If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms time delay. The Power-up Timer should always be enabled when Brown-out Reset is enabled.

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10.8 Time-out Sequence

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 10-7, Figure 10-8, Figure 10-9 and Figure 10-10 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (Figure 10-9). This is useful for testing purposes or to synchronize more than one PIC16CXXX family device operating in parallel.

Table 10-5 shows the reset conditions for some special function registers, while Table 10-6 shows the reset conditions for all the registers.

TABLE 10-3 TIME-OUT IN VARIOUS SITUATIONS

| Oscillator Configuration | Power-up | | Brown-out | Wake-up from SLEEP |
|--------------------------|------------------------------|------------------------------|------------------|--------------------|
| | $\overline{\text{PWRT}} = 0$ | $\overline{\text{PWRT}} = 1$ | | |
| XT, HS, LP | 72 ms + 1024Tosc | 1024Tosc | 72 ms + 1024Tosc | 1024Tosc |
| RC | 72 ms | — | 72 ms | — |

TABLE 10-4 STATUS BITS AND THEIR SIGNIFICANCE

| POR | BOR | $\overline{\text{TO}}$ | $\overline{\text{PD}}$ | |
|-----|-----|------------------------|------------------------|---|
| 0 | x | 1 | 1 | Power-on Reset |
| 0 | x | 0 | x | Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$ |
| 0 | x | x | 0 | Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$ |
| 1 | 0 | x | x | Brown-out Reset |
| 1 | 1 | 0 | 1 | WDT Reset |
| 1 | 1 | 0 | 0 | WDT Wake-up |
| 1 | 1 | u | u | $\overline{\text{MCLR}}$ Reset during normal operation |
| 1 | 1 | 1 | 0 | $\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP |

TABLE 10-5 RESET CONDITION FOR SPECIAL REGISTERS

| Condition | Program Counter | STATUS Register | PCON Register |
|--|-----------------------|-----------------|---------------|
| Power-on Reset | 000h | 0001 1xxx | ---- --0x |
| $\overline{\text{MCLR}}$ Reset during normal operation | 000h | 000u uuuu | ---- --uu |
| $\overline{\text{MCLR}}$ Reset during SLEEP | 000h | 0001 0uuu | ---- --uu |
| WDT Reset | 000h | 0000 1uuu | ---- --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | ---- --uu |
| Brown-out Reset | 000h | 0001 1uuu | ---- --u0 |
| Interrupt wake-up from SLEEP | PC + 1 ⁽¹⁾ | uuu1 0uuu | ---- --uu |

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

10.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON has up to two bits, depending upon the device.

Bit0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a BOR occurred. The $\overline{\text{BOR}}$ bit is a "Don't Care" bit and is not necessarily predictable if the Brown-out Reset circuitry is disabled (by clearing bit BODEN in the Configuration Word).

Bit1 is $\overline{\text{POR}}$ (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 10-6 INITIALIZATION CONDITIONS FOR ALL REGISTERS

| Register | Power-on Reset, Brown-out Reset | MCLR Resets WDT Reset | Wake-up via WDT or Inter- rupt |
|----------|------------------------------------|--------------------------|-----------------------------------|
| W | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | N/A | N/A | N/A |
| TMR0 | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 0000h | 0000h | PC + 1 ⁽²⁾ |
| STATUS | 0001 1xxx | 000q quuu ⁽³⁾ | uuuq quuu ⁽³⁾ |
| FSR | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTA | --0x 0000 | --0u 0000 | --uu uuuu |
| PORTB | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PORTC | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCLATH | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0000 000x | 0000 000u | uuuu uuuu ⁽¹⁾ |
| PIR1 | -0-- 0000 | -0-- 0000 | -u-- uuuu ⁽¹⁾ |
| TMR1L | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | --00 0000 | --uu uuuu | --uu uuuu |
| TMR2 | 0000 0000 | 0000 0000 | uuuu uuuu |
| T2CON | -000 0000 | -000 0000 | -uuu uuuu |
| SSPBUF | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| SSPCON | 0000 0000 | 0000 0000 | uuuu uuuu |
| CCPR1L | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCPR1H | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| CCP1CON | --00 0000 | --00 0000 | --uu uuuu |
| ADRES | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON0 | 0000 00-0 | 0000 00-0 | uuuu uu-u |
| OPTION | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISA | --11 1111 | --11 1111 | --uu uuuu |
| TRISB | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISC | 1111 1111 | 1111 1111 | uuuu uuuu |
| PIE1 | -0-- 0000 | -0-- 0000 | -u-- uuuu |
| PCON | ---- --0u | ---- --uu | ---- --uu |
| PR2 | 1111 1111 | 1111 1111 | 1111 1111 |
| SSPADD | 0000 0000 | 0000 0000 | uuuu uuuu |
| SSPSTAT | --00 0000 | --00 0000 | --uu uuuu |
| ADCON1 | ---- -000 | ---- -000 | ---- -uuu |

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 10-5 for reset value for specific condition.

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FIGURE 10-7: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})

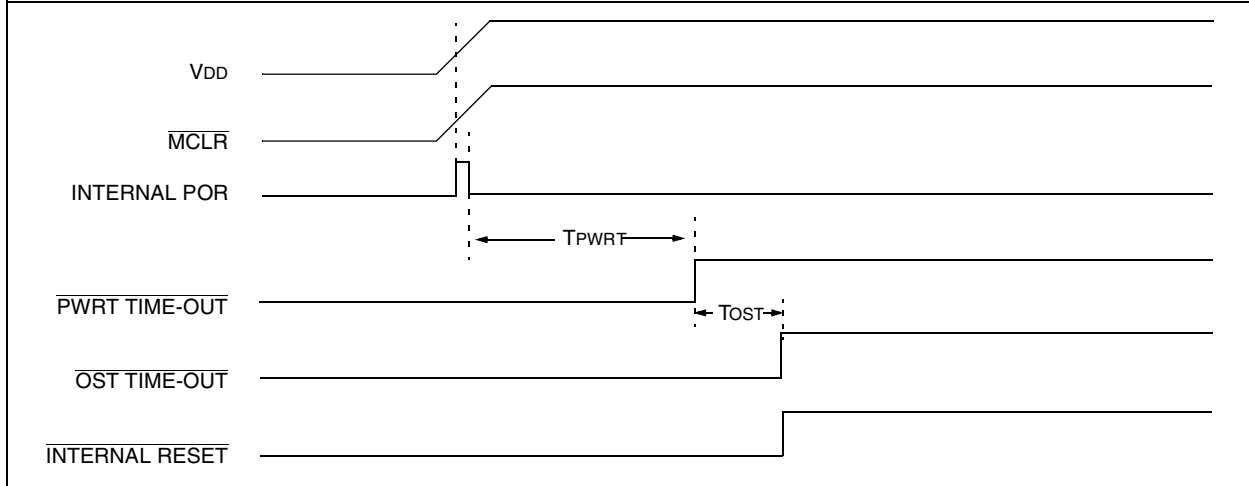


FIGURE 10-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

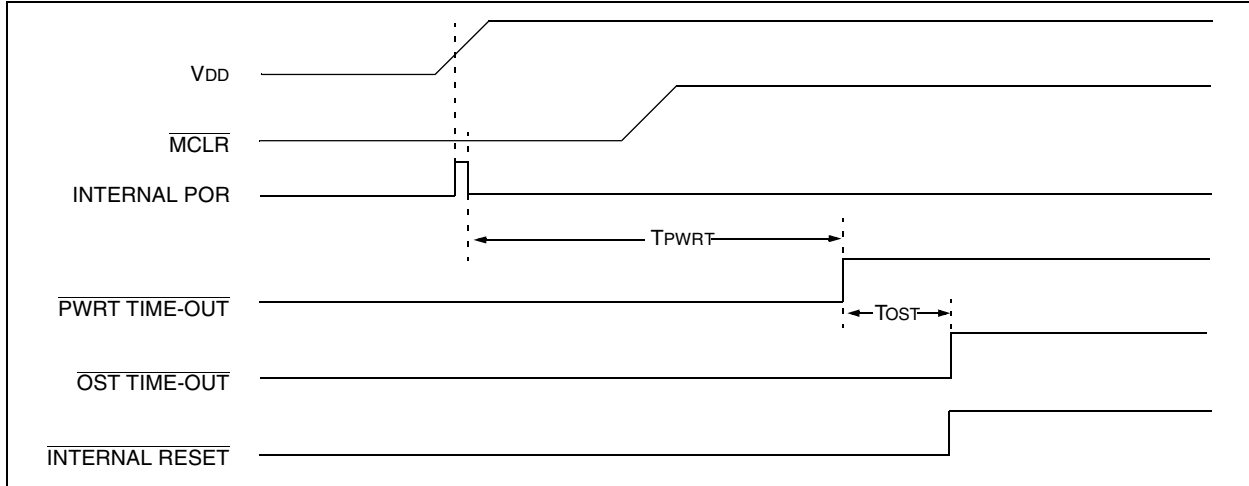


FIGURE 10-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

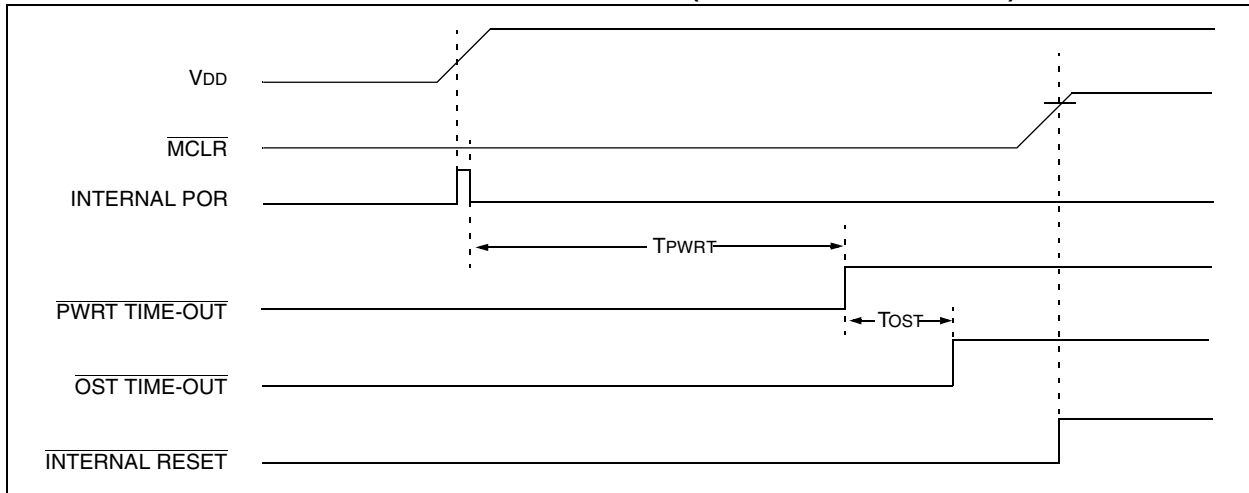
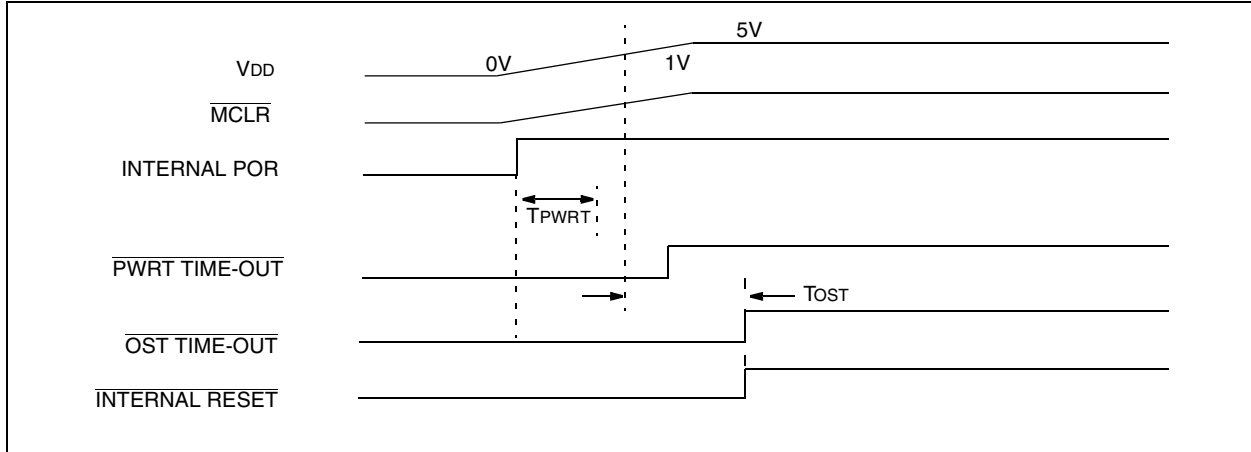


FIGURE 10-10: SLOW RISE TIME ($\overline{\text{MCLR}}$ TIED TO V_{DD})



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10.10 Interrupts

The PIC16C72/CR72 has 8 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit

10.10.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 10.13 for details on SLEEP mode.

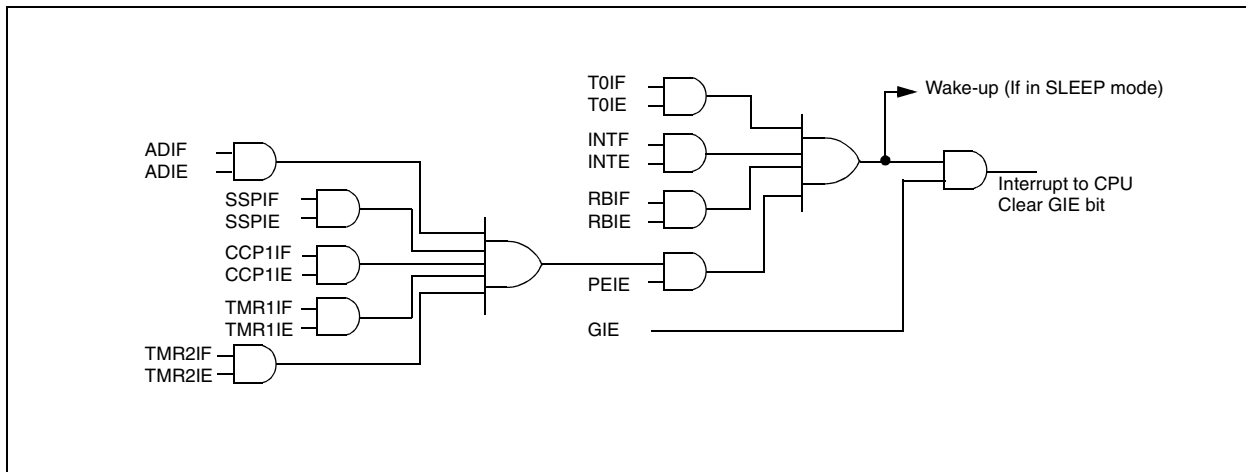
10.10.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 4.0)

10.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 3.2)

FIGURE 10-11: INTERRUPT LOGIC



10.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, i.e., W register and STATUS register. This will have to be implemented in software.

Example 10-1 stores and restores the W and STATUS registers. The register, W_TEMP, must be defined in each bank and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Executes the ISR code.
- d) Restores the STATUS register (and bank select bit).
- e) Restores the W register.

EXAMPLE 10-1: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM

```
MOVWF    W_TEMP                ;Copy W to W_TEMP register, could be bank one or zero
SWAPF    STATUS,W              ;Swap status to be saved into W
CLRF     STATUS                ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF    STATUS_TEMP           ;Save status to bank zero STATUS_TEMP register
:
: Interrupt Service Routine (ISR) - user defined
:
SWAPF    STATUS_TEMP,W         ;Swap STATUS_TEMP register into W
                                ;(sets bank to original state)
MOVWF    STATUS                ;Move W into STATUS register
SWAPF    W_TEMP,F             ;Swap W_TEMP
SWAPF    W_TEMP,W             ;Swap W_TEMP into W
```

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10.12 Watchdog Timer (WDT)

The Watchdog Timer is as a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The \overline{TO} bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing configuration bit WDTE (Section 10.1).

WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT prescaler (actually a postscaler, but shared with the Timer0 prescaler) may be assigned using the OPTION_REG register.

Note: The CLRWDT and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

Note: When a CLRWDT instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 10-12: WATCHDOG TIMER BLOCK DIAGRAM

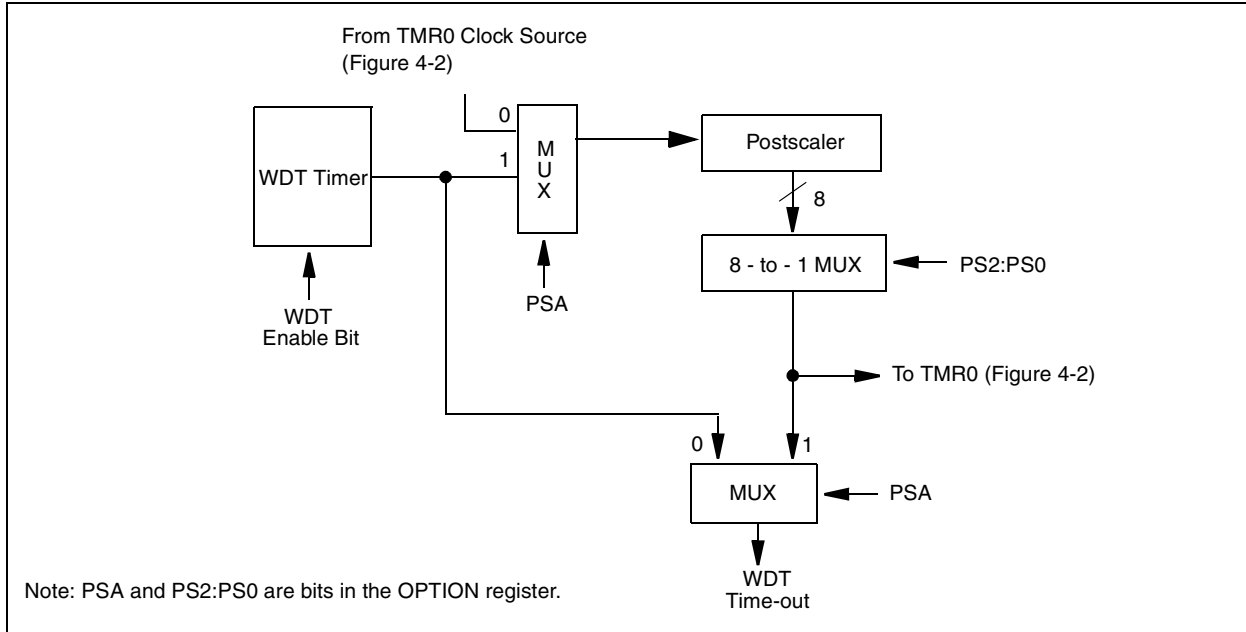


FIGURE 10-13: SUMMARY OF WATCHDOG TIMER REGISTERS

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|--------------|-------------------|----------------------|-------|-------|----------------------|-------|-------|-------|
| 2007h | Config. bits | (1) | BODEN ⁽¹⁾ | CP1 | CP0 | PWRTE ⁽¹⁾ | WDTE | FOSC1 | FOSC0 |
| 81h,181h | OPTION | \overline{RBPU} | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 10-1 for operation of these bits.

10.13 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (STATUS<3>) is cleared, the \overline{TO} (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD, or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The \overline{MCLR} pin must be at a logic high level (VIHMC).

10.13.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. External reset input on \overline{MCLR} pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External \overline{MCLR} Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The \overline{TO} and \overline{PD} bits in the STATUS register can be used to determine the cause of device reset. The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
2. SSP (Start/Stop) bit detect interrupt.
3. SSP transmit or receive in slave mode (SPI/I²C).
4. CCP capture mode interrupt.
5. A/D conversion (when A/D clock source is RC).
6. Special event trigger (Timer1 in asynchronous mode using an external clock).

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Other peripherals cannot generate interrupts since during SLEEP, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

10.13.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a

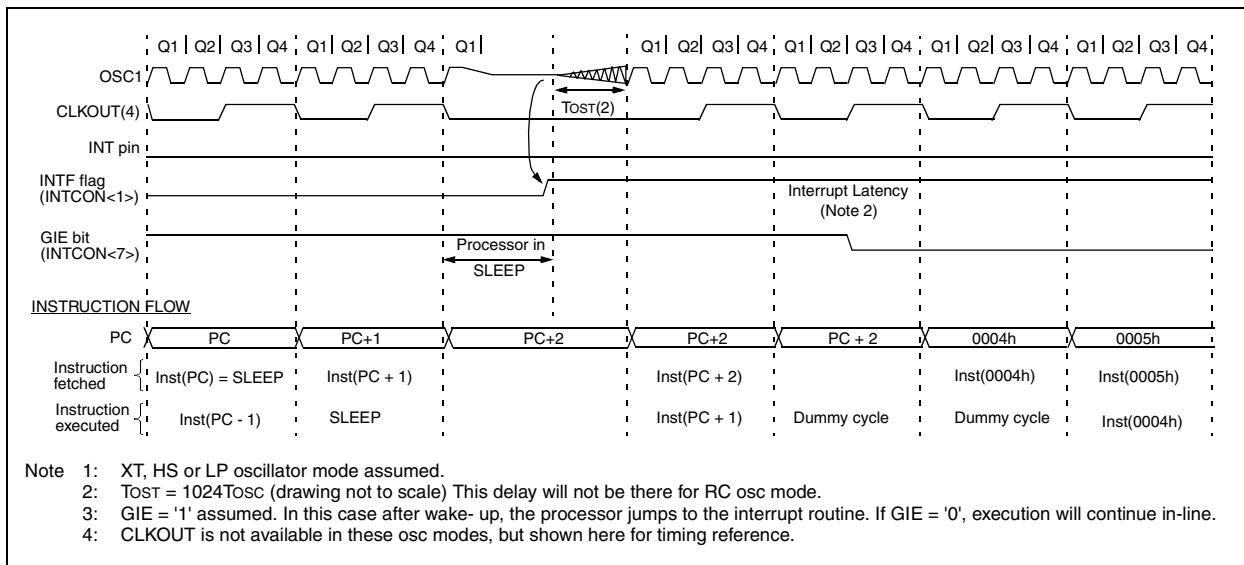
SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the \overline{TO} bit will not be set and \overline{PD} bits will not be cleared.

- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the \overline{TO} bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

FIGURE 10-14: WAKE-UP FROM SLEEP THROUGH INTERRUPT



10.14 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

10.15 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

10.16 In-Circuit Serial Programming™

PIC16CXXX family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP™) Guide, DS30277.

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11.0 INSTRUCTION SET SUMMARY

Each PIC16CXXX family instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16CXXX family instruction set summary in Table 11-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 11-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 11-1 OPCODE FIELD DESCRIPTIONS

| Field | Description |
|-------|---|
| f | Register file address (0x00 to 0x7F) |
| w | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1 |
| PC | Program Counter |
| TO | Time-out bit |
| PD | Power-down bit |

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 11-2 lists the instructions recognized by the MPASM assembler.

Figure 11-1 shows the general formats that the instructions can have.

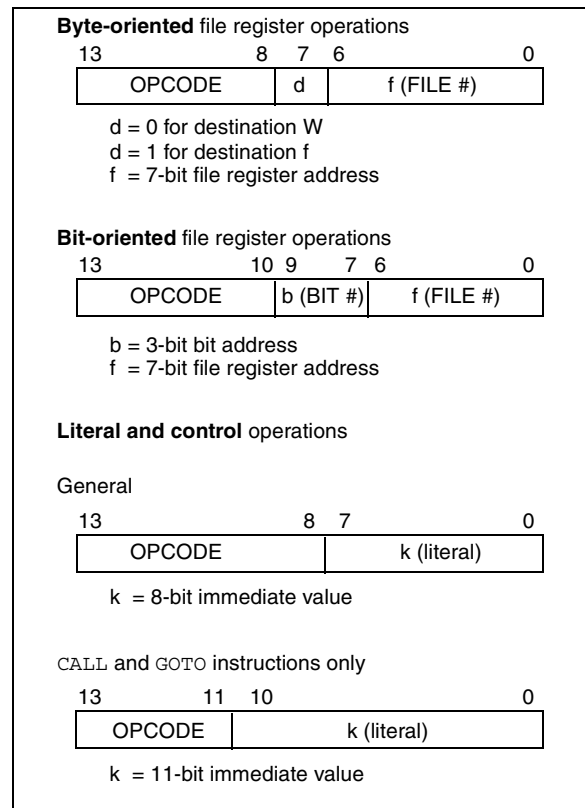
Note: To maintain upward compatibility with future PIC16CXXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 11-1: GENERAL FORMAT FOR INSTRUCTIONS



A description of each instruction is available in the PIC[®] Mid-Range MCU Family Reference Manual, DS33023.

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TABLE 11-2 PIC16CXXX INSTRUCTION SET

| Mnemonic, Operands | Description | Cycles | 14-Bit Opcode | | | Status Affected | Notes | |
|---|--|--------|---------------|------|------|--------------------|--------------------------------|-------|
| | | | MSb | LSb | | | | |
| BYTE-ORIENTED FILE REGISTER OPERATIONS | | | | | | | | |
| ADDWF | f, d Add W and f | 1 | 00 | 0111 | dfff | ffff | C,DC,Z | 1,2 |
| ANDWF | f, d AND W with f | 1 | 00 | 0101 | dfff | ffff | Z | 1,2 |
| CLRF | f Clear f | 1 | 00 | 0001 | 1fff | ffff | Z | 2 |
| CLRWF | - Clear W | 1 | 00 | 0001 | 0xxx | xxxx | Z | |
| COMF | f, d Complement f | 1 | 00 | 1001 | dfff | ffff | Z | 1,2 |
| DECWF | f, d Decrement f | 1 | 00 | 0011 | dfff | ffff | Z | 1,2 |
| DECFSZ | f, d Decrement f, Skip if 0 | 1(2) | 00 | 1011 | dfff | ffff | | 1,2,3 |
| INCF | f, d Increment f | 1 | 00 | 1010 | dfff | ffff | Z | 1,2 |
| INCFSZ | f, d Increment f, Skip if 0 | 1(2) | 00 | 1111 | dfff | ffff | | 1,2,3 |
| IORWF | f, d Inclusive OR W with f | 1 | 00 | 0100 | dfff | ffff | Z | 1,2 |
| MOVWF | f, d Move f | 1 | 00 | 1000 | dfff | ffff | Z | 1,2 |
| MOVWF | f Move W to f | 1 | 00 | 0000 | 1fff | ffff | | |
| NOP | - No Operation | 1 | 00 | 0000 | 0xx0 | 0000 | | |
| RLF | f, d Rotate Left f through Carry | 1 | 00 | 1101 | dfff | ffff | C | 1,2 |
| RRF | f, d Rotate Right f through Carry | 1 | 00 | 1100 | dfff | ffff | C | 1,2 |
| SUBWF | f, d Subtract W from f | 1 | 00 | 0010 | dfff | ffff | C,DC,Z | 1,2 |
| SWAPF | f, d Swap nibbles in f | 1 | 00 | 1110 | dfff | ffff | | 1,2 |
| XORWF | f, d Exclusive OR W with f | 1 | 00 | 0110 | dfff | ffff | Z | 1,2 |
| BIT-ORIENTED FILE REGISTER OPERATIONS | | | | | | | | |
| BCF | f, b Bit Clear f | 1 | 01 | 00bb | bfff | ffff | | 1,2 |
| BSF | f, b Bit Set f | 1 | 01 | 01bb | bfff | ffff | | 1,2 |
| BTFSC | f, b Bit Test f, Skip if Clear | 1 (2) | 01 | 10bb | bfff | ffff | | 3 |
| BTFSS | f, b Bit Test f, Skip if Set | 1 (2) | 01 | 11bb | bfff | ffff | | 3 |
| LITERAL AND CONTROL OPERATIONS | | | | | | | | |
| ADDLW | k Add literal and W | 1 | 11 | 111x | kkkk | kkkk | C,DC,Z | |
| ANDLW | k AND literal with W | 1 | 11 | 1001 | kkkk | kkkk | Z | |
| CALL | k Call subroutine | 2 | 10 | 0kkk | kkkk | kkkk | | |
| CLRWDT | - Clear Watchdog Timer | 1 | 00 | 0000 | 0110 | 0100 | $\overline{TO}, \overline{PD}$ | |
| GOTO | k Go to address | 2 | 10 | 1kkk | kkkk | kkkk | | |
| IORLW | k Inclusive OR literal with W | 1 | 11 | 1000 | kkkk | kkkk | Z | |
| MOVLW | k Move literal to W | 1 | 11 | 00xx | kkkk | kkkk | | |
| RETFIE | - Return from interrupt | 2 | 00 | 0000 | 0000 | 1001 | | |
| RETLW | k Return with literal in W | 2 | 11 | 01xx | kkkk | kkkk | | |
| RETURN | - Return from Subroutine | 2 | 00 | 0000 | 0000 | 1000 | | |
| SLEEP | - Go into standby mode | 1 | 00 | 0000 | 0110 | 0011 | $\overline{TO}, \overline{PD}$ | |
| SUBLW | k Subtract W from literal | 1 | 11 | 110x | kkkk | kkkk | C,DC,Z | |
| XORLW | k Exclusive OR literal with W | 1 | 11 | 1010 | kkkk | kkkk | Z | |

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVWF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

12.0 DEVELOPMENT SUPPORT

12.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER®/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzyTECH*®-MP)

A description of each development tool is available in the Midrange Reference Manual, DS33023.

12.2 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

PIC16C72 Series

NOTES:

13.0 ELECTRICAL CHARACTERISTICS - PIC16C72 SERIES

Absolute Maximum Ratings †

| Parameter | PIC16C72 | PIC16CR72 |
|--|-----------------------------------|-----------------------------------|
| Ambient temperature under bias | -55 to +125°C | -55 to +125°C |
| Storage temperature | -65°C to +150°C | -65°C to +150°C |
| Voltage on any pin with respect to V _{SS} (except V _{DD} , $\overline{\text{MCLR}}$, and RA4) | -0.3V to (V _{DD} + 0.3V) | -0.3V to (V _{DD} + 0.3V) |
| Voltage on V _{DD} with respect to V _{SS} | -0.3 to +7.5V | TBD |
| Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} (Note 1) | -0.3 to +14V | TBD |
| Voltage on RA4 with respect to V _{SS} | -0.3 to +14V | TBD |
| Total power dissipation (Note 2) | 1.0W | 1.0W |
| Maximum current out of V _{SS} pin | 300 mA | 300 mA |
| Maximum current into V _{DD} pin | 250 mA | 250 mA |
| Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}) | ± 20 mA | ± 20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}) | ± 20 mA | ± 20 mA |
| Maximum output current sunk by any I/O pin | 25 mA | 25 mA |
| Maximum output current sourced by any I/O pin | 25 mA | 25 mA |
| Maximum current sunk by PORTA and PORTB (combined) | 200 mA | 200 mA |
| Maximum current sourced by PORTA and PORTB (combined) | 200 mA | 200 mA |
| Maximum current sunk by PORTC | 200 mA | 200 mA |
| Maximum current sourced by PORTC | 200 mA | 200 mA |

1. Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to V_{SS}.
2. Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16C72 Series

TABLE 13-1 CROSS REFERENCE OF DEVICE SPECS (PIC16C72) FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

| OSC | PIC16C72-04 | PIC16C72-10 | PIC16C72-20 | PIC16LC72-04 | JW Devices |
|-----|--|--|--|--|--|
| RC | VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5.0 μ A max. at 3V Freq: 4 MHz max. | VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. |
| XT | VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 2.5V to 6.0V IDD: 3.8 mA max. at 3.0V IPD: 5.0 μ A max. at 3V Freq: 4 MHz max. | VDD: 4.0V to 6.0V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 10 MHz max. | VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 20 MHz max. |
| LP | VDD: 4.0V to 6.0V IDD: 52.5 μ A typ. at 32 kHz, 4.0V IPD: 0.9 μ A typ. at 4.0V Freq: 200 kHz max. | Not recommended for use in LP mode | Not recommended for use in LP mode | VDD: 2.5V to 6.0V IDD: 48 μ A max. at 32 kHz, 3.0V IPD: 5.0 μ A max. at 3.0V Freq: 200 kHz max. | VDD: 2.5V to 6.0V IDD: 48 μ A max. at 32 kHz, 3.0V IPD: 5.0 μ A max. at 3.0V Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

TABLE 13-2 CROSS REFERENCE OF DEVICE SPECS (PIC16CR72) FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

| OSC | PIC16CR72-04 | PIC16CR72-10 | PIC16CR72-20 | PIC16LCR72-04 | JW Devices |
|-----|--|--|--|--|--|
| RC | VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 2.5V to 5.5V IDD: 3.8 mA max. at 3.0V IPD: 5.0 μ A max. at 3V Freq: 4 MHz max. | VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. |
| XT | VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max. | VDD: 2.5V to 5.5V IDD: 3.8 mA max. at 3.0V IPD: 5.0 μ A max. at 3V Freq: 4 MHz max. | VDD: 4.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 16 μ A max. at 4V Freq: 4 MHz max. |
| HS | VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 4 MHz max. | VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 10 MHz max. | VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 20 MHz max. | Not recommended for use in HS mode | VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 20 MHz max. |
| LP | VDD: 4.0V to 5.5V IDD: 52.5 μ A typ. at 32 kHz, 4.0V IPD: 0.9 μ A typ. at 4.0V Freq: 200 kHz max. | Not recommended for use in LP mode | Not recommended for use in LP mode | VDD: 2.5V to 5.5V IDD: 48 μ A max. at 32 kHz, 3.0V IPD: 5.0 μ A max. at 3.0V Freq: 200 kHz max. | VDD: 2.5V to 5.5V IDD: 48 μ A max. at 32 kHz, 3.0V IPD: 5.0 μ A max. at 3.0V Freq: 200 kHz max. |

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

13.1 DC Characteristics: PIC16C72/CR72-04 (Commercial, Industrial, Extended) PIC16C72/CR72-10 (Commercial, Industrial, Extended) PIC16C72/CR72-20 (Commercial, Industrial, Extended)

| Standard Operating Conditions (unless otherwise stated) | | | | | | | | | | |
|---|--|-------|----------------------------------|-------|------------|-----------|------|------------|-------|--|
| DC CHARACTERISTICS | | | | | | | | | | |
| Operating temperature -40°C ≤ TA ≤ +125°C for extended, -40°C ≤ TA ≤ +85°C for industrial and 0°C ≤ TA ≤ +70°C for commercial | | | | | | | | | | |
| Param No. | Characteristic | Sym | PIC16C72 | | | PIC16CR72 | | | Units | Conditions |
| | | | Min | Typ† | Max | Min | Typ† | Max | | |
| D001 | Supply Voltage | VDD | 4.0 | - | 6.0 | 4.0 | - | 5.5 | V | XT, RC and LP osc HS osc |
| D001A | | | 4.5 | - | 5.5 | 4.5 | - | 5.5 | V | |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset Signal | VPOR | - | VSS | - | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset Signal | SVDD | 0.05 | - | - | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D005 | Brown-out Reset Voltage | Bvdd | 3.7 | 4.0 | 4.3 | 3.7 | 4.0 | 4.3 | V | BODEN bit in configuration word enabled Extended Only |
| | | | 3.7 | 4.0 | 4.4 | 3.7 | 4.0 | 4.4 | V | |
| D010 | Supply Current (Note 2,5) | IDD | - | 2.7 | 5.0 | - | 2.7 | 5.0 | mA | XT, RC osc FOSC = 4 MHz, VDD = 5.5V (Note 4) |
| D013 | | | - | 10 | 20 | - | 10 | 20 | mA | HS osc FOSC = 20 MHz, VDD = 5.5V |
| D015 | | | Brown-out Reset Current (Note 6) | ΔIbor | - | 350 | 425 | - | 350 | 425 |
| D020 | Power-down Current (Note 3,5) | IPD | - | 10.5 | 42 | - | 10.5 | 42 | μA | VDD = 4.0V, WDT enabled, -40°C to +85°C |
| D021 | | | - | 1.5 | 16 | - | 1.5 | 16 | μA | VDD = 4.0V, WDT disabled, -0°C to +70°C |
| D021A | | | - | 1.5 | 19 | - | 1.5 | 19 | μA | VDD = 4.0V, WDT disabled, -40°C to +85°C |
| D021B | | | - | 2.5 | 19 | - | 2.5 | 19 | μA | VDD = 4.0V, WDT disabled, -40°C to +125°C |
| D023 | Brown-out Reset Current (Note 6) | ΔIbor | - | 350 | 425 | - | 350 | 425 | μA | BOR enabled VDD = 5.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

Note 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

Note 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

Note 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

Note 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C72 Series

13.2 DC Characteristics: PIC16LC72/LCR72-04 (Commercial, Industrial)

| Standard Operating Conditions (unless otherwise stated) | | | | | | | | | | |
|---|--|------------------|----------|------|-----|-----------|------|-----|---------------|--|
| DC CHARACTERISTICS | | | | | | | | | | |
| Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial | | | | | | | | | | |
| Param No. | Characteristic | Sym | PIC16C72 | | | PIC16CR72 | | | Units | Conditions |
| | | | Min | Typ† | Max | Min | Typ† | Max | | |
| D001 | Supply Voltage | VDD | 2.5 | - | 6.0 | 2.5 | - | 5.5 | V | LP, XT, RC (DC - 4 MHz) |
| D002* | RAM Data Retention Voltage (Note 1) | VDR | - | 1.5 | - | - | 1.5 | - | V | |
| D003 | VDD start voltage to ensure internal Power-on Reset signal | VPOR | - | VSS | - | - | VSS | - | V | See section on Power-on Reset for details |
| D004* | VDD rise rate to ensure internal Power-on Reset signal | SVDD | 0.05 | - | - | 0.05 | - | - | V/ms | See section on Power-on Reset for details |
| D005 | Brown-out Reset Voltage | Bvdd | 3.7 | 4.0 | 4.3 | 3.7 | 4.0 | 4.3 | V | BODEN bit in configuration word enabled |
| D010 | Supply Current (Note 2,5) | IDD | - | 2.0 | 3.8 | - | 2.0 | 3.8 | mA | XT, RC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4) |
| D010A | | | - | 22.5 | 48 | - | 22.5 | 48 | μA | LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| D015* | Brown-out Reset Current (Note 6) | ΔI_{bor} | - | 350 | 425 | - | 350 | 425 | μA | BOR enabled VDD = 5.0V |
| D020 | Power-down Current (Note 3,5) | IPD | - | 7.5 | 30 | - | 7.5 | 30 | μA | VDD = 3.0V, WDT enabled, -40°C to $+85^{\circ}\text{C}$ |
| D021 | | | - | 0.9 | 5 | - | 0.9 | 5 | μA | VDD = 3.0V, WDT disabled, 0°C to $+70^{\circ}\text{C}$ |
| D021A | | | - | 0.9 | 5 | - | 0.9 | 5 | μA | VDD = 3.0V, WDT disabled, -40°C to $+85^{\circ}\text{C}$ |
| D023* | Brown-out Reset Current (Note 6) | ΔI_{bor} | - | 350 | 425 | - | 350 | 425 | μA | BOR enabled VDD = 5.0V |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

Note 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

Note 3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

Note 4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

Note 5: Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

Note 6: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16C72 Series

13.3 DC Characteristics: PIC16C72/CR72-04 (Commercial, Industrial, Extended) PIC16C72/CR72-10 (Commercial, Industrial, Extended) PIC16C72/CR72-20 (Commercial, Industrial, Extended) PIC16LC72/LCR72-04 (Commercial, Industrial)

| Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage V_{DD} range as described in DC spec Section 13.1 and Section 13.2. | | | | | | | |
|---|---------------------------------------|------------|---------------------|------|--------------|---------------|--|
| Param No. | Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
| DC CHARACTERISTICS | | | | | | | |
| Input Low Voltage | | | | | | | |
| D030 | I/O ports | V_{IL} | V_{SS} | - | $0.15V_{DD}$ | V | For entire V_{DD} range |
| D030A | with TTL buffer | | V_{SS} | - | 0.8V | V | $4.5 \leq V_{DD} \leq 5.5V$ |
| D031 | with Schmitt Trigger buffer | | V_{SS} | - | $0.2V_{DD}$ | V | |
| D032 | \overline{MCLR} , OSC1 (in RC mode) | | V_{SS} | - | $0.2V_{DD}$ | V | |
| D033 | OSC1 (in XT, HS and LP) | | V_{SS} | - | $0.3V_{DD}$ | V | Note1 |
| Input High Voltage | | | | | | | |
| D040 | I/O ports | V_{IH} | 2.0 | - | V_{DD} | V | $4.5 \leq V_{DD} \leq 5.5V$ |
| D040A | with TTL buffer | | $0.25V_{DD} + 0.8V$ | - | V_{DD} | V | For entire V_{DD} range |
| D041 | with Schmitt Trigger buffer | | $0.8V_{DD}$ | - | V_{DD} | V | For entire V_{DD} range |
| D042 | \overline{MCLR} | | $0.8V_{DD}$ | - | V_{DD} | V | |
| D042A | OSC1 (XT, HS and LP) | | $0.7V_{DD}$ | - | V_{DD} | V | Note1 |
| D043 | OSC1 (in RC mode) | | $0.9V_{DD}$ | - | V_{DD} | V | |
| D070 | PORTB weak pull-up current | I_{PURB} | 50 | 250 | †400 | μA | $V_{DD} = 5V, V_{PIN} = V_{SS}$ |
| Input Leakage Current (Notes 2, 3) | | | | | | | |
| D060 | I/O ports | I_{IL} | - | - | ± 1 | μA | $V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance |
| D061 | \overline{MCLR} , RA4/T0CKI | | - | - | ± 5 | μA | $V_{SS} \leq V_{PIN} \leq V_{DD}$ |
| D063 | OSC1 | | - | - | ± 5 | μA | $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration |
| Output Low Voltage | | | | | | | |
| D080 | I/O ports | V_{OL} | - | - | 0.6 | V | $I_{OL} = 8.5 \text{ mA}, V_{DD} = 4.5V, -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$ |
| D080A | | | - | - | 0.6 | V | $I_{OL} = 7.0 \text{ mA}, V_{DD} = 4.5V, -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}$ |
| D083 | OSC2/CLKOUT (RC osc config) | | - | - | 0.6 | V | $I_{OL} = 1.6 \text{ mA}, V_{DD} = 4.5V, -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$ |
| D083A | | | - | - | 0.6 | V | $I_{OL} = 1.2 \text{ mA}, V_{DD} = 4.5V, -40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}$ |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

Note 2: The leakage current on the \overline{MCLR}/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 3: Negative current is defined as current sourced by the pin.

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| Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial Operating voltage V_{DD} range as described in DC spec Section 13.1 and Section 13.2. | | | | | | | |
|---|--|-------------------|----------------|------|-----|-------|---|
| Param No. | Characteristic | Sym | Min | Typ† | Max | Units | Conditions |
| DC CHARACTERISTICS | | | | | | | |
| D090 | Output High Voltage I/O ports (Note 3) | V _{OH} | $V_{DD} - 0.7$ | - | - | V | I _{OH} = -3.0 mA, V _{DD} = 4.5V, -40°C to +85°C |
| D090A | | | $V_{DD} - 0.7$ | - | - | V | I _{OH} = -2.5 mA, V _{DD} = 4.5V, -40°C to +125°C |
| D092 | OSC2/CLKOUT (RC osc config) | | $V_{DD} - 0.7$ | - | - | V | I _{OH} = -1.3 mA, V _{DD} = 4.5V, -40°C to +85°C |
| D092A | | | $V_{DD} - 0.7$ | - | - | V | I _{OH} = -1.0 mA, V _{DD} = 4.5V, -40°C to +125°C |
| D150* | Open-Drain High Voltage | V _{od} | - | - | 14 | V | RA4 pin, PIC16C72/LC72 |
| | | | - | - | TBD | V | RA4 pin, PIC16CR72/LCR72 |
| Capacitive Loading Specs on Output Pins | | | | | | | |
| D100 | OSC2 pin | C _{OSC2} | - | - | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | All I/O pins and OSC2 (in RC mode) | C _{IO} | - | - | 50 | pF | |
| D102 | SCL, SDA in I ² C mode | C _b | - | - | 400 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt trigger input. It is not recommended that the PIC16C7X be driven with external clock in RC mode.

Note 2: The leakage current on the $\overline{\text{MCLR}}/\text{VPP}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

Note 3: Negative current is defined as current sourced by the pin.

13.4 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

- | | | |
|-------------|-----------|--|
| 1. TppS2ppS | 3. TCC:ST | (I ² C specifications only) |
| 2. TppS | 4. Ts | (I ² C specifications only) |

| | | | |
|---|-----------|---|------|
| T | | T | |
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| | | | |
|----|-------------------|-----|------------------------------------|
| pp | | osc | OSC1 |
| cc | CCP1 | rd | \overline{RD} |
| ck | CLKOUT | rw | \overline{RD} or \overline{WR} |
| cs | \overline{CS} | sc | SCK |
| di | SDI | ss | \overline{SS} |
| do | SDO | t0 | T0CKI |
| dt | Data in | t1 | T1CKI |
| io | I/O port | wr | \overline{WR} |
| mc | \overline{MCLR} | | |

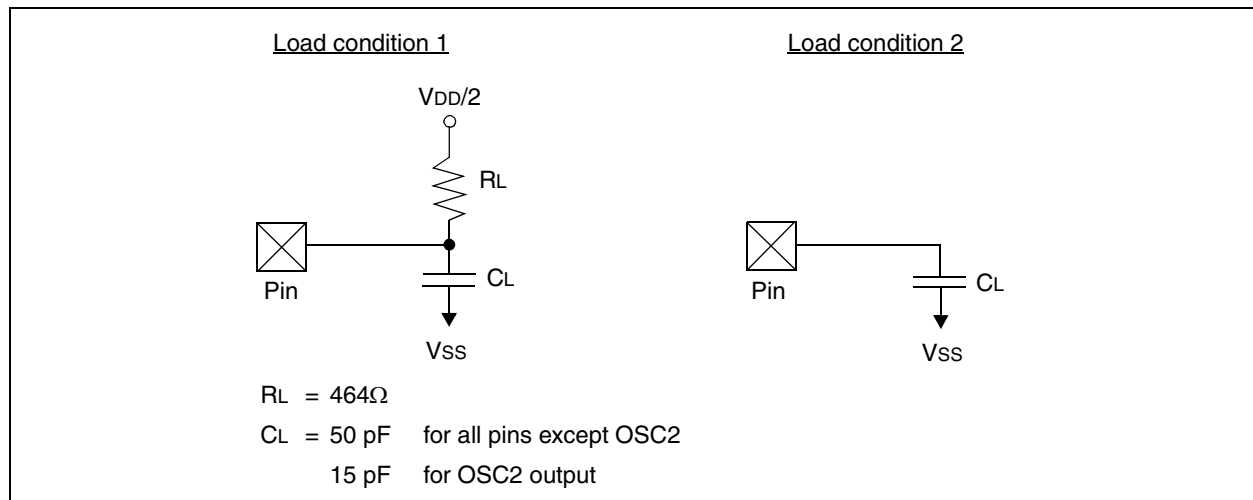
Uppercase letters and their meanings:

| | | | |
|-----------------------|------------------------|------|--------------|
| S | | P | Period |
| F | Fall | R | Rise |
| H | High | V | Valid |
| I | Invalid (Hi-impedance) | Z | Hi-impedance |
| L | Low | | |
| I ² C only | | | |
| AA | output access | High | High |
| BUF | Bus free | Low | Low |

TCC:ST (I²C specifications only)

| | | | |
|-----|-----------------|-----|----------------|
| CC | | SU | Setup |
| HD | Hold | | |
| ST | | STO | STOP condition |
| DAT | DATA input hold | | |
| STA | START condition | | |

FIGURE 13-1: LOAD CONDITIONS



PIC16C72 Series

13.5 Timing Diagrams and Specifications

FIGURE 13-2: EXTERNAL CLOCK TIMING

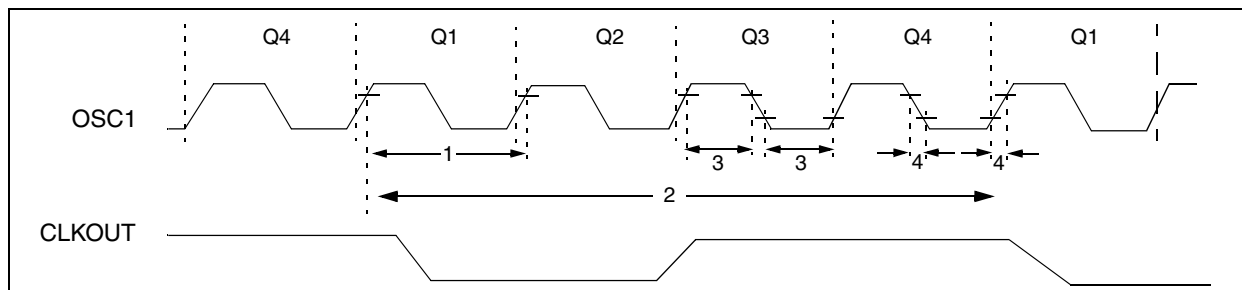


TABLE 13-3 EXTERNAL CLOCK TIMING REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|----------------------------|-------------------------------|--|------|--------------------------------|-----|-------------------|--------------------|
| | Fosc | External CLKIN Frequency (Note 1) | DC | — | 4 | MHz | XT and RC osc mode |
| | | | DC | — | 4 | MHz | HS osc mode (-04) |
| | | | DC | — | 10 | MHz | HS osc mode (-10) |
| | | | DC | — | 20 | MHz | HS osc mode (-20) |
| | | | DC | — | 200 | kHz | LP osc mode |
| | Oscillator Frequency (Note 1) | DC | — | 4 | MHz | RC osc mode | |
| | | 0.1 | — | 4 | MHz | XT osc mode | |
| | | 4 | — | 20 | MHz | HS osc mode | |
| | | 5 | — | 200 | kHz | LP osc mode | |
| | | 1 | Tosc | External CLKIN Period (Note 1) | 250 | — | — |
| 250 | — | | | | — | ns | HS osc mode (-04) |
| 100 | — | | | | — | ns | HS osc mode (-10) |
| 50 | — | | | | — | ns | HS osc mode (-20) |
| 5 | — | | | | — | μs | LP osc mode |
| Oscillator Period (Note 1) | 250 | | — | — | ns | RC osc mode | |
| | 250 | | — | 10,000 | ns | XT osc mode | |
| | 250 | | — | 250 | ns | HS osc mode (-04) | |
| | 100 | | — | 250 | ns | HS osc mode (-10) | |
| | 50 | | — | 250 | ns | HS osc mode (-20) | |
| 5 | — | — | μs | LP osc mode | | | |
| 2 | TCY | Instruction Cycle Time (Note 1) | 200 | — | DC | ns | TCY = 4/FOSC |
| 3 | TosL, TosH | External Clock in (OSC1) High or Low Time | 100 | — | — | ns | XT oscillator |
| | | | 2.5 | — | — | μs | LP oscillator |
| | | | 15 | — | — | ns | HS oscillator |
| 4 | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 25 | ns | XT oscillator |
| | | | — | — | 50 | ns | LP oscillator |
| | | | — | — | 15 | ns | HS oscillator |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 13-3: CLKOUT AND I/O TIMING

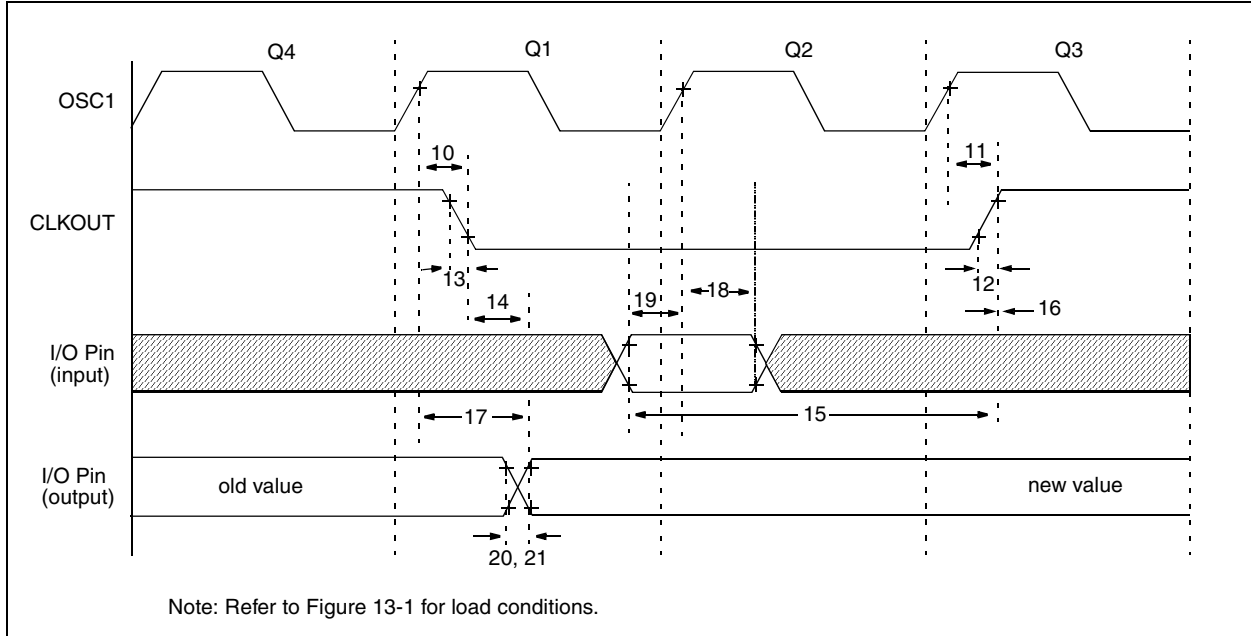


TABLE 13-4 CLKOUT AND I/O TIMING REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---------------|----------|---|-----------------|------|-------------|-------|------------|
| 10* | TosH2ckL | OSC1↑ to CLKOUT↓ | — | 75 | 200 | ns | Note 1 |
| 11* | TosH2ckH | OSC1↑ to CLKOUT↑ | — | 75 | 200 | ns | Note 1 |
| 12* | TckR | CLKOUT rise time | — | 35 | 100 | ns | Note 1 |
| 13* | TckF | CLKOUT fall time | — | 35 | 100 | ns | Note 1 |
| 14* | TckL2ioV | CLKOUT ↓ to Port out valid | — | — | 0.5TCY + 20 | ns | Note 1 |
| 15* | TioV2ckH | Port in valid before CLKOUT ↑ | Tosc + 200 | — | — | ns | Note 1 |
| 16* | TckH2ioI | Port in hold after CLKOUT ↑ | 0 | — | — | ns | Note 1 |
| 17* | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid | — | 50 | 150 | ns | |
| 18* | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | PIC16C72/CR72 | 100 | — | — | ns |
| | | | PIC16LC72/LCR72 | 200 | — | — | ns |
| 19* | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | 0 | — | — | ns | |
| 20* | TioR | Port output rise time | PIC16C72/CR72 | — | 10 | 40 | ns |
| | | | PIC16LC72/LCR72 | — | — | 80 | ns |
| 21* | TioF | Port output fall time | PIC16C72/CR72 | — | 10 | 40 | ns |
| | | | PIC16LC72/LCR72 | — | — | 80 | ns |
| 22††* | Tinp | INT pin high or low time | TCY | — | — | ns | |
| 23††* | Trbp | RB7:RB4 change INT high or low time | TCY | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

PIC16C72 Series

FIGURE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

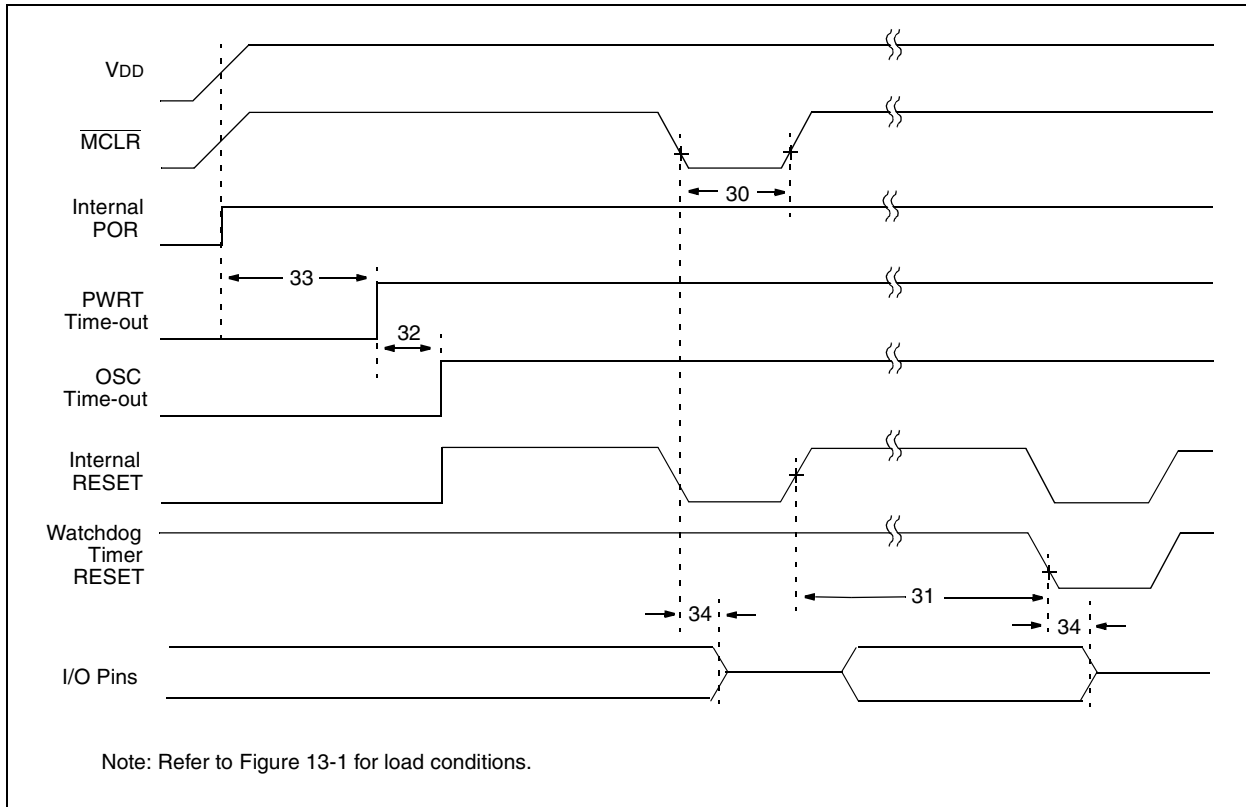


FIGURE 13-5: BROWN-OUT RESET TIMING

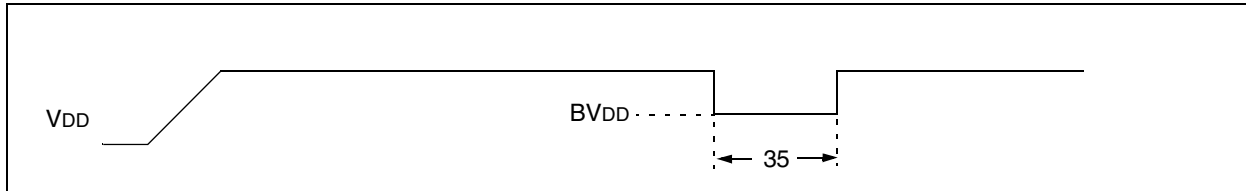


TABLE 13-5 RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT RESET REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---------------|-------|--|-----|----------|-----|-------|---------------------------|
| 30 | Tmcl | MCLR Pulse Width (low) | 2 | — | — | μs | VDD = 5V, -40°C to +125°C |
| 31* | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +125°C |
| 32 | Tost | Oscillation Start-up Timer Period | — | 1024Tosc | — | — | Tosc = OSC1 period |
| 33* | Tpwrt | Power-up Timer Period | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +125°C |
| 34 | Tioz | I/O Hi-impedance from MCLR Low or Watchdog Timer Reset | — | — | 2.1 | μs | |
| 35 | TBOR | Brown-out Reset pulse width | 100 | — | — | μs | VDD ≤ BVDD (D005) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-6: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

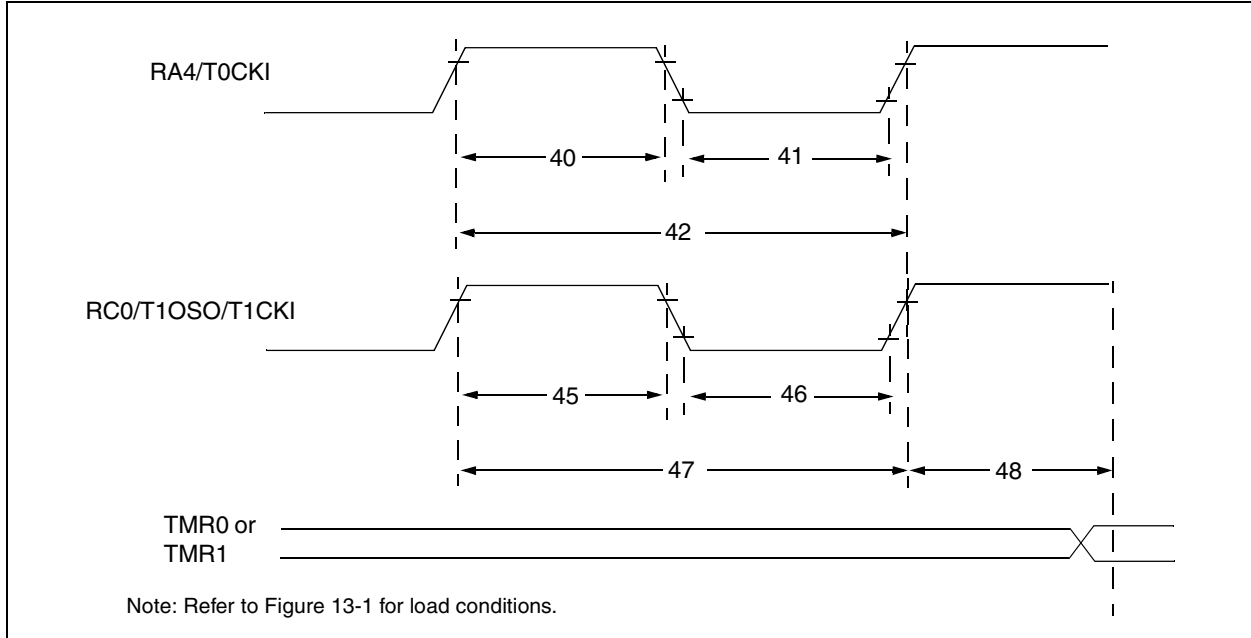


TABLE 13-6 TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions | |
|-----------|-----------|---|--------------------------------|--|--|------------|-------|-------------------------------------|---------------------------------|
| 40* | Tt0H | T0CKI High Pulse Width | No Prescaler | $0.5T_{CY} + 20$ | — | — | ns | Must also meet parameter 42 | |
| | | | With Prescaler | 10 | — | — | ns | | |
| 41* | Tt0L | T0CKI Low Pulse Width | No Prescaler | $0.5T_{CY} + 20$ | — | — | ns | Must also meet parameter 42 | |
| | | | With Prescaler | 10 | — | — | ns | | |
| 42* | Tt0P | T0CKI Period | No Prescaler | $T_{CY} + 40$ | — | — | ns | N = prescale value (2, 4, ..., 256) | |
| | | | With Prescaler | Greater of: 20 or $\frac{T_{CY} + 40}{N}$ | — | — | ns | | |
| 45* | Tt1H | T1CKI High Time | Synchronous, Prescaler = 1 | $0.5T_{CY} + 20$ | — | — | ns | Must also meet parameter 47 | |
| | | | Synchronous, Prescaler = 2,4,8 | PIC16C7X/CR72 | 15 | — | — | | ns |
| | | | | PIC16LC7X/LCR72 | 25 | — | — | | ns |
| | | | Asynchronous | PIC16C7X/CR72 | 30 | — | — | | ns |
| | | | PIC16LC7X/LCR72 | 50 | — | — | ns | | |
| 46* | Tt1L | T1CKI Low Time | Synchronous, Prescaler = 1 | $0.5T_{CY} + 20$ | — | — | ns | Must also meet parameter 47 | |
| | | | Synchronous, Prescaler = 2,4,8 | PIC16C7X/CR72 | 15 | — | — | | ns |
| | | | | PIC16LC7X/LCR72 | 25 | — | — | | ns |
| | | | Asynchronous | PIC16C7X/CR72 | 30 | — | — | | ns |
| | | | PIC16LC7X/LCR72 | 50 | — | — | ns | | |
| 47* | Tt1P | T1CKI input period | Synchronous | PIC16C7X/CR72 | Greater of: 30 OR $\frac{T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 2, 4, 8) |
| | | | | PIC16LC7X/LCR72 | Greater of: 50 OR $\frac{T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1, 2, 4, 8) |
| | | | Asynchronous | PIC16C7X/CR72 | 60 | — | — | ns | |
| | | | | PIC16LC7X/LCR72 | 100 | — | — | ns | |
| | Ft1 | Timer1 oscillator input frequency range (oscillator enabled by setting bit T10SCEN) | | DC | — | 200 | kHz | | |
| 48 | TCKEZtmr1 | Delay from external clock edge to timer increment | | $2T_{osc}$ | — | $7T_{osc}$ | — | | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 13-7: CAPTURE/COMPARE/PWM TIMINGS (CCP1)

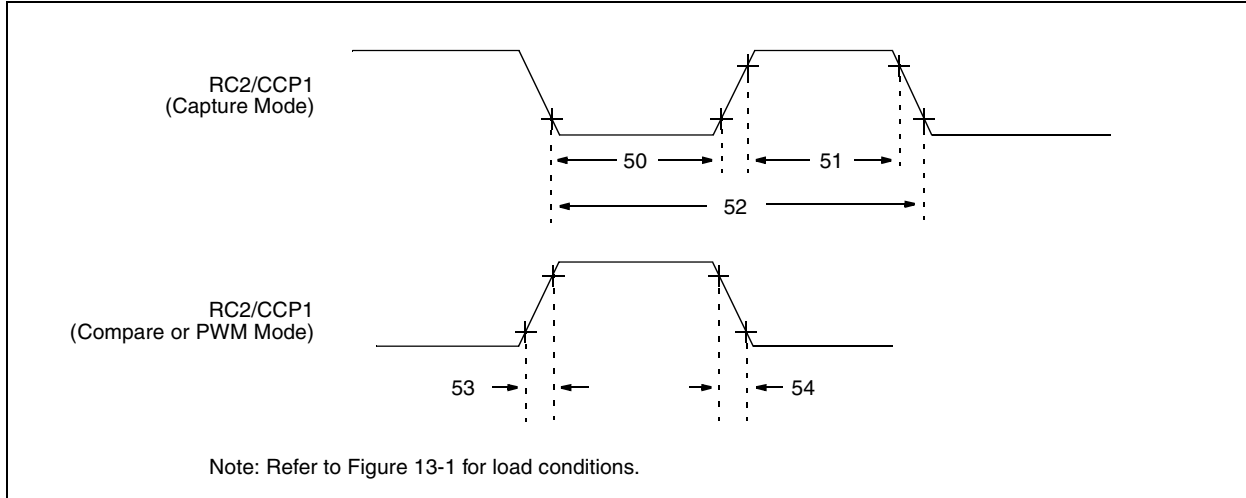


TABLE 13-7 CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

| Param No. | Sym | Characteristic | | Min | Typ† | Max | Units | Conditions | |
|-----------|------|-----------------------|-----------------|--------------------------|------|-----|-------|--------------------------------|----|
| 50* | TccL | CCP1 input low time | No Prescaler | $0.5T_{CY} + 20$ | — | — | ns | | |
| | | | With Prescaler | PIC16C72/CR72 | 10 | — | — | | ns |
| | | | | PIC16LC72/LCR72 | 20 | — | — | | ns |
| 51* | TccH | CCP1 input high time | No Prescaler | $0.5T_{CY} + 20$ | — | — | ns | | |
| | | | With Prescaler | PIC16C72/CR72 | 10 | — | — | | ns |
| | | | | PIC16LC72/LCR72 | 20 | — | — | | ns |
| 52* | TccP | CCP1 input period | | $\frac{3T_{CY} + 40}{N}$ | — | — | ns | N = prescale value (1,4 or 16) | |
| 53* | TccR | CCP1 output rise time | PIC16C72/CR72 | — | 10 | 25 | ns | | |
| | | | PIC16LC72/LCR72 | — | 25 | 45 | ns | | |
| 54* | TccF | CCP1 output fall time | PIC16C72/CR72 | — | 10 | 25 | ns | | |
| | | | PIC16LC72/LCR72 | — | 25 | 45 | ns | | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-8: SPI MASTER OPERATION TIMING (CKE = 0)

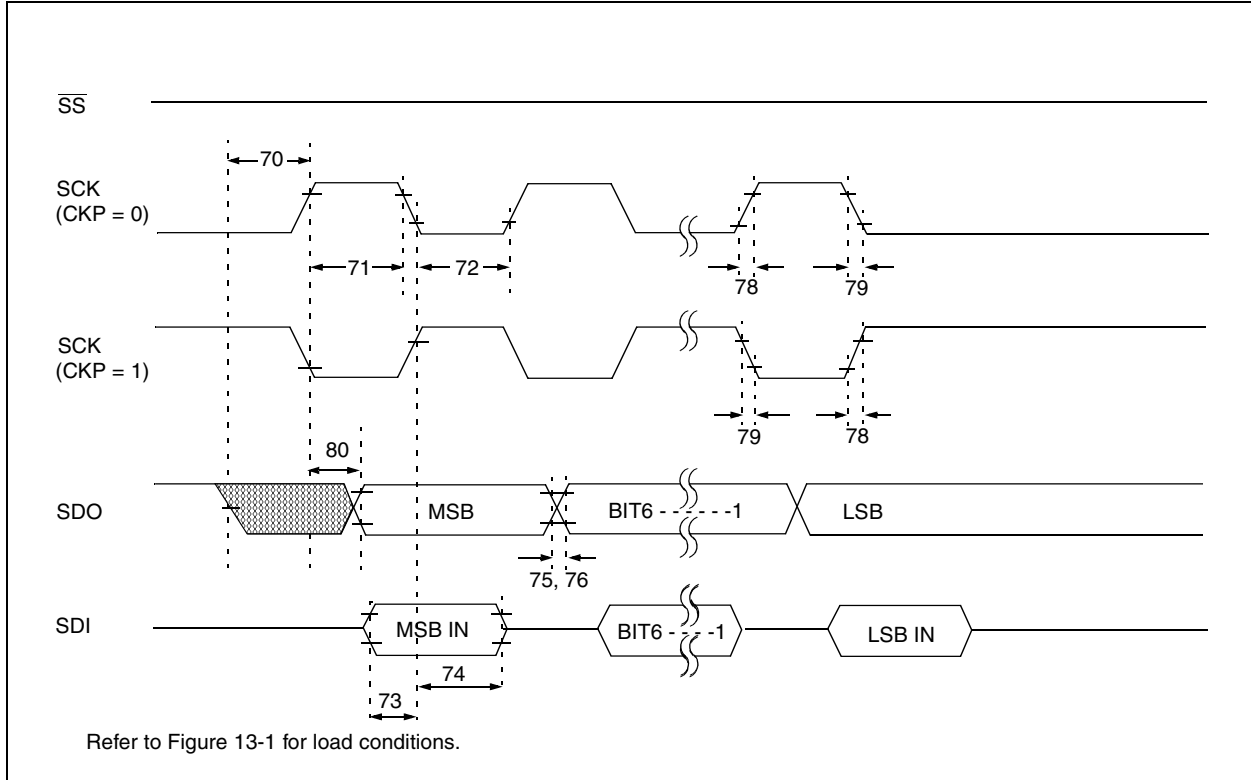
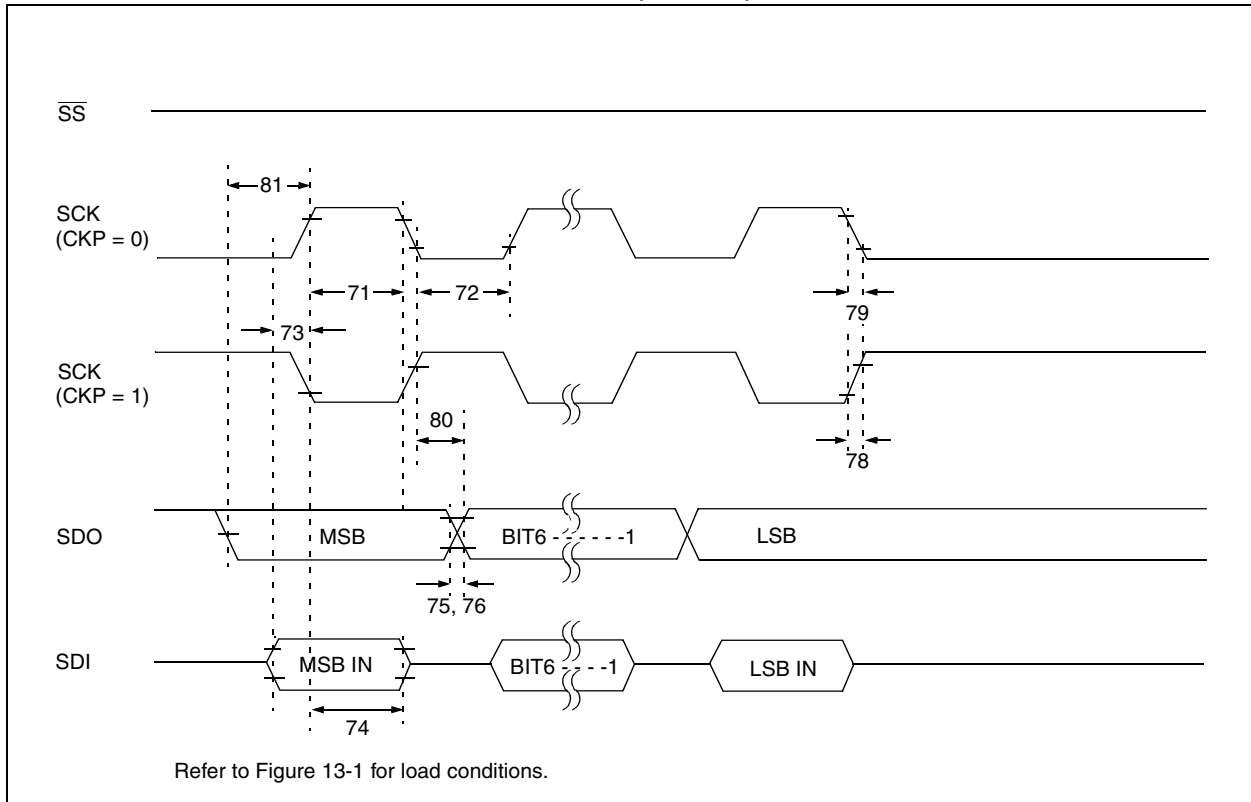


FIGURE 13-9: SPI MASTER OPERATION TIMING (CKE = 1)



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FIGURE 13-10: SPI SLAVE MODE TIMING (CKE = 0)

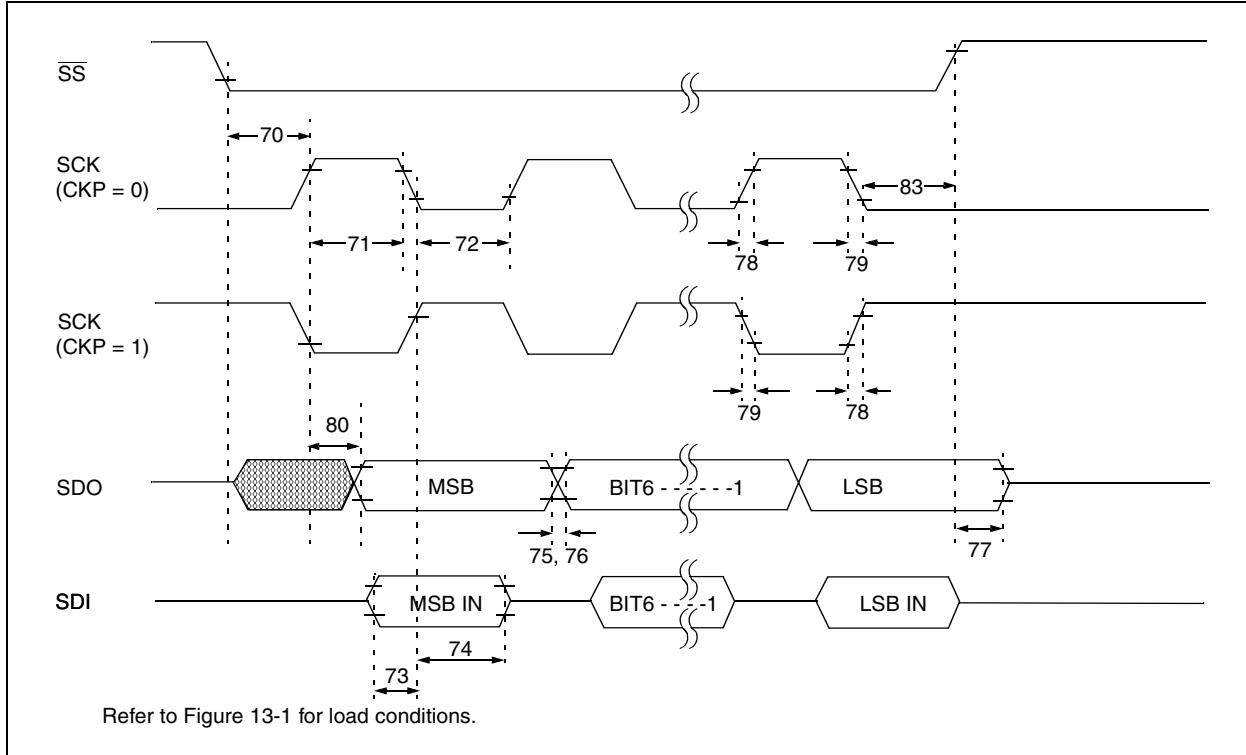


FIGURE 13-11: SPI SLAVE MODE TIMING (CKE = 1)

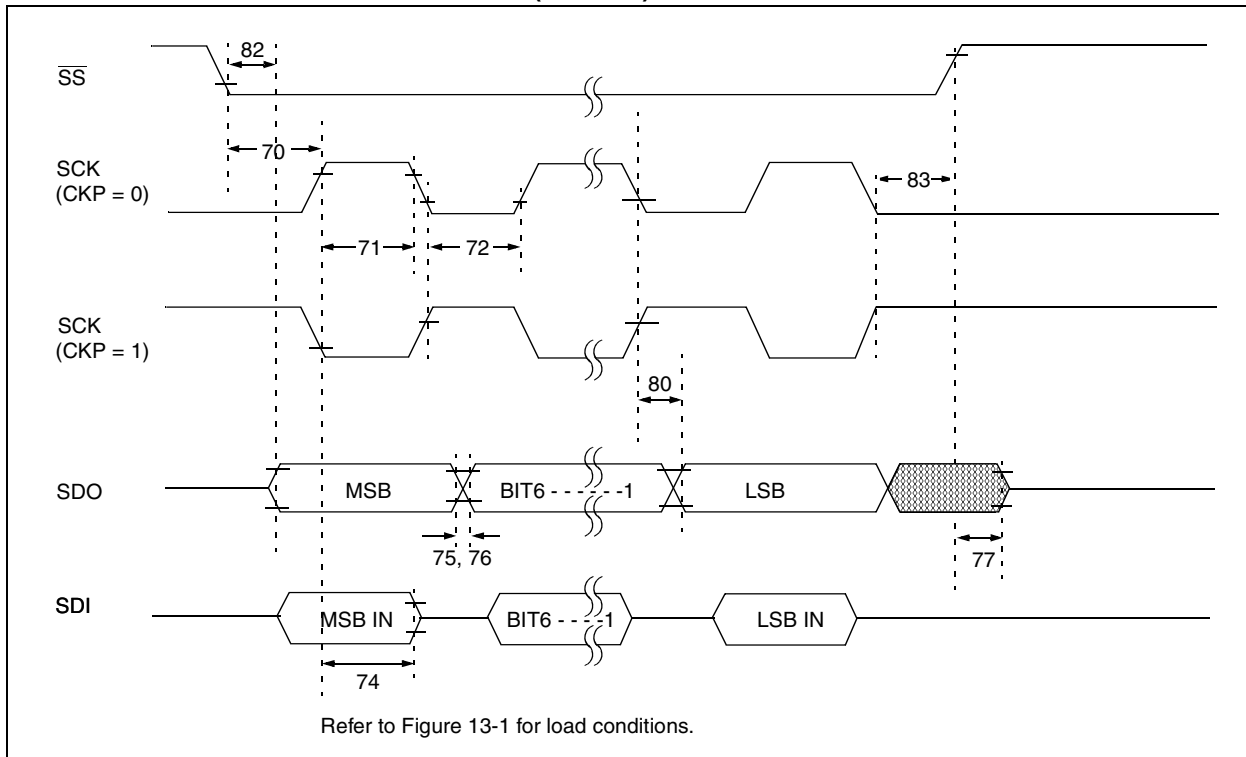


TABLE 13-8 SPI SLAVE MODE REQUIREMENTS (CKE=0) - PIC16C72

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|-----------|-----------------------|--|----------------------|------|-----|-------|------------|
| 70 | TssL2scH, TssL2scL | SS↓ to SCK↓ or SCK↑ input | T _{CY} | — | — | ns | |
| 71 | TscH | SCK input high time (slave mode) | T _{CY} + 20 | — | — | ns | |
| 72 | TscL | SCK input low time (slave mode) | T _{CY} + 20 | — | — | ns | |
| 73 | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 50 | — | — | ns | |
| 74 | Tsch2diL, TscL2diL | Hold time of SDI data input to SCK edge | 50 | — | — | ns | |
| 75 | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76 | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77 | TssH2doZ | SS↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78 | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79 | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80 | Tsch2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 13-9 SPI MODE REQUIREMENTS - PIC16CR72

| Parameter No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions |
|---------------|-----------------------|--|-------------------------|------|-----|-------|------------|
| 70* | TssL2scH, TssL2scL | SS↓ to SCK↓ or SCK↑ input | T _{CY} | — | — | ns | |
| 71* | TscH | SCK input high time (slave mode) | T _{CY} + 20 | — | — | ns | |
| 72* | TscL | SCK input low time (slave mode) | T _{CY} + 20 | — | — | ns | |
| 73* | TdiV2scH, TdiV2scL | Setup time of SDI data input to SCK edge | 100 | — | — | ns | |
| 74* | Tsch2diL, TscL2diL | Hold time of SDI data input to SCK edge | 100 | — | — | ns | |
| 75* | TdoR | SDO data output rise time | — | 10 | 25 | ns | |
| 76* | TdoF | SDO data output fall time | — | 10 | 25 | ns | |
| 77* | TssH2doZ | SS↑ to SDO output hi-impedance | 10 | — | 50 | ns | |
| 78* | TscR | SCK output rise time (master mode) | — | 10 | 25 | ns | |
| 79* | TscF | SCK output fall time (master mode) | — | 10 | 25 | ns | |
| 80* | Tsch2doV, TscL2doV | SDO data output valid after SCK edge | — | — | 50 | ns | |
| 81* | TdoV2scH, TdoV2scL | SDO data output setup to SCK edge | T _{CY} | — | — | ns | |
| 82* | TssL2doV | SDO data output valid after SS↓ edge | — | — | 50 | ns | |
| 83* | Tsch2ssH, TscL2ssH | SS↑ after SCK edge | 1.5T _{CY} + 40 | — | — | ns | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 13-12: I²C BUS START/STOP BITS TIMING

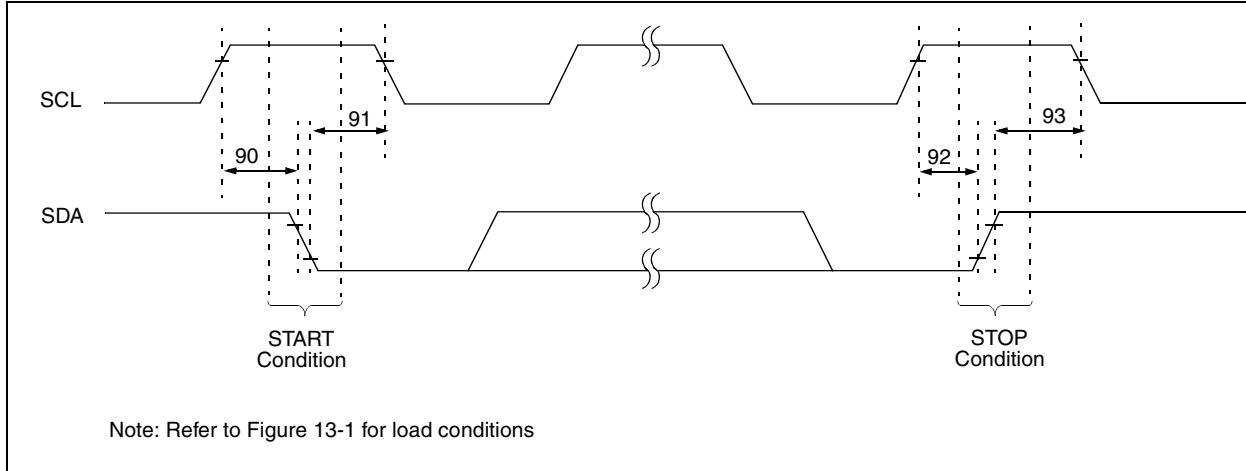


TABLE 13-10 I²C BUS START/STOP BITS REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions | |
|---------------|---------|----------------------------|--------------|------|-----|-------|------------|--|
| 90 | TSU:STA | START condition Setup time | 100 kHz mode | 4700 | — | — | ns | Only relevant for repeated START condition |
| | | 400 kHz mode | 600 | — | — | | | |
| 91 | THD:STA | START condition Hold time | 100 kHz mode | 4000 | — | — | ns | After this period the first clock pulse is generated |
| | | 400 kHz mode | 600 | — | — | | | |
| 92 | TSU:STO | STOP condition Setup time | 100 kHz mode | 4700 | — | — | ns | |
| | | 400 kHz mode | 600 | — | — | | | |
| 93 | THD:STO | STOP condition Hold time | 100 kHz mode | 4000 | — | — | ns | |
| | | 400 kHz mode | 600 | — | — | | | |

FIGURE 13-13: I²C BUS DATA TIMING

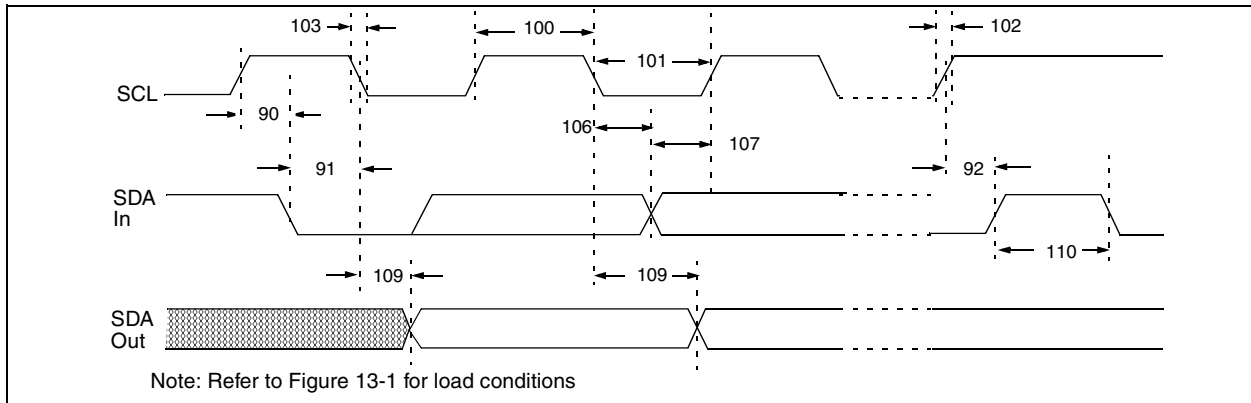


TABLE 13-11 I²C BUS DATA REQUIREMENTS

| Parameter No. | Sym | Characteristic | Min | Max | Units | Conditions | |
|---------------|---------------------|----------------------------|--------------|------------------------|-------|------------|---|
| 100 | T _{HIGH} | Clock high time | 100 kHz mode | 4.0 | — | μs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5T _{CY} | — | | |
| 101 | T _{LOW} | Clock low time | 100 kHz mode | 4.7 | — | μs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5T _{CY} | — | | |
| 102 | T _R | SDA and SCL rise time | 100 kHz mode | — | 1000 | ns | |
| | | | 400 kHz mode | 20 + 0.1C _b | 300 | ns | C _b is specified to be from 10 to 400 pF |
| 103 | T _F | SDA and SCL fall time | 100 kHz mode | — | 300 | ns | |
| | | | 400 kHz mode | 20 + 0.1C _b | 300 | ns | C _b is specified to be from 10 to 400 pF |
| 90 | T _{SU:STA} | START condition setup time | 100 kHz mode | 4.7 | — | μs | Only relevant for repeated START condition |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 91 | T _{HD:STA} | START condition hold time | 100 kHz mode | 4.0 | — | μs | After this period the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 106 | T _{HD:DAT} | Data input hold time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| 107 | T _{SU:DAT} | Data input setup time | 100 kHz mode | 250 | — | ns | Note 2 |
| | | | 400 kHz mode | 100 | — | ns | |
| 92 | T _{SU:STO} | STOP condition setup time | 100 kHz mode | 4.7 | — | μs | |
| | | | 400 kHz mode | 0.6 | — | μs | |
| 109 | T _{AA} | Output valid from clock | 100 kHz mode | — | 3500 | ns | Note 1 |
| | | | 400 kHz mode | — | — | ns | |
| 110 | T _{BUF} | Bus free time | 100 kHz mode | 4.7 | — | μs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | C _b | Bus capacitive loading | — | 400 | pF | | |

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement t_{SU:DAT} ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line T_R max. + t_{SU:DAT} = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

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TABLE 13-12 A/D CONVERTER CHARACTERISTICS:
PIC16C72/CR72-04 (Commercial, Industrial, Extended)
PIC16C72/CR72-10 (Commercial, Industrial, Extended)
PIC16C72/CR72-20 (Commercial, Industrial, Extended)
PIC16LC72/LCR72-04 (Commercial, Industrial)

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions | |
|-----------|------|--|-----------------|------------|------------|-------|---|--|
| A01 | NR | Resolution | — | — | 8 bits | bit | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A02 | EABS | Total Absolute error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A03 | EIL | Integral linearity error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A04 | EDL | Differential linearity error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A05 | EFS | Full scale error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A06 | EOFF | Offset error | — | — | < ± 1 | LSb | VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF | |
| A10 | — | Monotonicity | — | guaranteed | — | — | VSS ≤ VAIN ≤ VREF | |
| A20 | VREF | Reference voltage | 2.5V | — | VDD + 0.3 | V | | |
| A25 | VAIN | Analog input voltage | VSS - 0.3 | — | VREF + 0.3 | V | | |
| A30 | ZAIN | Recommended impedance of analog voltage source | — | — | 10.0 | kΩ | | |
| A40 | IAD | A/D conversion current (VDD) | PIC16C72/CR72 | — | 180 | — | μA | Average current consumption when A/D is on. (Note 1) |
| | | | PIC16LC72/LCR72 | — | 90 | — | μA | |
| A50 | IREF | VREF input current (Note 2) | 10 | — | 1000 | μA | During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 9.1. | |
| | | | — | — | 10 | μA | During A/D Conversion cycle | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

Note 2: VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

FIGURE 13-14: A/D CONVERSION TIMING

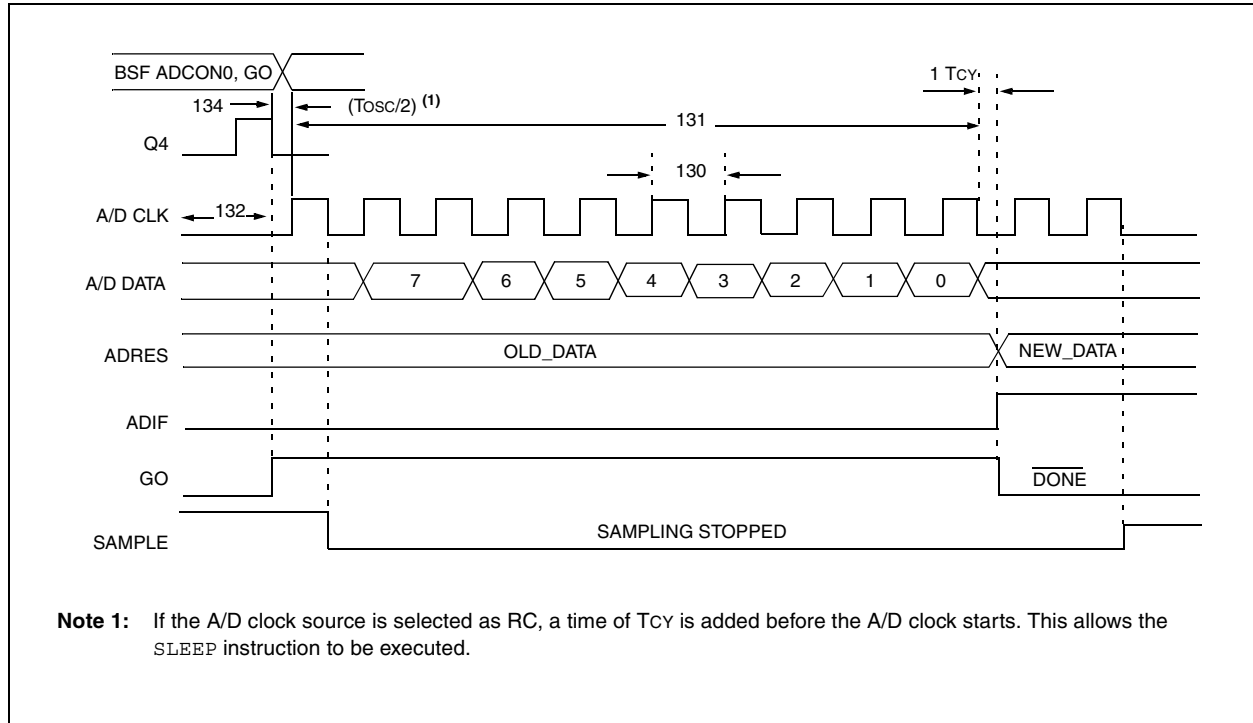


TABLE 13-13 A/D CONVERSION REQUIREMENTS

| Param No. | Sym | Characteristic | Min | Typ† | Max | Units | Conditions | |
|-----------|------|---|-----------------|---------------|-----|---------------|---|----------------------------------|
| 130 | TAD | A/D clock period | PIC16C72/LCR72 | 1.6 | — | — | μs | TOSC based, $V_{REF} \geq 2.5V$ |
| | | | PIC16LC72/LCR72 | 2.0 | — | — | μs | TOSC based, V_{REF} full range |
| | | | PIC16C72/LCR72 | 2.0 | 4.0 | 6.0 | μs | A/D RC Mode |
| | | | PIC16LC72/LCR72 | 2.5 | 6.0 | 9.0 | μs | A/D RC Mode |
| 131 | TCNV | Conversion time (not including S/H time) (Note 1) | — | 9.5 | — | TAD | | |
| 132 | TACQ | Acquisition time | Note 2 | 20 | — | μs | The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1 LSb (i.e., 20.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD). | |
| | | | 5* | — | — | μs | | |
| 134 | Tgo | Q4 to A/D clock start | — | $T_{OSC}/2$ § | — | — | If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the <code>SLEEP</code> instruction to be executed. | |
| 135 | Tswc | Switching from convert → sample time | 1.5 § | — | — | TAD | | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES register may be read on the following T_{CY} cycle.

Note 2: See Section 9.1 for min conditions.

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NOTES:

14.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES - PIC16C72

The graphs and tables provided in this section are for **design guidance** and are **not tested or guaranteed**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C, while 'max' or 'min' represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

FIGURE 14-1: TYPICAL IPD vs. VDD (WDT DISABLED, RC MODE)

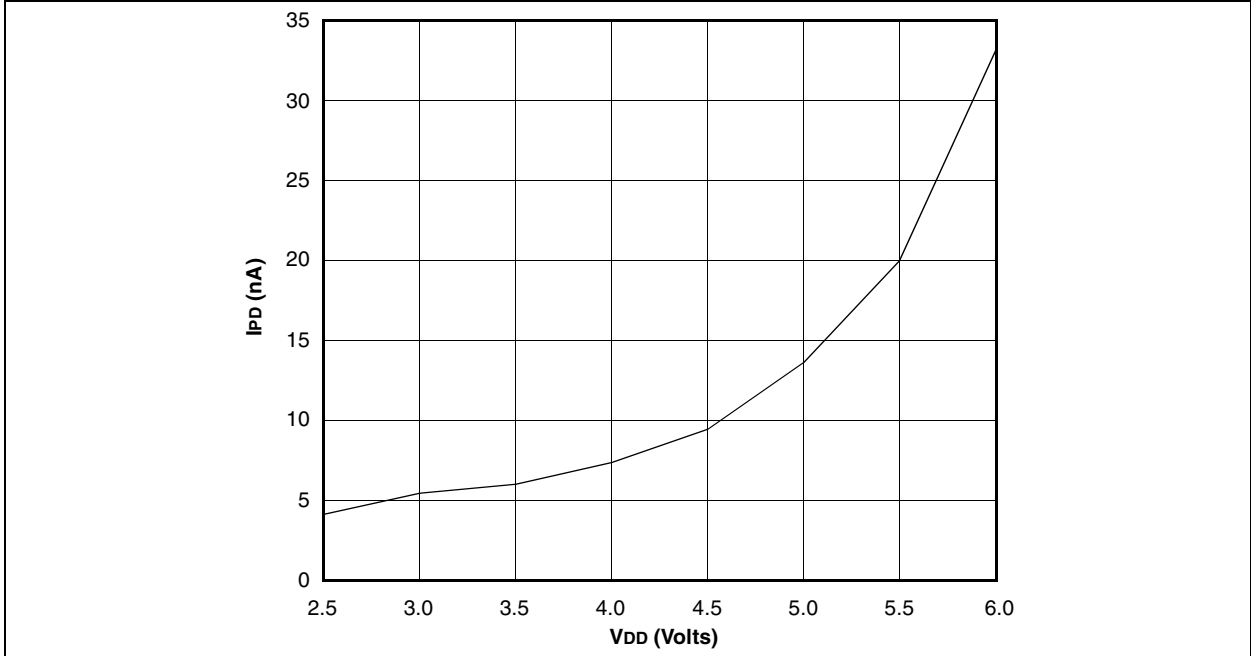


FIGURE 14-2: MAXIMUM IPD vs. VDD (WDT DISABLED, RC MODE)

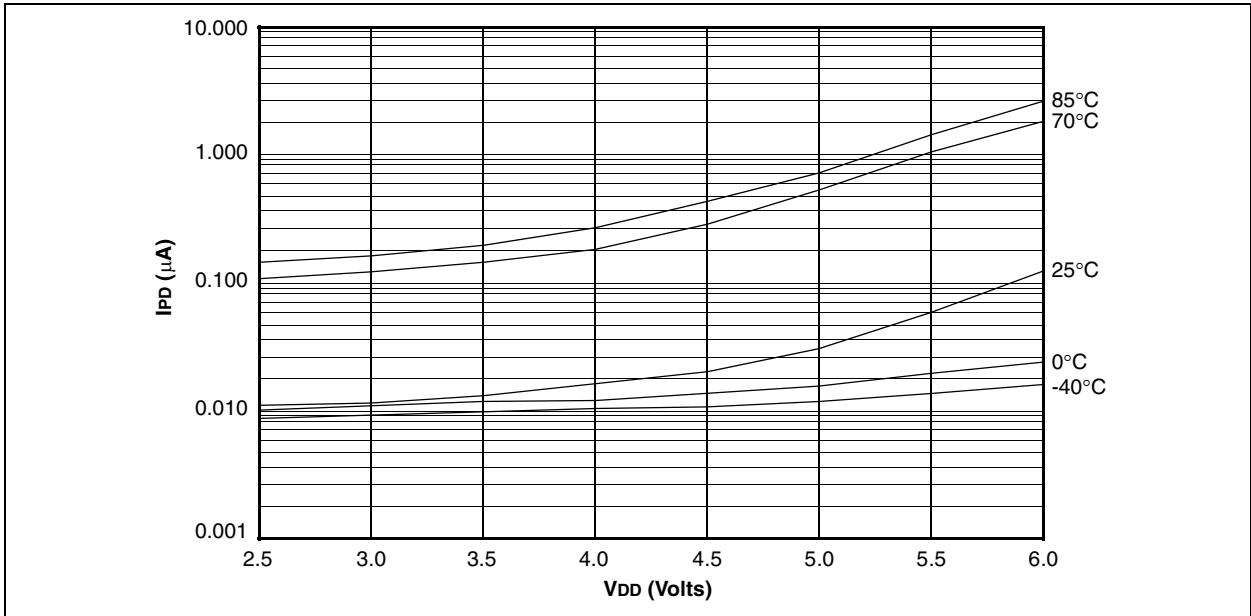


FIGURE 14-3: TYPICAL I_{PD} vs. V_{DD} @ 25°C (WDT ENABLED, RC MODE)

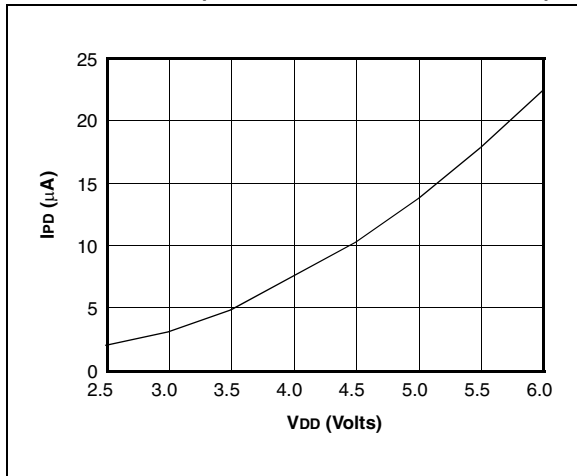


FIGURE 14-5: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}

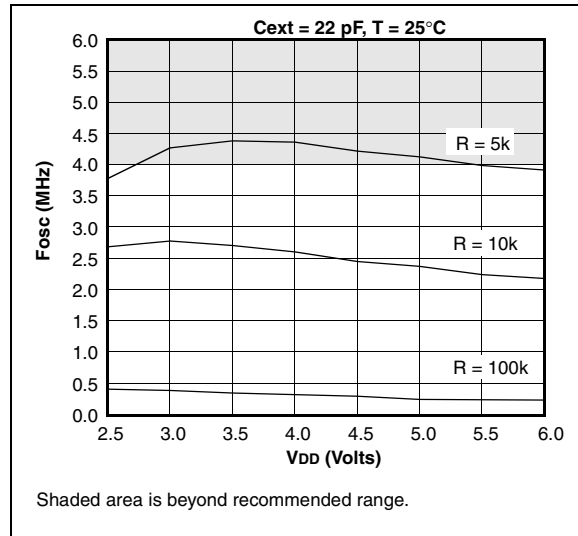


FIGURE 14-4: MAXIMUM I_{PD} vs. V_{DD} (WDT ENABLED, RC MODE)

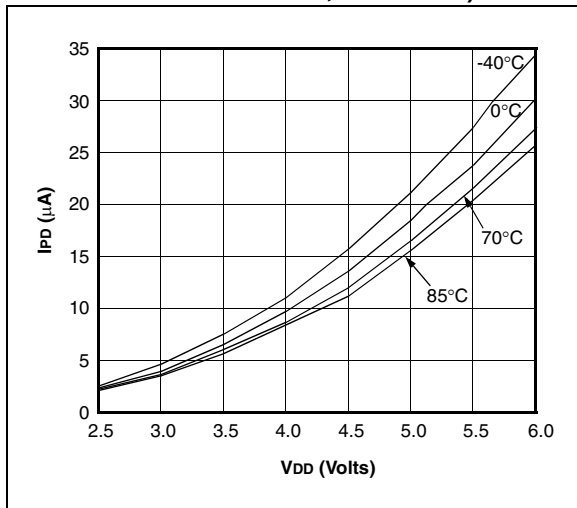


FIGURE 14-6: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}

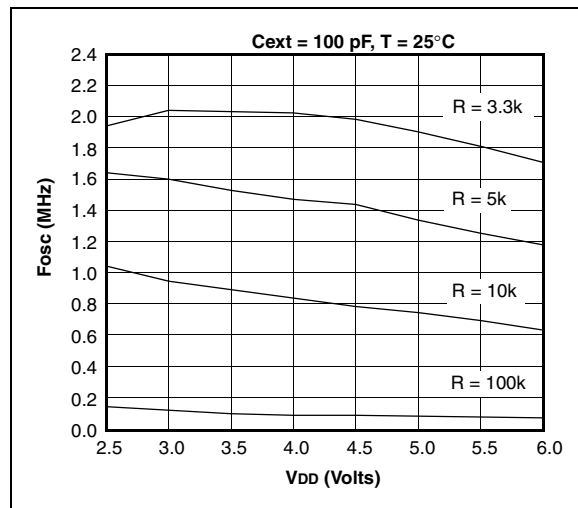
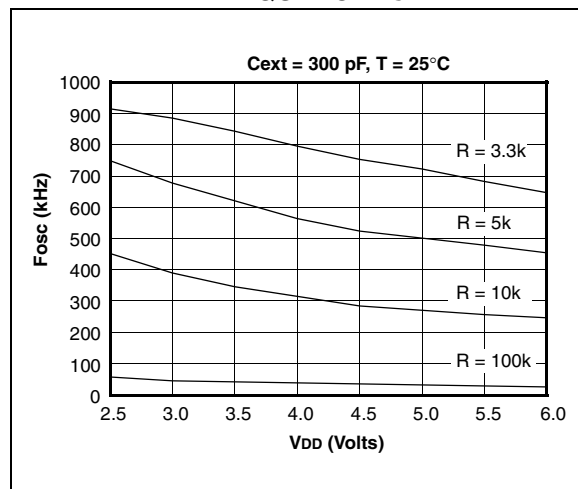


FIGURE 14-7: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}



Data based on matrix samples. See first page of this section for details.

FIGURE 14-8: TYPICAL I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (RC MODE)

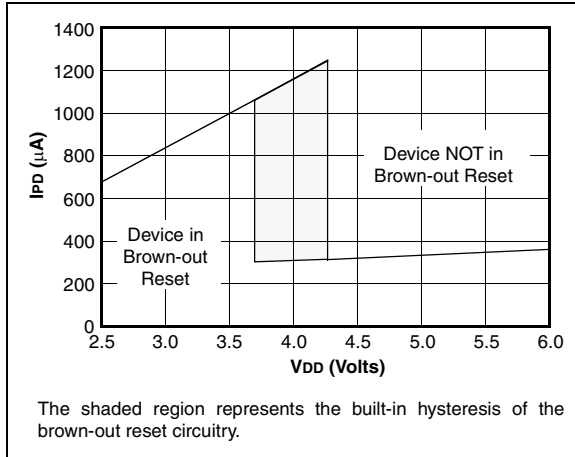


FIGURE 14-9: MAXIMUM I_{PD} vs. V_{DD} BROWN-OUT DETECT ENABLED (85°C TO -40°C, RC MODE)

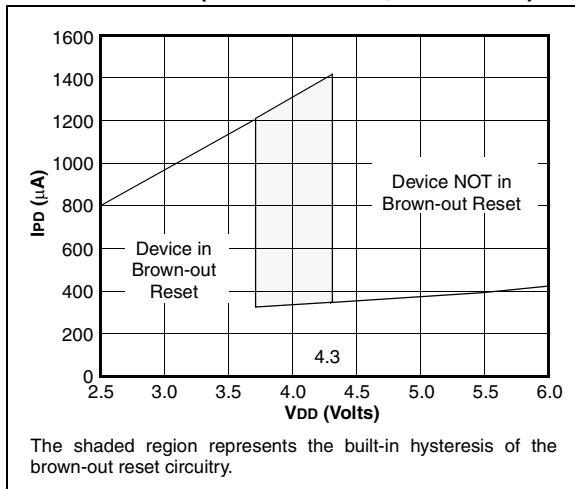


FIGURE 14-10: TYPICAL I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, RC MODE)

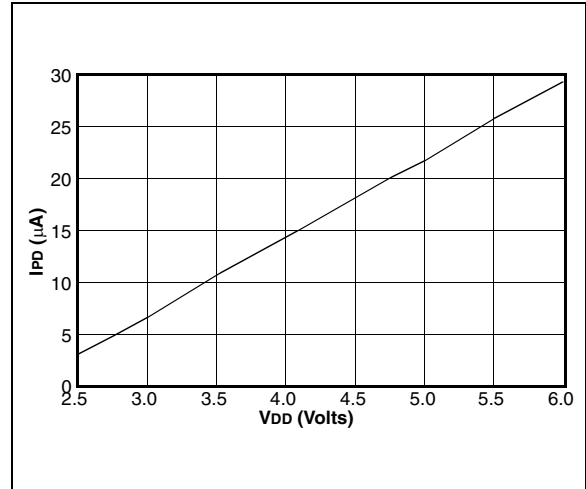
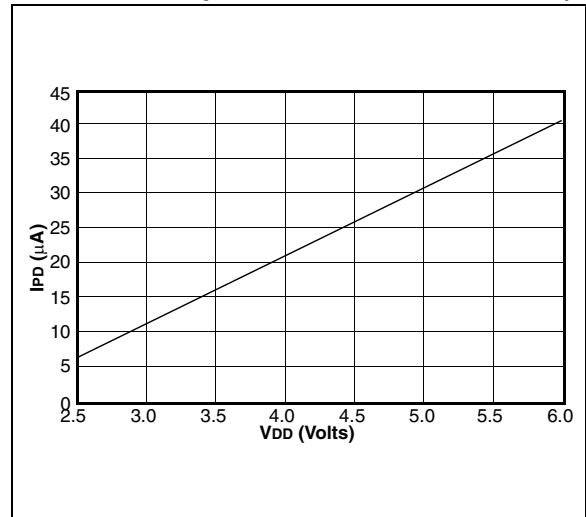


FIGURE 14-11: MAXIMUM I_{PD} vs. TIMER1 ENABLED (32 kHz, RC0/RC1 = 33 pF/33 pF, 85°C TO -40°C, RC MODE)



Data based on matrix samples. See first page of this section for details.

FIGURE 14-12: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 22 pF, 25°C)

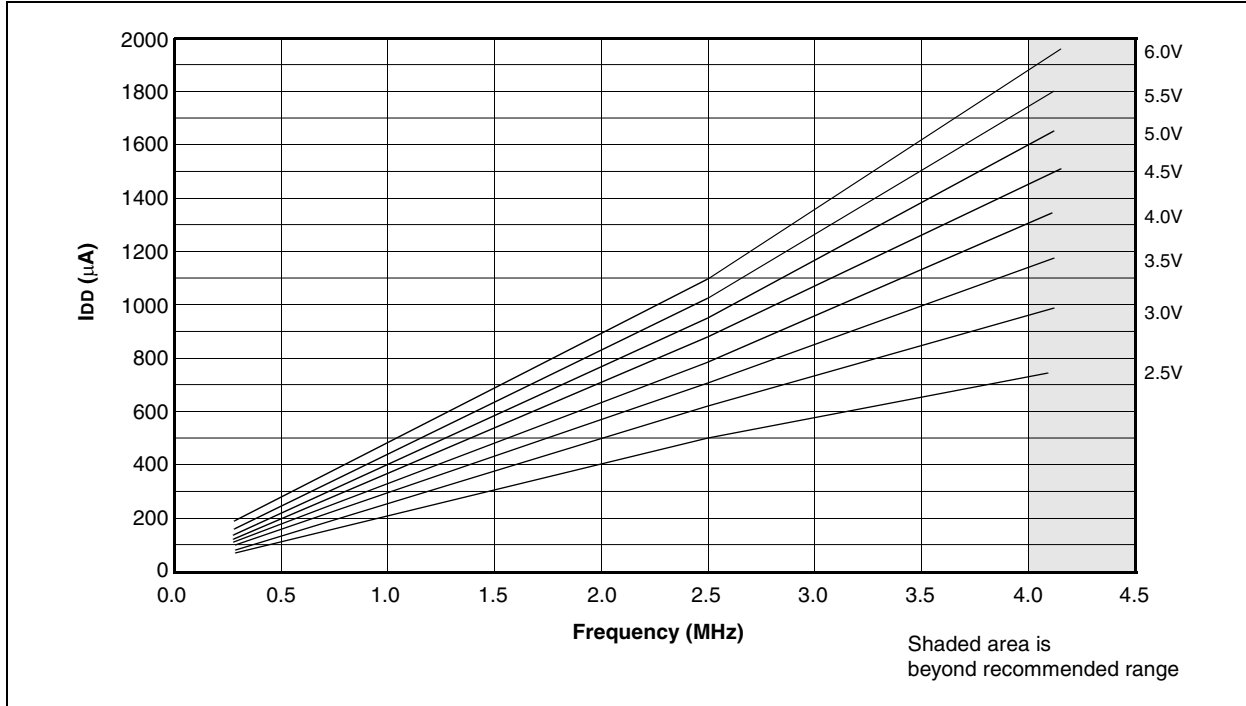
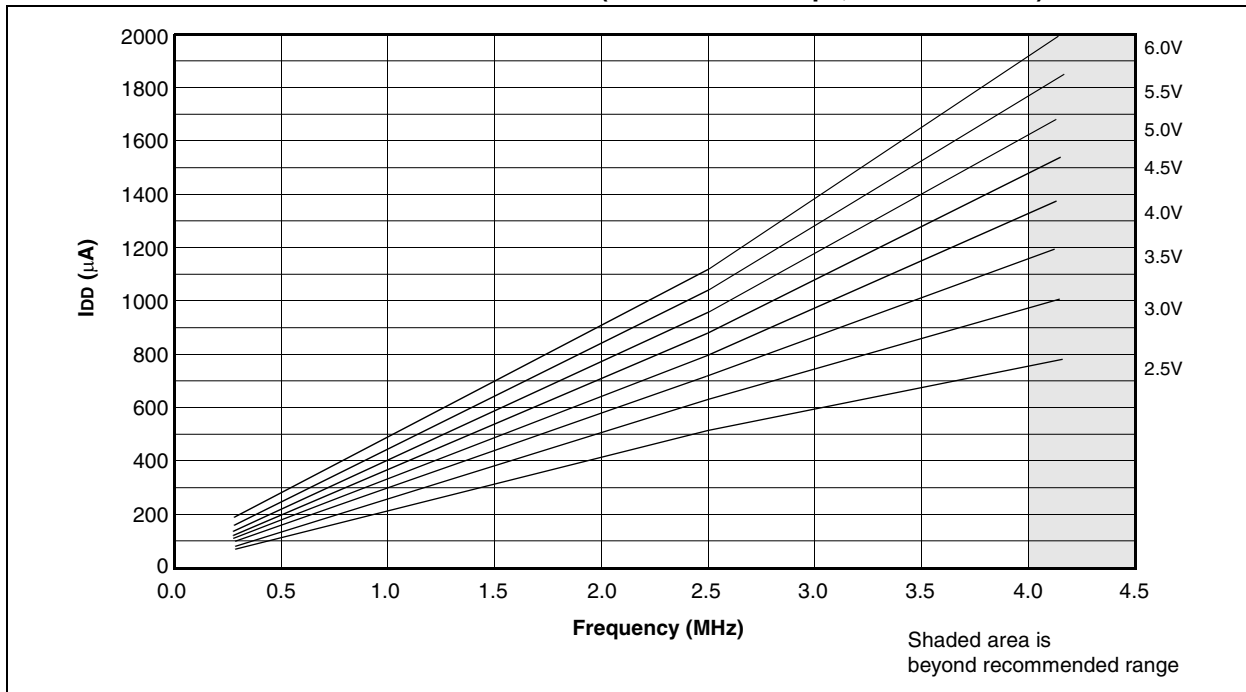


FIGURE 14-13: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 22 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

FIGURE 14-14: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 100 pF, 25°C)

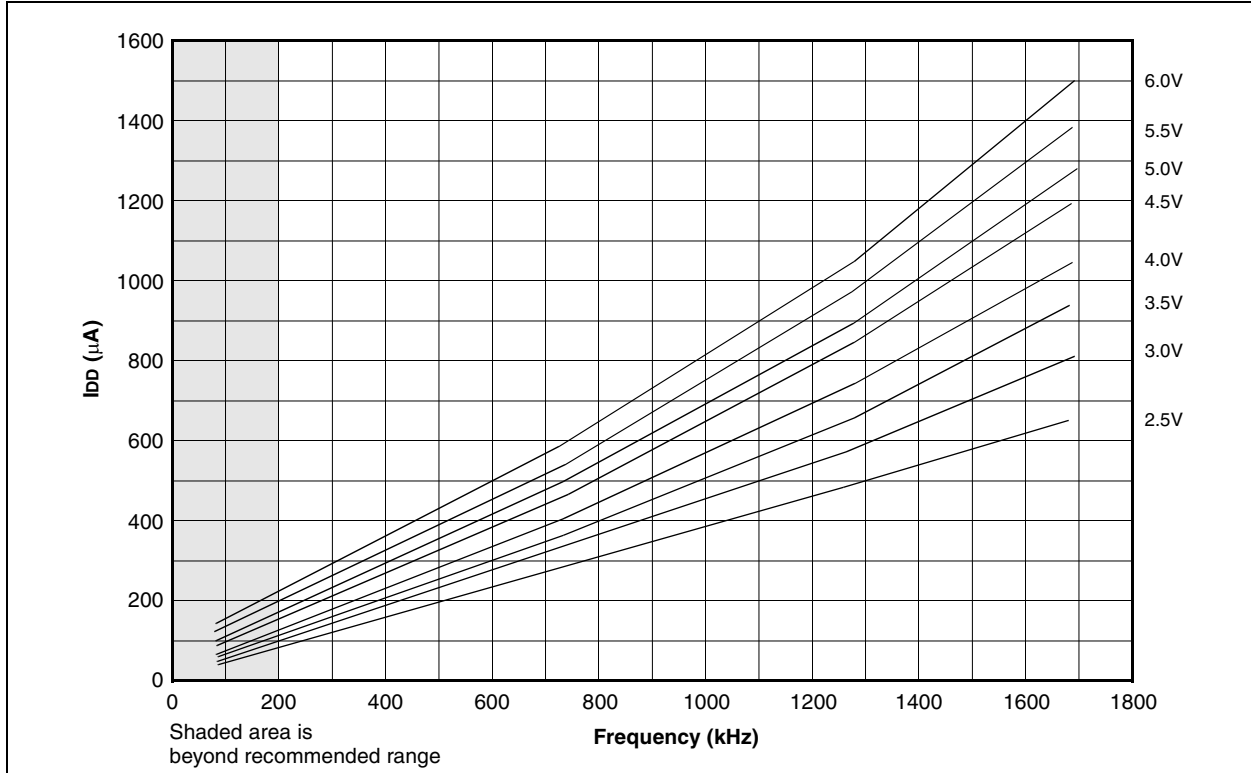
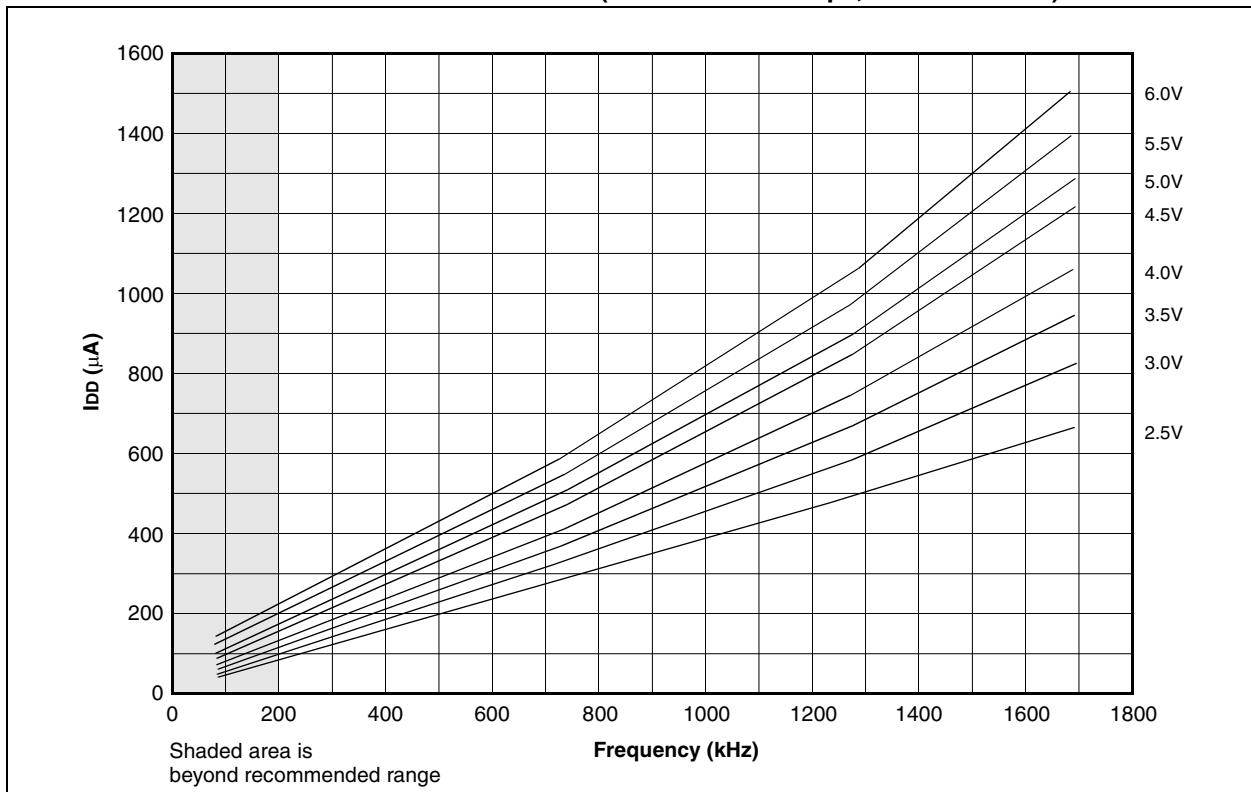


FIGURE 14-15: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 100 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

FIGURE 14-16: TYPICAL I_{DD} vs. FREQUENCY (RC MODE @ 300 pF, 25°C)

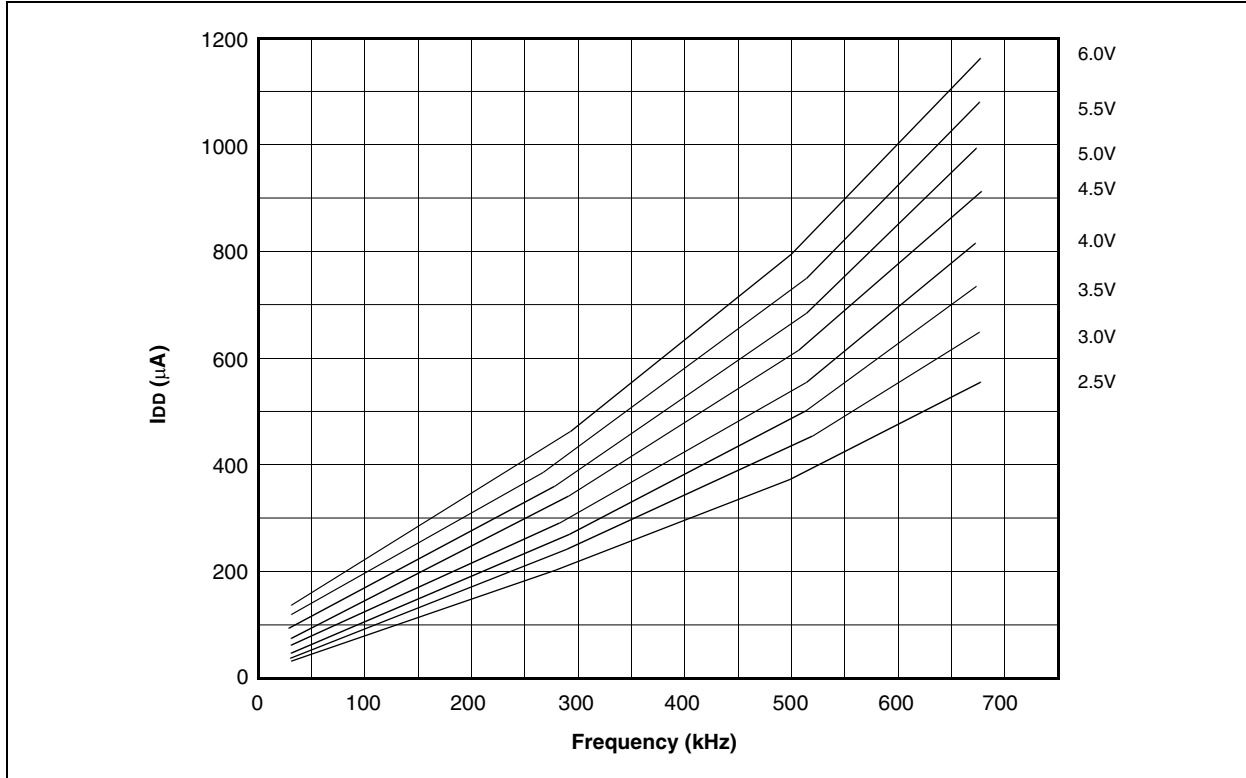
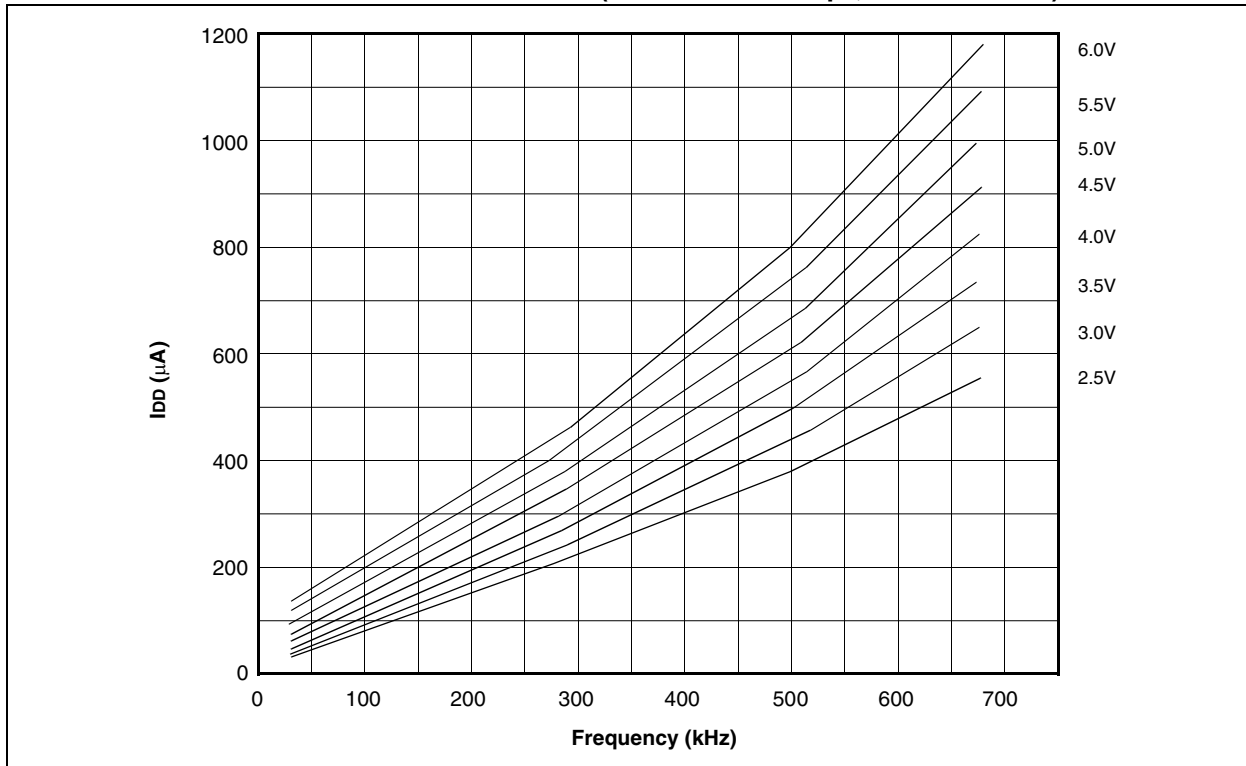


FIGURE 14-17: MAXIMUM I_{DD} vs. FREQUENCY (RC MODE @ 300 pF, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

FIGURE 14-18: TYPICAL I_{DD} vs. CAPACITANCE @ 500 kHz (RC MODE)

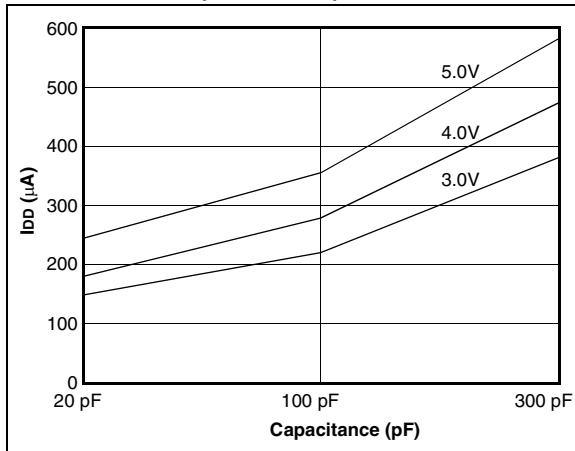


TABLE 14-1 RC OSCILLATOR FREQUENCIES

| Cext | Rext | Average | |
|--------|------|-----------------|--------|
| | | Fosc @ 5V, 25°C | |
| 22 pF | 5k | 4.12 MHz | ± 1.4% |
| | 10k | 2.35 MHz | ± 1.4% |
| | 100k | 268 kHz | ± 1.1% |
| 100 pF | 3.3k | 1.80 MHz | ± 1.0% |
| | 5k | 1.27 MHz | ± 1.0% |
| | 10k | 688 kHz | ± 1.2% |
| 300 pF | 100k | 77.2 kHz | ± 1.0% |
| | 3.3k | 707 kHz | ± 1.4% |
| | 5k | 501 kHz | ± 1.2% |
| | 10k | 269 kHz | ± 1.6% |
| | 100k | 28.3 kHz | ± 1.1% |

The percentage variation indicated here is part to part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for V_{DD} = 5V.

FIGURE 14-19: TRANSCONDUCTANCE(g_m) OF HS OSCILLATOR vs. V_{DD}

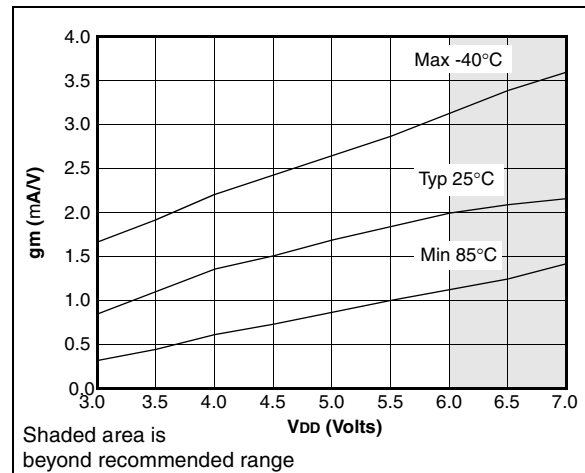


FIGURE 14-20: TRANSCONDUCTANCE(g_m) OF LP OSCILLATOR vs. V_{DD}

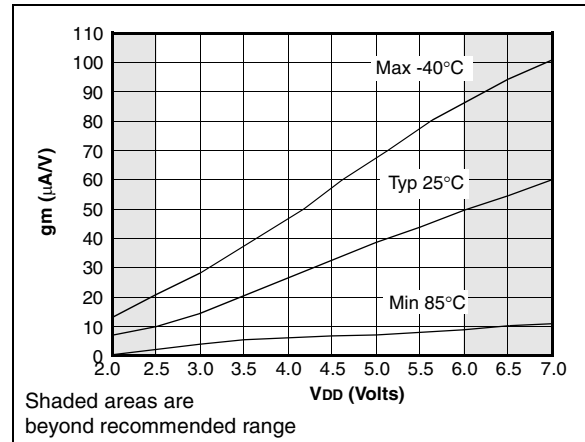
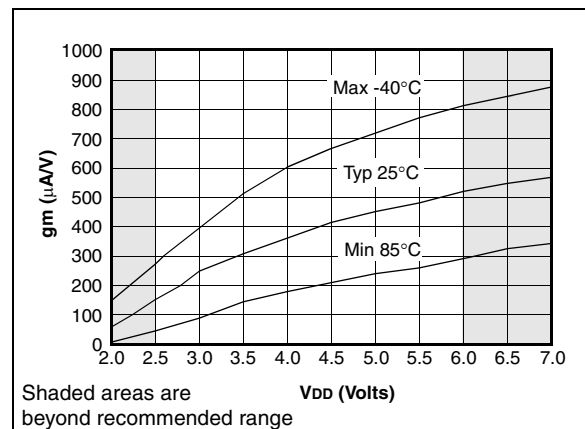


FIGURE 14-21: TRANSCONDUCTANCE(g_m) OF XT OSCILLATOR vs. V_{DD}



Data based on matrix samples. See first page of this section for details.

FIGURE 14-22: TYPICAL XTAL STARTUP TIME vs. VDD (LP MODE, 25°C)

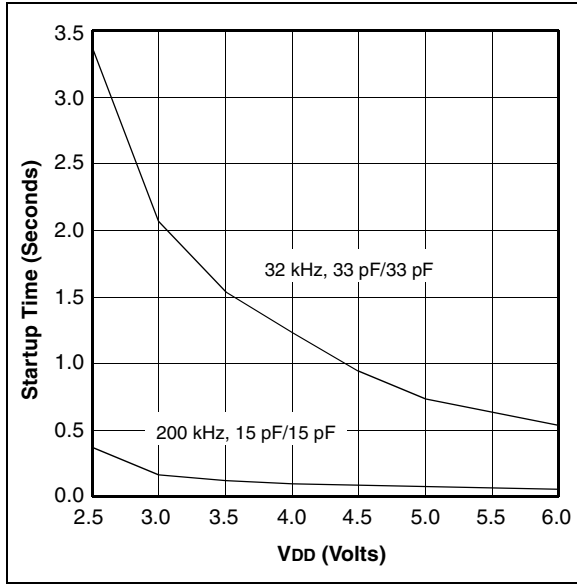


FIGURE 14-24: TYPICAL XTAL STARTUP TIME vs. VDD (XT MODE, 25°C)

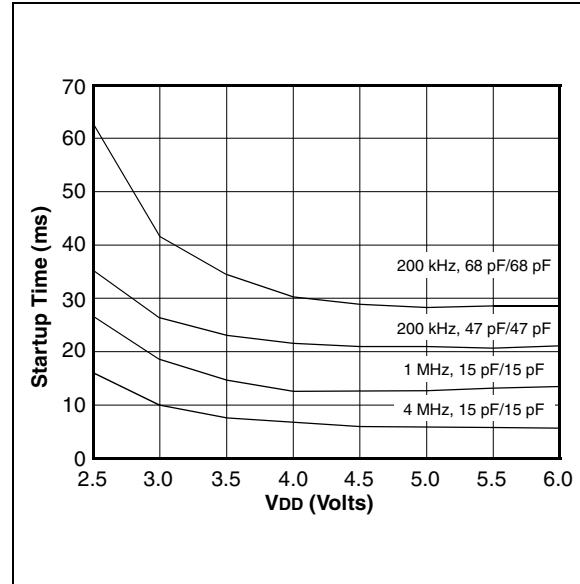


FIGURE 14-23: TYPICAL XTAL STARTUP TIME vs. VDD (HS MODE, 25°C)

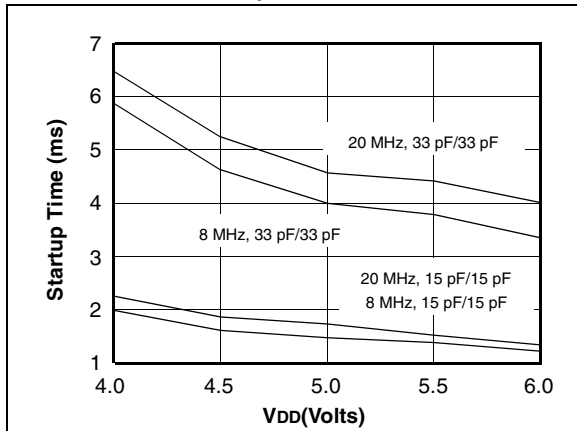


TABLE 14-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATORS

| Osc Type | Crystal Freq | Cap. Range C1 | Cap. Range C2 |
|----------------------|------------------------|---------------|---------------|
| LP | 32 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15-33 pF | 15-33 pF |
| | 20 MHz | 15-33 pF | 15-33 pF |
| Crystals Used | | | |
| 32 kHz | Epson C-001R32.768K-A | | ± 20 PPM |
| 200 kHz | STD XTL 200.000KHz | | ± 20 PPM |
| 1 MHz | ECS ECS-10-13-1 | | ± 50 PPM |
| 4 MHz | ECS ECS-40-20-1 | | ± 50 PPM |
| 8 MHz | EPSON CA-301 8.000M-C | | ± 30 PPM |
| 20 MHz | EPSON CA-301 20.000M-C | | ± 30 PPM |

Data based on matrix samples. See first page of this section for details.

FIGURE 14-25: TYPICAL I_{DD} vs. FREQUENCY (LP MODE, 25°C)

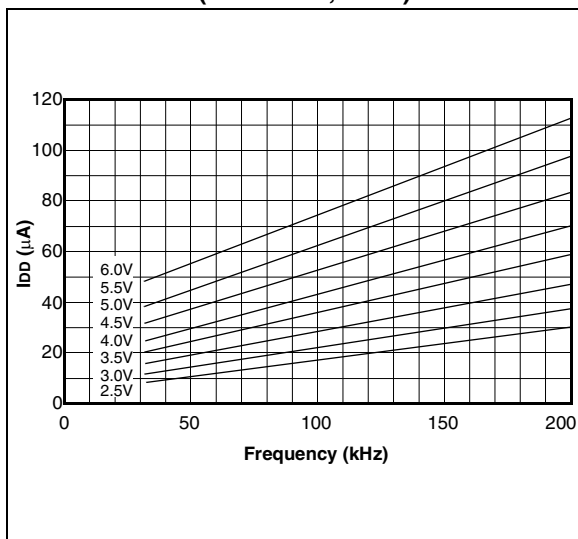


FIGURE 14-27: TYPICAL I_{DD} vs. FREQUENCY (XT MODE, 25°C)

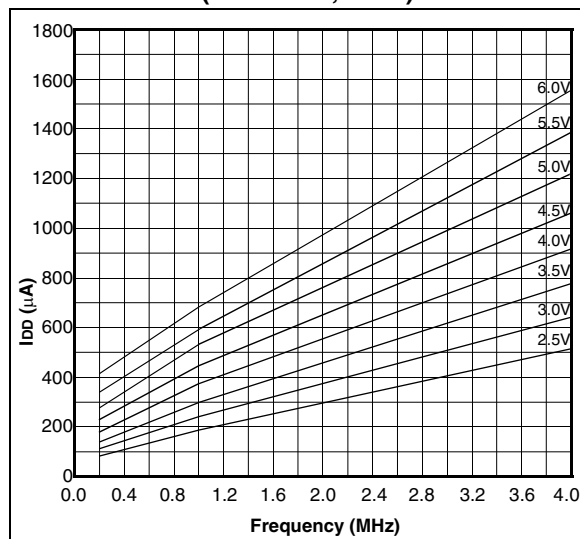


FIGURE 14-26: MAXIMUM I_{DD} vs. FREQUENCY (LP MODE, 85°C TO -40°C)

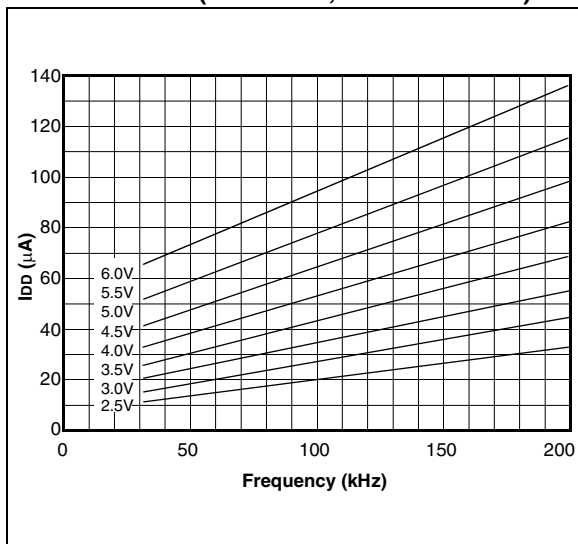
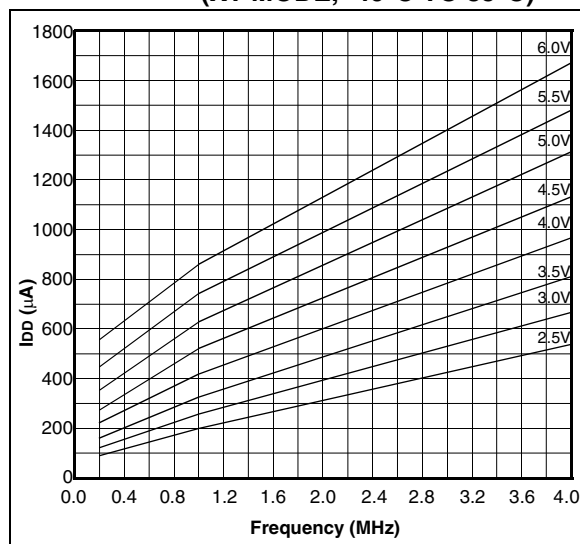
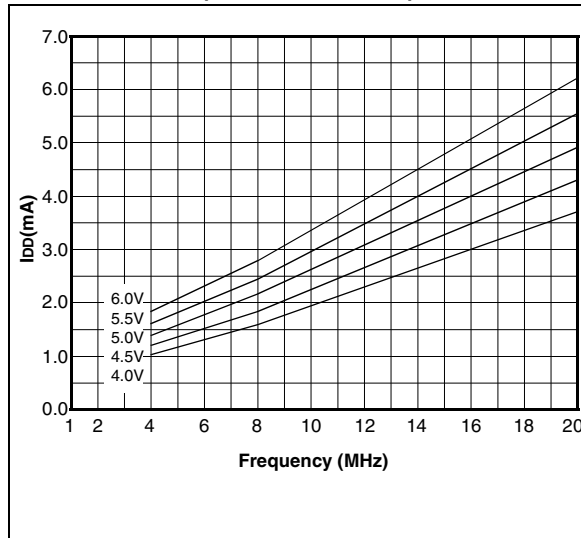


FIGURE 14-28: MAXIMUM I_{DD} vs. FREQUENCY (XT MODE, -40°C TO 85°C)



Data based on matrix samples. See first page of this section for details.

**FIGURE 14-29: TYPICAL I_{DD} vs. FREQUENCY
(HS MODE, 25°C)**



**FIGURE 14-30: MAXIMUM I_{DD} vs.
FREQUENCY
(HS MODE, -40°C TO 85°C)**

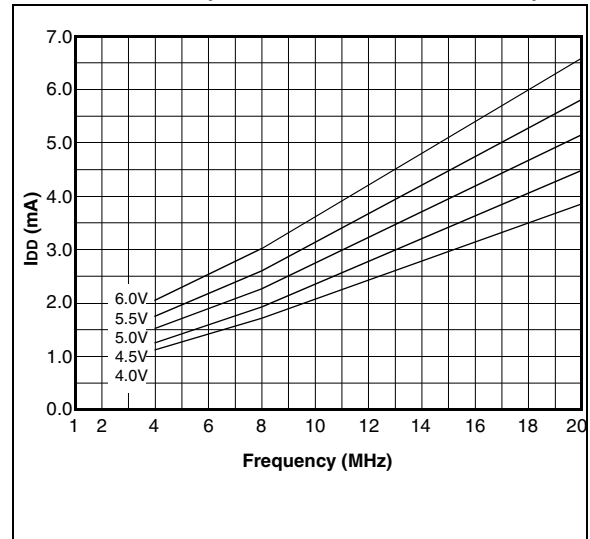


TABLE 14-3 TYPICAL EPROM ERASE TIME RECOMMENDATIONS

| Process Technology | Wavelength (Angstroms) | Intensity ($\mu\text{W}/\text{cm}^2$) | Distance from UV lamp (inches) | Typical Time ⁽¹⁾ (minutes) |
|--------------------|------------------------|---|--------------------------------|---------------------------------------|
| 57K | 2537 | 12,000 | 1 | 15 - 20 |
| 77K | 2537 | 12,000 | 1 | 20 |
| 90K | 2537 | 12,000 | 1 | 40 |
| 120K | 2537 | 12,000 | 1 | 60 |

Note 1: If these criteria are not met, the erase times will be different.

Note: Fluorescent lights and sunlight both emit ultraviolet light at the erasure wavelength. Leaving a UV erasable device's window uncovered could cause, over time, the devices memory cells to become erased. The erasure time for a fluorescent light is about three years. While sunlight requires only about one week. To prevent the memory cells from losing data an opaque label should be placed over the erasure window.

Data based on matrix samples. See first page of this section for details.

15.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES - PIC16CR72

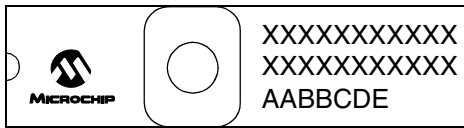
NO GRAPHS OR TABLES AVAILABLE AT THIS TIME

NOTES:

16.0 PACKAGING INFORMATION

16.1 Package Marking Information

28-Lead Side Brazed Skinny Windowed



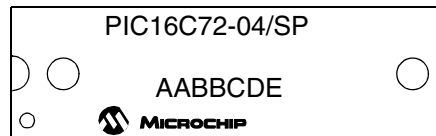
Example



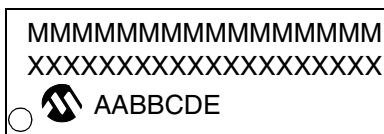
28-Lead PDIP (Skinny DIP)



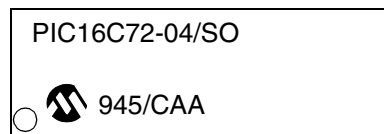
Example



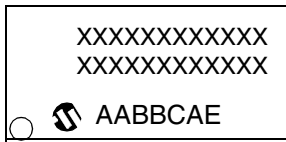
28-Lead SOIC



Example



28-Lead SSOP



Example



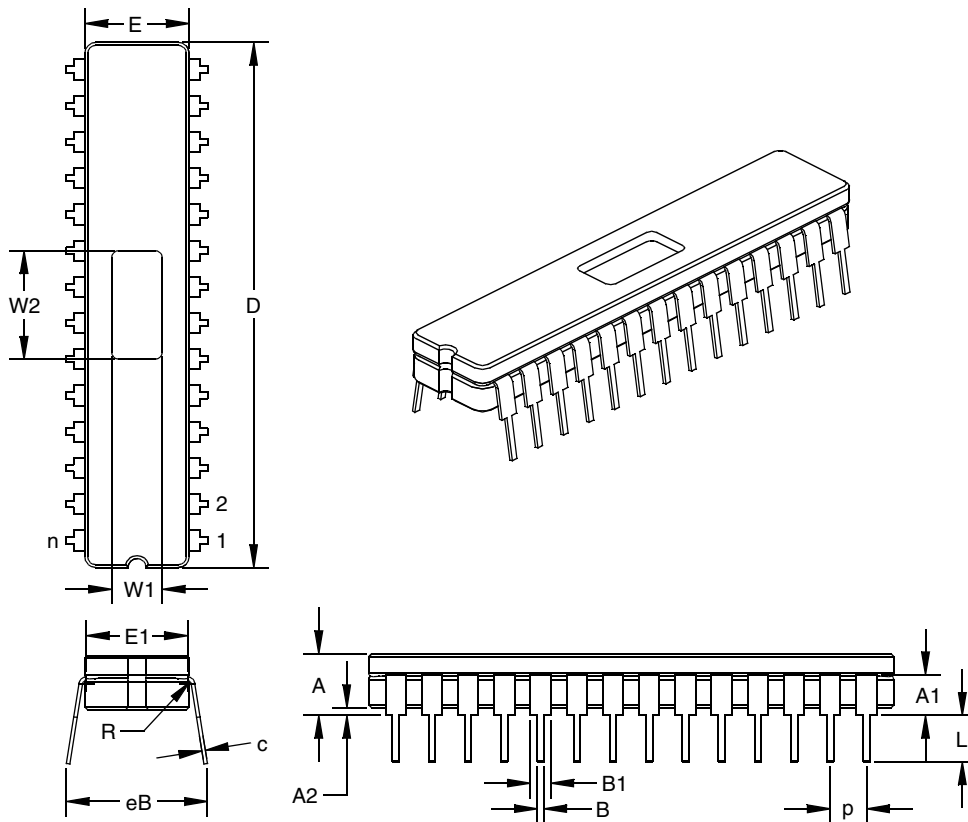
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC16C72 Series

16.2 28-Lead Ceramic Side Brazed Dual In-Line with Window (300 mil)(JW)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

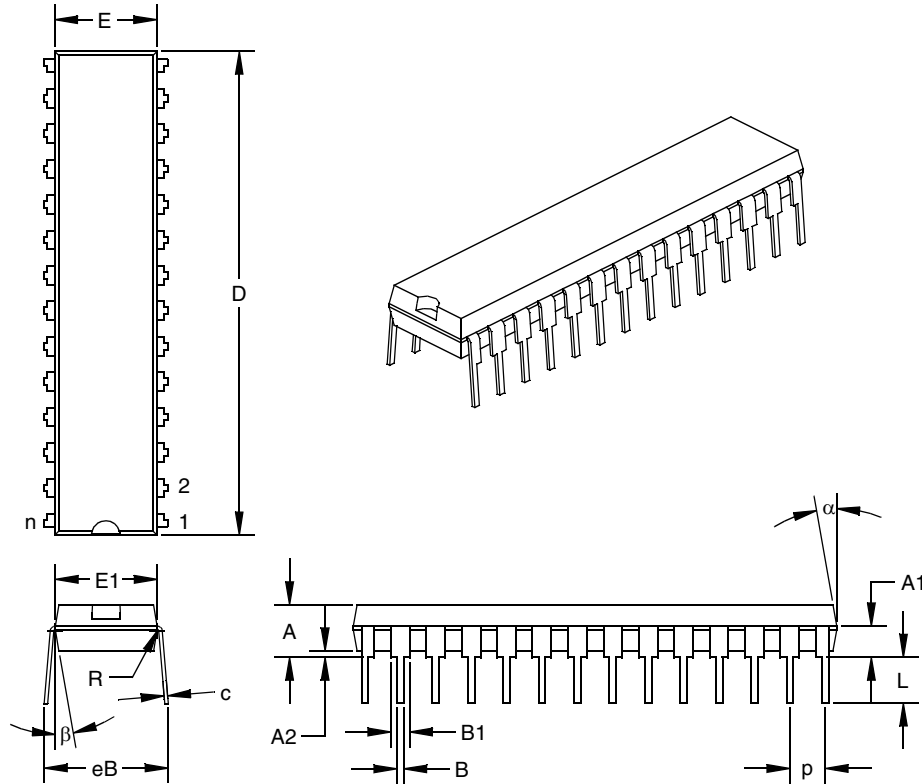


| Units | | INCHES* | | | MILLIMETERS | | |
|------------------------------|----|---------|-------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Dimension Limits | | | 0.300 | | | 7.62 | |
| PCB Row Spacing | | | | | | | |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | 0.098 | 0.100 | 0.102 | 2.49 | 2.54 | 2.59 |
| Lower Lead Width | B | 0.016 | 0.019 | 0.021 | 0.41 | 0.47 | 0.53 |
| Upper Lead Width | B1 | 0.050 | 0.058 | 0.065 | 1.27 | 1.46 | 1.65 |
| Shoulder Radius | R | 0.010 | 0.013 | 0.015 | 0.25 | 0.32 | 0.38 |
| Lead Thickness | c | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| Top to Seating Plane | A | 0.170 | 0.183 | 0.195 | 4.32 | 4.64 | 4.95 |
| Top of Lead to Seating Plane | A1 | 0.107 | 0.125 | 0.143 | 2.72 | 3.18 | 3.63 |
| Base to Seating Plane | A2 | 0.015 | 0.023 | 0.030 | 0.00 | 0.57 | 0.76 |
| Tip to Seating Plane | L | 0.135 | 0.140 | 0.145 | 3.43 | 3.56 | 3.68 |
| Package Length | D | 1.430 | 1.458 | 1.485 | 36.32 | 37.02 | 37.72 |
| Package Width | E | 0.285 | 0.290 | 0.295 | 7.24 | 7.37 | 7.49 |
| Radius to Radius Width | E1 | 0.255 | 0.270 | 0.285 | 6.48 | 6.86 | 7.24 |
| Overall Row Spacing | eB | 0.345 | 0.385 | 0.425 | 8.76 | 9.78 | 10.80 |
| Window Width | W1 | 0.130 | 0.140 | 0.150 | 0.13 | 0.14 | 0.15 |
| Window Length | W2 | 0.290 | 0.300 | 0.310 | 0.29 | 0.3 | 0.31 |

* Controlling Parameter.

16.3 28-Lead Plastic Dual In-line (300 mil) (SP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES* | | | MILLIMETERS | | |
|------------------------------|-----------------|---------|-------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Dimension Limits | | | 0.300 | | | 7.62 | |
| PCB Row Spacing | | | | | | | |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | 0.100 | | | 2.54 | |
| Lower Lead Width | B | 0.016 | 0.019 | 0.022 | 0.41 | 0.48 | 0.56 |
| Upper Lead Width | B1 [†] | 0.040 | 0.053 | 0.065 | 1.02 | 1.33 | 1.65 |
| Shoulder Radius | R | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Lead Thickness | c | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| Top to Seating Plane | A | 0.140 | 0.150 | 0.160 | 3.56 | 3.81 | 4.06 |
| Top of Lead to Seating Plane | A1 | 0.070 | 0.090 | 0.110 | 1.78 | 2.29 | 2.79 |
| Base to Seating Plane | A2 | 0.015 | 0.020 | 0.025 | 0.38 | 0.51 | 0.64 |
| Tip to Seating Plane | L | 0.125 | 0.130 | 0.135 | 3.18 | 3.30 | 3.43 |
| Package Length | D [‡] | 1.345 | 1.365 | 1.385 | 34.16 | 34.67 | 35.18 |
| Molded Package Width | E [‡] | 0.280 | 0.288 | 0.295 | 7.11 | 7.30 | 7.49 |
| Radius to Radius Width | E1 | 0.270 | 0.283 | 0.295 | 6.86 | 7.18 | 7.49 |
| Overall Row Spacing | eB | 0.320 | 0.350 | 0.380 | 8.13 | 8.89 | 9.65 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter.

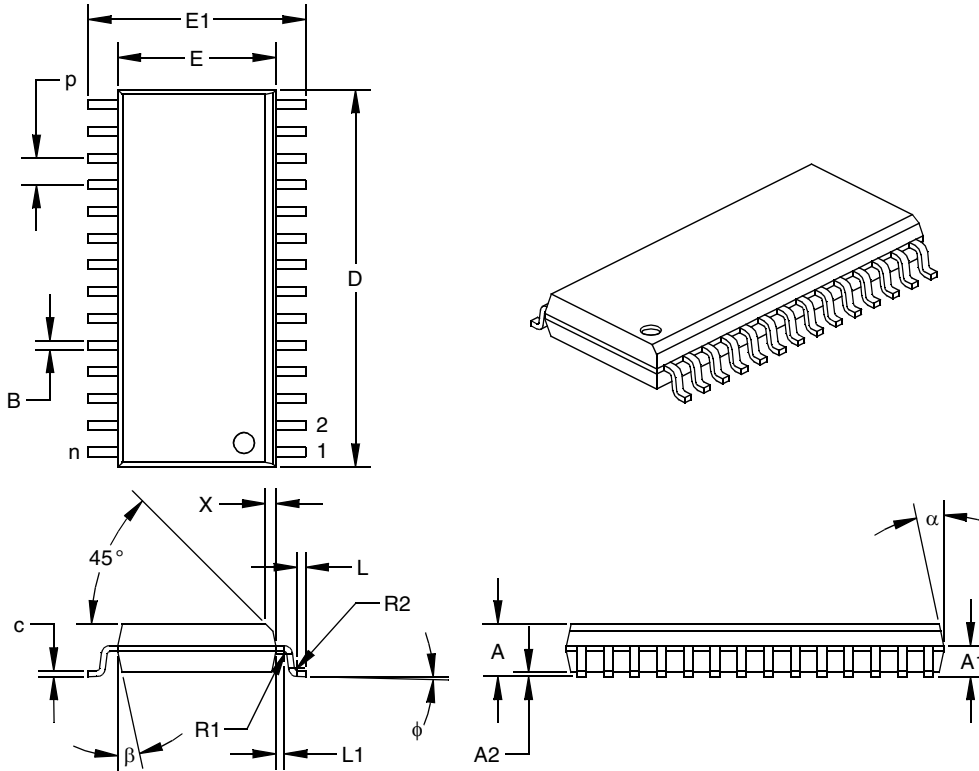
[†] Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16C72 Series

16.4 28-Lead Plastic Surface Mount (SOIC - Wide, 300 mil Body) (SO)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES* | | | MILLIMETERS | | |
|-------------------------|----------------|---------|-------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Dimension Limits | | | | | | | |
| Pitch | p | | 0.050 | | | 1.27 | |
| Number of Pins | n | | 28 | | | 28 | |
| Overall Pack. Height | A | 0.093 | 0.099 | 0.104 | 2.36 | 2.50 | 2.64 |
| Shoulder Height | A1 | 0.048 | 0.058 | 0.068 | 1.22 | 1.47 | 1.73 |
| Standoff | A2 | 0.004 | 0.008 | 0.011 | 0.10 | 0.19 | 0.28 |
| Molded Package Length | D [†] | 0.700 | 0.706 | 0.712 | 17.78 | 17.93 | 18.08 |
| Molded Package Width | E [†] | 0.292 | 0.296 | 0.299 | 7.42 | 7.51 | 7.59 |
| Outside Dimension | E1 | 0.394 | 0.407 | 0.419 | 10.01 | 10.33 | 10.64 |
| Chamfer Distance | X | 0.010 | 0.020 | 0.029 | 0.25 | 0.50 | 0.74 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.011 | 0.016 | 0.021 | 0.28 | 0.41 | 0.53 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.010 | 0.015 | 0.020 | 0.25 | 0.38 | 0.51 |
| Lead Thickness | c | 0.009 | 0.011 | 0.012 | 0.23 | 0.27 | 0.30 |
| Lower Lead Width | B [†] | 0.014 | 0.017 | 0.019 | 0.36 | 0.42 | 0.48 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

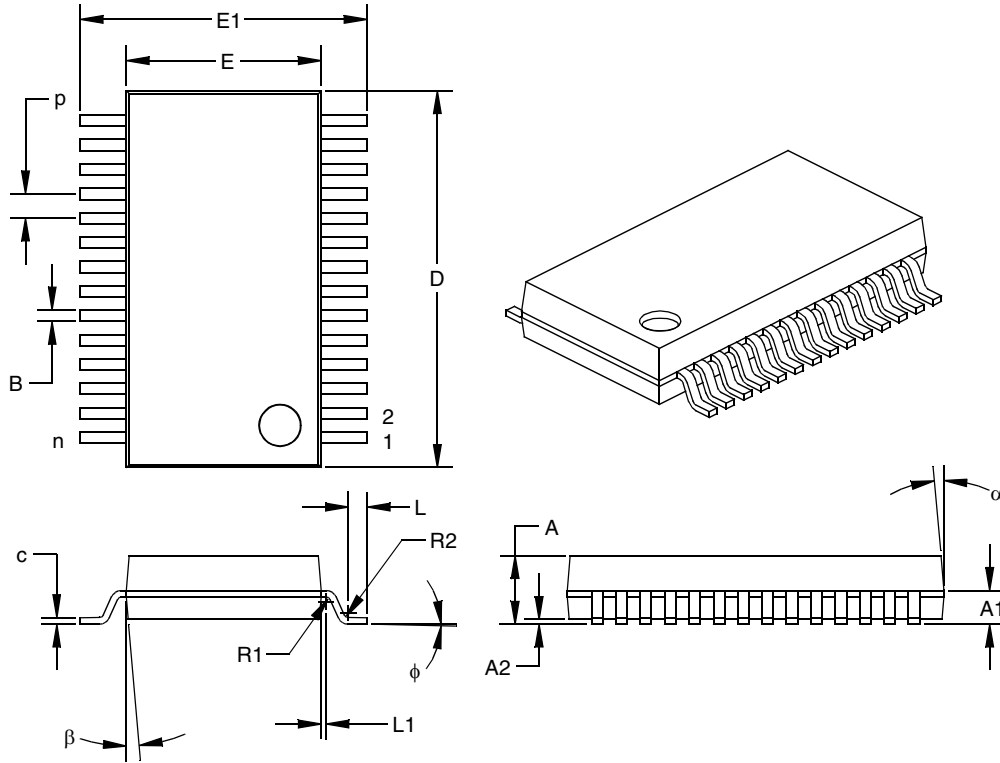
* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

16.5 28-Lead Plastic Surface Mount (SSOP - 209 mil Body 5.30 mm) (SS)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES | | | MILLIMETERS* | | |
|-------------------------|----------------|--------|-------|-------|--------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Dimension Limits | | | | | | | |
| Pitch | p | | 0.026 | | | 0.65 | |
| Number of Pins | n | | 28 | | | 28 | |
| Overall Pack. Height | A | 0.068 | 0.073 | 0.078 | 1.73 | 1.86 | 1.99 |
| Shoulder Height | A1 | 0.026 | 0.036 | 0.046 | 0.66 | 0.91 | 1.17 |
| Standoff | A2 | 0.002 | 0.005 | 0.008 | 0.05 | 0.13 | 0.21 |
| Molded Package Length | D [‡] | 0.396 | 0.402 | 0.407 | 10.07 | 10.20 | 10.33 |
| Molded Package Width | E [‡] | 0.205 | 0.208 | 0.212 | 5.20 | 5.29 | 5.38 |
| Outside Dimension | E1 | 0.301 | 0.306 | 0.311 | 7.65 | 7.78 | 7.90 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.015 | 0.020 | 0.025 | 0.38 | 0.51 | 0.64 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Lead Thickness | c | 0.005 | 0.007 | 0.009 | 0.13 | 0.18 | 0.22 |
| Lower Lead Width | B [†] | 0.010 | 0.012 | 0.015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16C72 Series

NOTES:

APPENDIX A: WHAT'S NEW IN THIS DATA SHEET

This is a new data sheet. However, information on the PIC16C72 device was previously found in the PIC16C7X Data Sheet, DS30390. Information on the PIC16CR72 device is new.

APPENDIX B: WHAT'S CHANGED IN THIS DATA SHEET

Revision A (1998)

New data sheet.

Revision B (January 2013)

Added a note to each package outline drawing.

APPENDIX C: DEVICE DIFFERENCES

A table of the differences between the devices described in this document is found below.

| Difference | PIC16C72 | PIC16CR72 |
|------------------------|-----------|-----------|
| SSP module in SPI mode | Basic SSP | SSP |

PIC16C72 Series

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|-------------------|--|-------------------|------------|------------|
| Device | Frequency Range | Temperature Range | Package | Pattern |
| Device | PIC16C72 ⁽¹⁾ , PIC16C72T ⁽²⁾ PIC16LC72 ⁽¹⁾ , PIC16LC72T ⁽²⁾ PIC16CR72 ⁽¹⁾ , PIC16CR72T ⁽²⁾ PIC16LCR72 ⁽¹⁾ , PIC16LCR72T ⁽²⁾ | | | |
| Frequency Range | 02 = 2 MHz 04 = 4 MHz 10 = 10 MHz 20 = 20 MHz | | | |
| Temperature Range | b ⁽³⁾ = 0°C to 70°C (Commercial) I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) | | | |
| Package | JW = Ceramic Dual In-Line Package with Window SO = Small Outline - 300 mil SP = Skinny PDIP SS = Shrink Small Outline Package - 209 mil | | | |
| Pattern | 3-digit Pattern Code for QTP, ROM (blank otherwise) | | | |

Examples:

a) PIC16C72 -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal V_{DD} limits, QTP pattern #301.

b) PIC16LC72 - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended V_{DD} limits.

c) PIC16CR72 - 10I/P = ROM program memory, Industrial temp., PDIP package, 10MHz, normal V_{DD} limits.

Note 1: C= CMOS
CR= CMOS ROM
LC= Low Power CMOS
LCR= ROM Version, Extended V_{DD} range

2: T = in tape and reel - SOIC, SSOP packages only.

3: b = blank

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