

1. DESCRIPTION

The XD/XL485 is a +5V, half-duplex, $\pm 15\text{KV}$ ESD protected high speed RS485 transceiver circuit. The circuit contains one driver and one receiver. A transmission rate of 10Mbps can be realized.

The XD/XL485 is a half-duplex type with drive enable (DE) and receive enable (RE) pins, and the drive and receive outputs are high-resistance when off.

The XD/XL485 has a fail-safe circuit to ensure correct receiver output when the receiver input is open or shorted.

The XD/XL485 receiver input impedance is 1/8 unit load, allowing up to 256 transceivers to be hooked up to the bus.

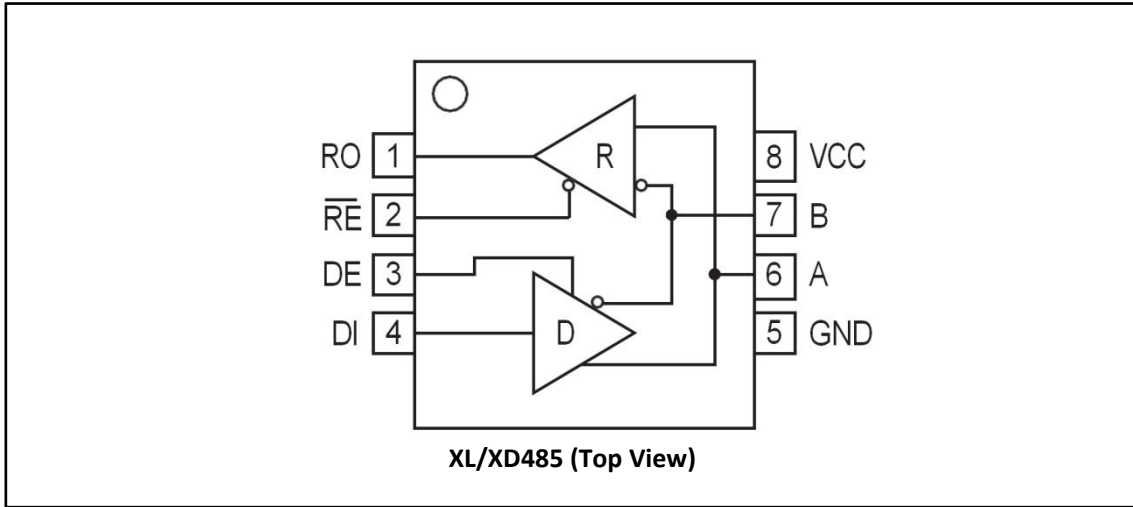
2. FEATURES

- Electro-Static Discharge (ESD): A/B $\pm 15\text{KV}$ - Human Body Mode (HBM)
- Bus allows up to 256 transceivers to be hooked up
- Maximum data speed 10 Mbps
- Tri-state outputs
- SOP8(XL485CS), MSOP8(XL485 - SS), DIP8(XD485)

3. APPLICATION

- Industrial Controls
- Industrial Motor Drives
- Automatic HVAC systems
- RS485/RS422 Interface

4. PIN CONFIGURATIONS AND FUNCTIONS



Pin Functions

Pin	Name	Description
1	RO	Receive outputs
2	\overline{RE}	Receive Enable: active low, when high, the receive output is high resistance.
3	DE	Transmit Enable: active high, when DE is low, the transmit output is high resistance. When DE is high, the chip works in transmit state, when DE is low, the chip works in receive state.
4	DI	Transmit data input
5	GND	Ground
6	A	Receive Input/Transmit Output
7	B	Receive Input/Transmit Output
8	Vcc	Power supply

5. LOGICAL RELATION

5.1. XD/XL485 Chip Driver Truth Table

INPUT	ENABLE	OUTPUT	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

5.2. XD/XL485 Chip Receiver Truth Table

INPUT			OUTPUT
RE	DE	AXB	RO
L	X	>-50mV	H
L	X	<-200mV	L
L	X	Open circuit	H
L	X	Short circuit	H
H	H	X	Z
H	L	X	Z

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{CC}	Supply voltage range	-	+6.0	V
	Input pin voltage range	-0.5	+6.0	V
	Output pin voltage range	-0.5	+6.0	V
	Input clamp current	-7.0	+12.0	V
	Output clamp current	-7.0	+12.0	V
	Input/output clamp current	-0.3	V _{CC} +0.3	V
	T _{STG}	Continuous output low current	-55	+150
T _{OP}	Continuous output high current	-40	+85	°C
T _{MOP}	Continuous current through GND	-55	+125	°C
	Continuous current through V _{CC}	-	725	mW
Continuous power consumption	Total Power Dissipation	-	470	mW
	Storage temperature range	-55	+150	°C

6.2. DC Characteristics

(Unless otherwise indicated, $V_{CC}=5V\pm 10\%$, $T_A=25^\circ C\pm 10\%$) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Operating voltage range	V_{CC}			4.5		5.5	V
Driver differential output (no load)	V_{OD1}	-		-	-	5	V
Driver differential output (with load)	V_{OD2}	Figure 1, $R=54\Omega$ or $R=27\Omega$		1.5		-	V
Driver Differential Output Voltage Amplitude of change (Note 2)	ΔV_{OD}			-	-	0.2	V
Driver Common Mode Output Voltage	V_{OC}			1		3	V
Amplitude of change in common mode output voltage of the driver (Note 2)	ΔV_{OC}			-	-	0.2	V
Input High Voltage	V_{IH}	$\overline{DE}, \overline{RE}, DI$		2	-	-	V
Input Low Voltage	V_{IL}	$\overline{DE}, \overline{RE}, DI$		-	-	0.8	V
Input Current	I_{IN1}	DE, RE, DI		-	-	± 2	μA
Input Current (A,B)	I_{IN2}	$DE=0V, V_{CC}=5V$	$V_{IN}=5V$	-	40	90	μA
			$V_{IN}=0V$	-	60	100	
Receiver differential input threshold voltage	V_{TH}	$-7V \leq V_{CM} \leq +12V$		-200	-	-50	mV
Receiver input hysteresis	ΔV_{TH}			-	25	-	mV
Receiver output high	V_{OH}	$I_o=-4mA$		4	-	-	V
Receiver output low	V_{OL}	$I_o=4mA$		-	-	0.4	V
Receiver-side tri-state (high-resistance) output current	I_{OZR}	$0.4V \leq V_o \leq 2.4V$		-	-	1	μA
Receiver Input Impedance	R_{IN}	$-7V \leq V_{CM} \leq +12V$		96	-	-	$k\Omega$
No-load operating current	I_{CC}	No-load, $\overline{RE}=DI=GND$ 或 V_{CC}	$DE=V_{CC}$	-	480	600	μA
			$DE=GND$	-	450	600	μA
Receiver output short-circuit current	I_{OSR}	$0V \leq V_{RO} \leq V_{CC}$		-	-	95	mA
ESD protection		A/B, Body Mode		± 8	± 15	-	kV

Note:

- [1] All currents flowing into the device are positive and currents flowing out of the device are negative; all voltages are referenced to ground if not otherwise noted.
- [2] ΔV_{OD} and ΔV_{OC} are the respective changes in V_{OD} and V_{OC} when the DI input state is changed.

6.3. Switching Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drive Input to Output	tDPLH	Figure 3 and Figure 5 RDIFF=50Ω CL1=CL2=100pF	-	34	60	nS
	tDPHL		-	34	60	nS
Driver Output Offset tDPLH – tDPHL	tDSKEW		-	-2.5	±10	nS
Drive Rise and Fall Time	tDR		-	10	25	nS
	tDF		-	10	25	nS
Driver enable to output high	tDZH		Figure 4 and Figure 6, CL=100pF S2 close	-	-	150
Driver enable to output low	tDZL	Figure 4 and Figure 6, CL=100pF S1 close	-	-	150	nS
Drive from low to off	tDLZ	Figure 4 and Figure 6, CL=15pF S1 close	-	-	100	nS
Drive from high to off	tDHZ	Figure 4 and Figure 6, CL=15pF S2 close	-	-	100	nS
Receiver input to output	tRPLH	Figure 7 and Figure 9, VID ≥ 2.0V; VID Rise and fall time ≤15nS	-	-	150	nS
	tRPHL		-	-	150	nS
Differential Receiver Offset tRPLH - tRPHL	tRSKEW		-	0	±10	nS
Receiver enable to output low	tRZL	Figure 2 and Figure 8 CL=100pF S1 close	-	20	50	nS
Receiver enable to output high	tRZH	Figure 2 and Figure 8 CL=100pF S2 close	-	20	50	nS
Receiver low to off	tRLZ	Figure 2 和 Figure 8 CL=100pF S1 close	-	20	50	nS
Receiver high to off	tRHZ	Figure 2 和 Figure 8 CL=100pF S2 close	-	20	50	nS
Driver output short-circuit current	I _{OD}	Short-circuit current between A/B	-	-	100	mA
Maximum data speed	f _{MAX}		10	-	-	Mbps

6.4. Test line and switch waveforms

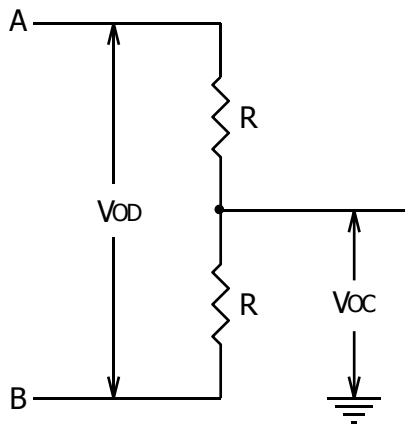


Figure 1: Driver DC Characteristics Test Load

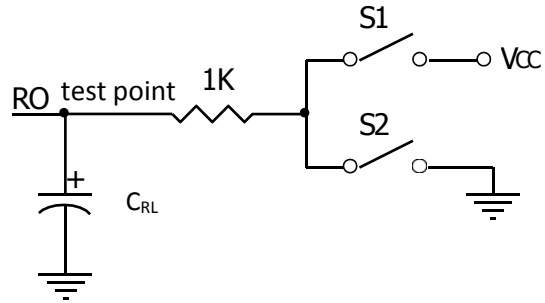


Figure 2: Receiver Enable/Off Switching Characteristics Test Load

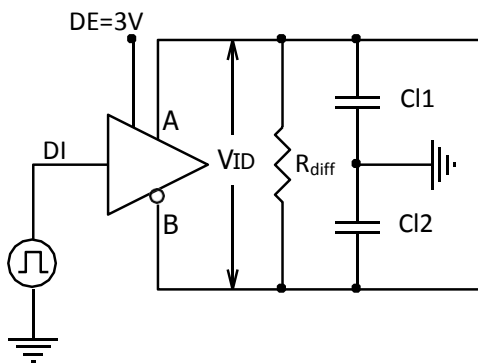


Figure 3: Driver Switching Characteristics Test Load

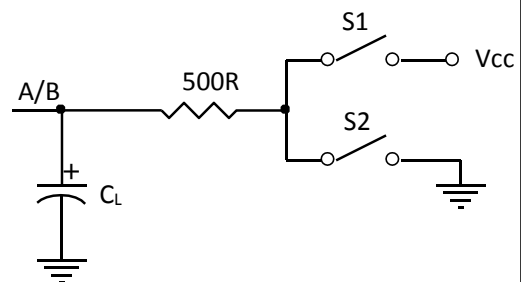


Figure 4: Driver Enable/Off Switching Characteristics Test Load

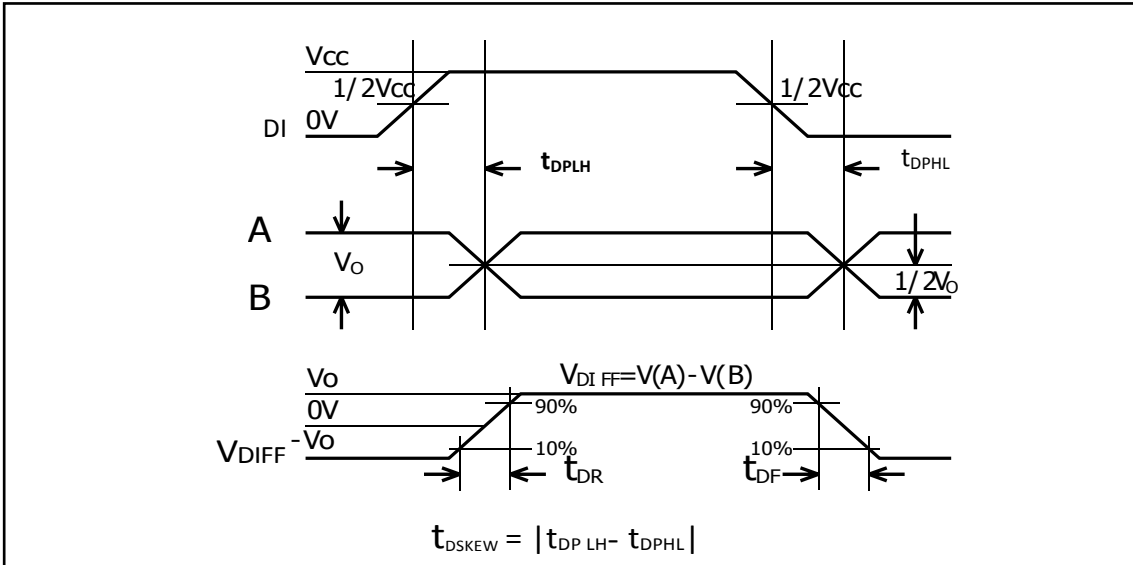


Figure 5: Drive Transfer Delay

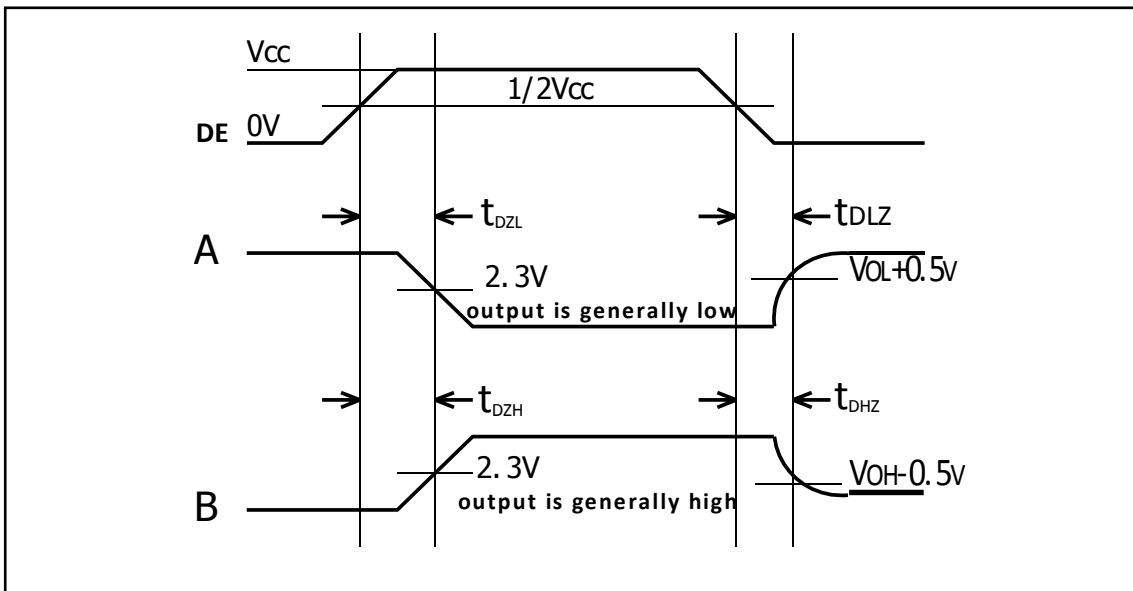


Figure 6: Driver Enable/Off Timing

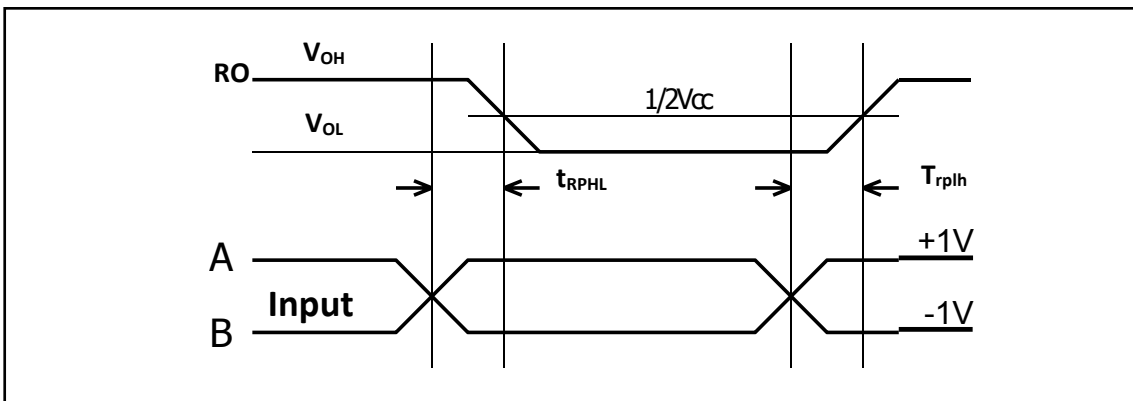


Figure 7: Receiver Transmission Delay

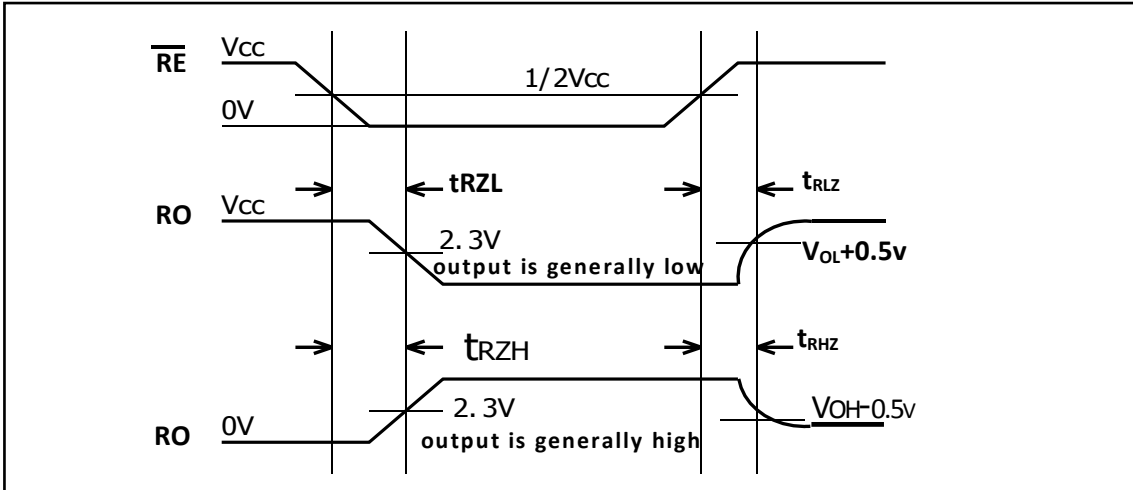


Figure 8: Receiver Enable/Off Timing

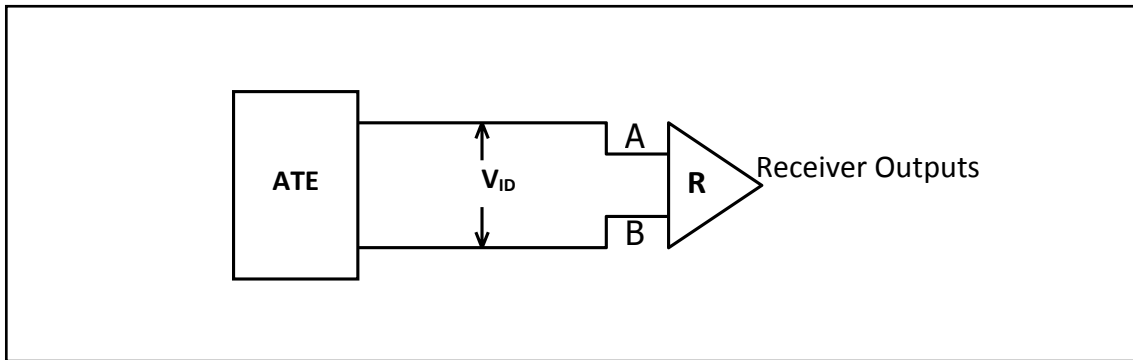


Figure 9: Receiver Transmission Delay Test Circuitry

6.5. Typical Application Diagram

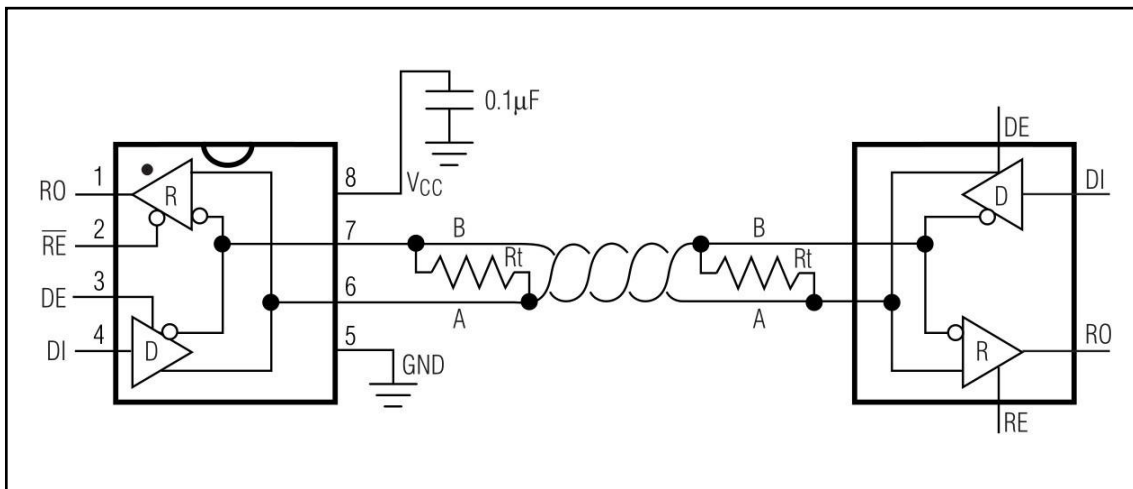


Figure 10: Typical Half-Duplex Operation Circuit for XD/XL485

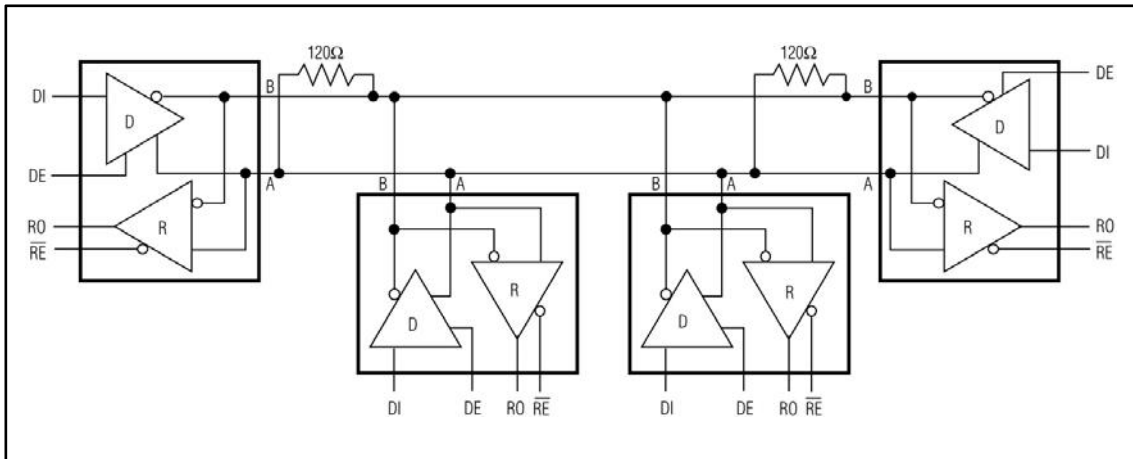


Figure 11: Typical half-duplex XD/XL485 operating network

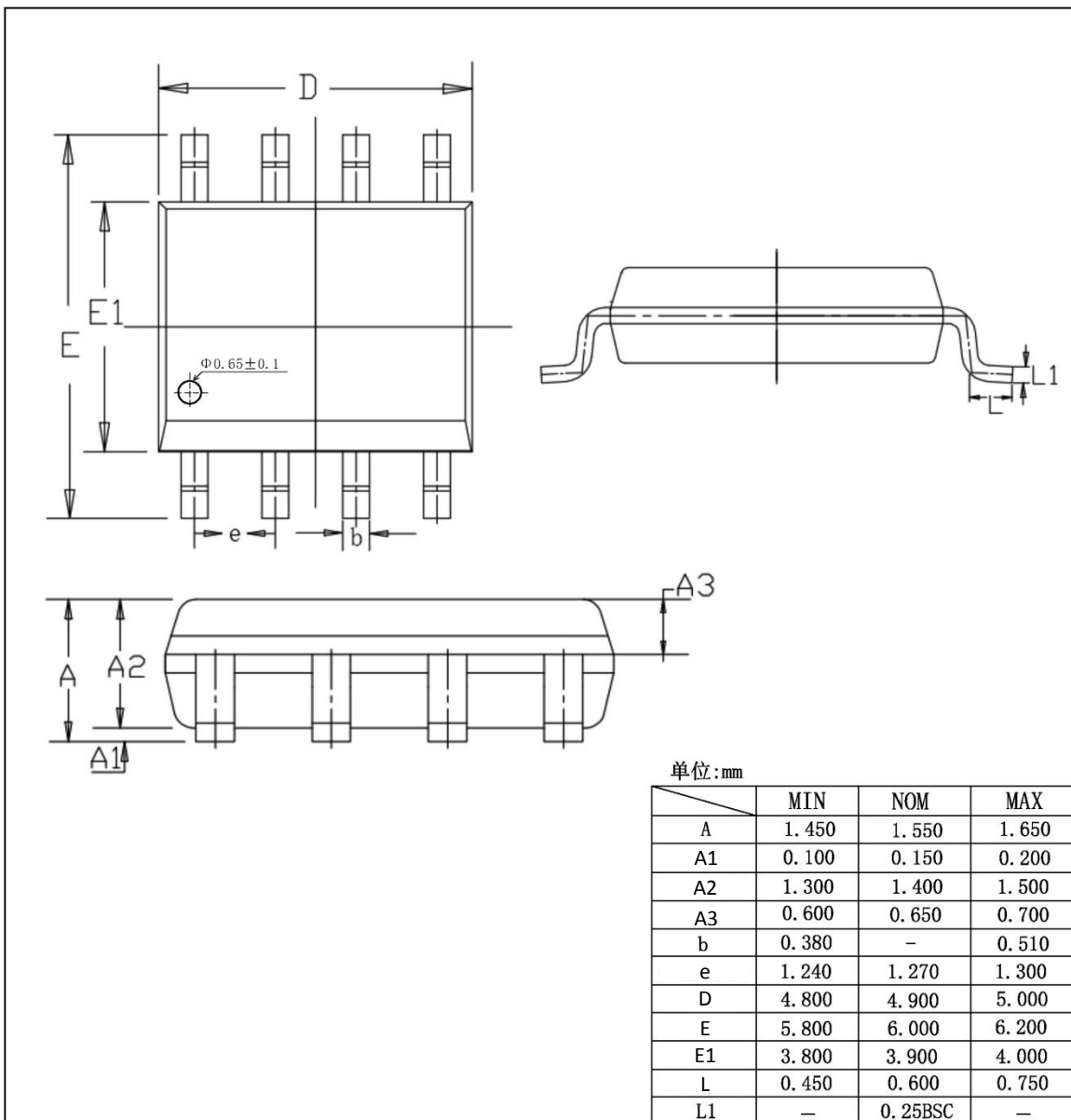
7. ORDERING INFORMATION

Ordering Information

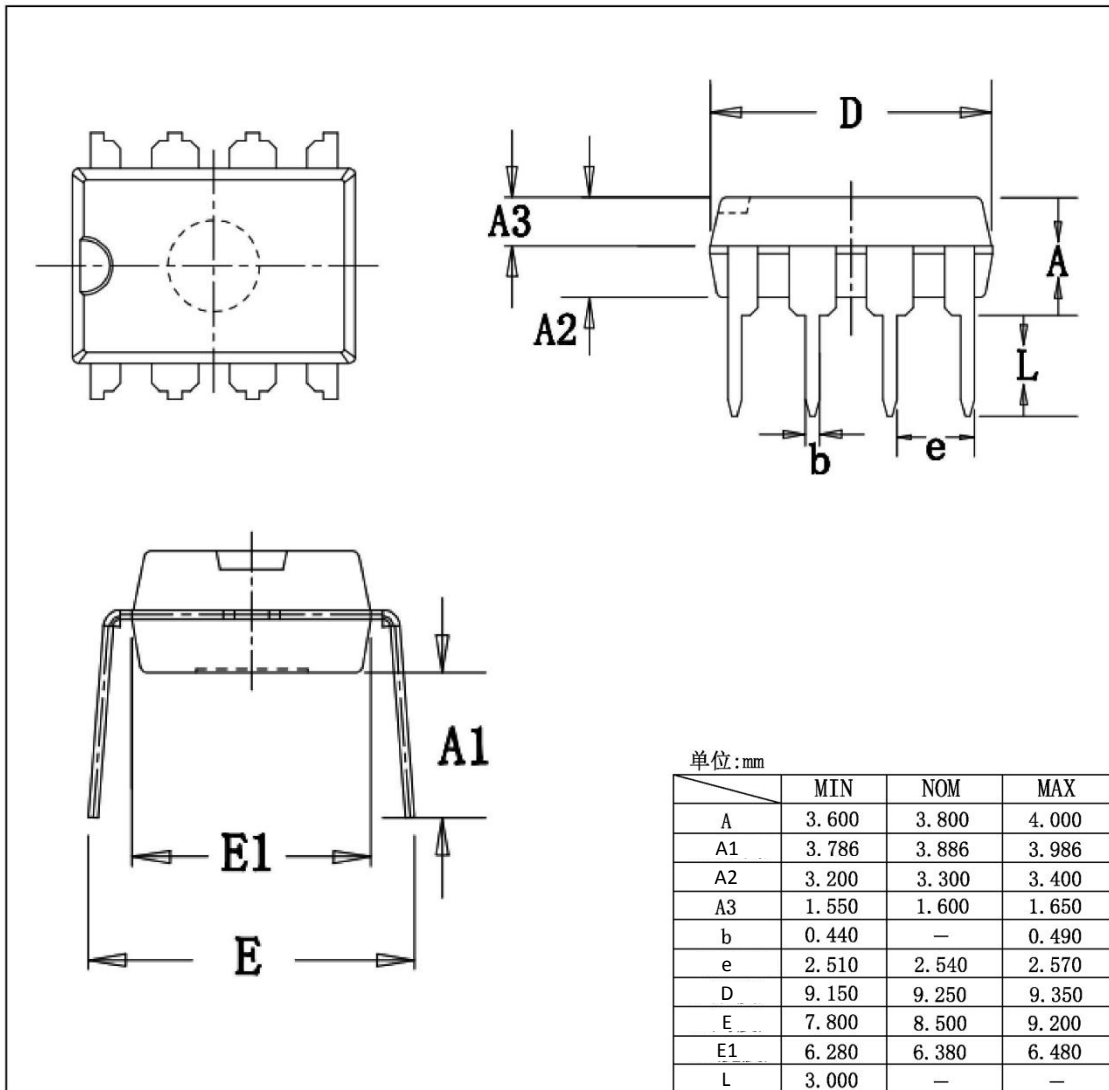
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL485CS	XL485CS	SOP8	4.90 * 3.90	-40 to +85	MSL3	T&R	2500
XL485 - SS	XL485 - SS	MSOP8	3.00 * 3.00	-40 to +85	MSL3	T&R	2500
XD485	XD485	DIP8	9.25 * 6.38	-40 to +85	MSL3	Tube 50	2000

8. DIMENSIONAL DRAWINGS

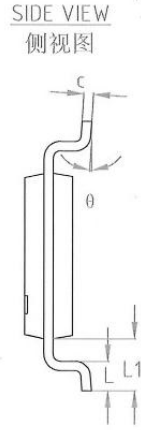
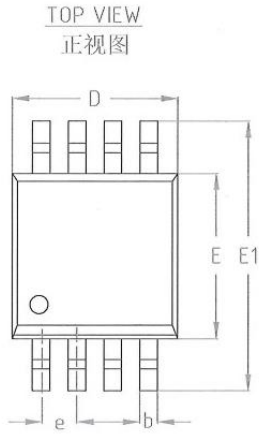
SOP8



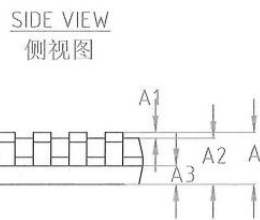
DIP8



MSOP8



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	-	0.36
c	0.15	-	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65 BSC		
L1	0.95 REF		
L	0.40	-	0.70
θ	0°	-	8°



The above information is for reference only, if you need help contact customer service staff. Thank you XINLUDA