36V, 1.5A Monolithic Step-Down Switching Regulator

1 Features

- 1.5A continuous output current capability
- 4.5V to 36V wide operating input range with 33V input Over Voltage Protection
- Integrated 36V, 250mΩ high side and 36V, 140mΩ low side power MOSFET switches
- Up to 97% efficiency
- Internal Soft-Start limits the inrush current at turn-on
- Internal compensation to save external components
- Input Under-Voltage Lockout
- Input over-voltage protection to protect device from working in high voltage and high current condition
- Output Over-Voltage Protection
- Output short protection with both high side current limit and low side current limit to protect the device in hard short
- Over-Temperature Protection
- Pulse skip mode at light load to improve light load efficiency
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 150KHz Switching Frequency
- Fewest external components and intensive internal protection features
- ESOP8 Package

2 Applications

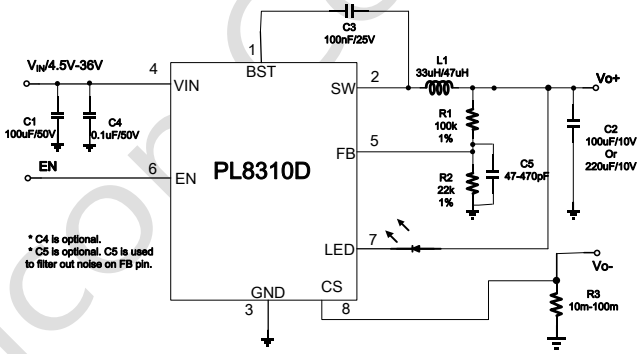
- USB car charger
- Portable charging device
- General purpose DC-DC conversion

3 Description

PL8310D is a monolithic 36V, 1.5A step-down switching regulator. PL8310D integrates a 36V 250mΩ high side and a 36V, 140mΩ low side MOSFETs to provide 1.5A continuous load current over a 4.5V to 36V wide operating input voltage with 33V input over voltage protection. Peak current mode control provides fast transient responses and cycle-by-cycle current limiting.

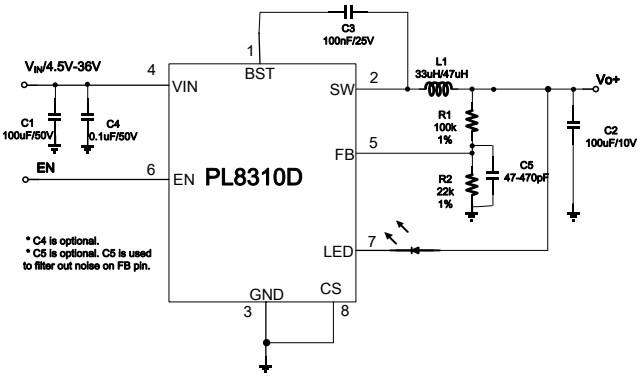
PL8310D has configurable line drop compensation, configurable charging current limit. CC/CV mode control provides a smooth transition between constant current charging and constant voltage charging stages. Built-in soft-start prevents inrush current at power-up.

4 Typical Application Schematic



Work Mode 1: CS to GND with sensing resistor

Fig. 1 Schematic



Work Mode2: CS to GND

Fig. 2 Schematic

5 Pin Configuration and Functions

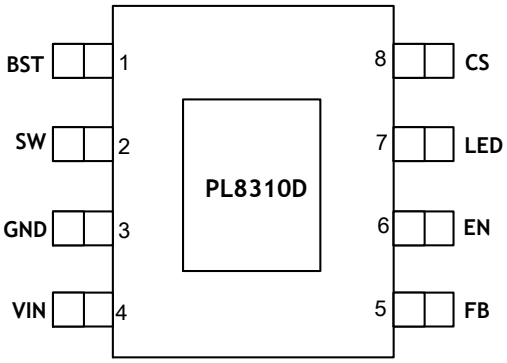


Fig3. PL8310D ESOP-8 Package

PL8310D Pin-Functions (SOP-8 Package)

Pin		Description
8310D	Name	
1	BST	Boot-Strap pin. Connect a 0.1μF or greater capacitor between SW and BST to power the high side gate driver.
2	SW	Power Switching pin. Connect this pin to the switching node of inductor.
3	GND	Ground
4	VIN	Power Input. Vin supplies the power to the IC. Supply Vin with a 4.5V to 36V power source. Bypass Vin to GND with a large capacitor and at least another 0.1uF ceramic capacitor to eliminate noise on the input to the IC. Put the capacitors close to Vin and GND pins.
5	FB	Feedback Input. FB senses the output voltage. Connect FB with a resistor divider connected between the output and ground. FB is a sensitive node. Keep FB away from SW and BST pin. When CS pin is floating or connected to output, connect FB directly to output since internal resistor divider is used to set output voltage.
6	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. EN pin is pulled to VIN internally by a larger resistor. EN threshold is set to 1.1V without hysteresis.
7	LED	LED input. Connect the negative terminal of a LED to indicate output status.
8	CS	Current sense input. Connect a 10mΩ to 100mΩ resistor between this pin and GND to program current limit. CS pin is also used to set the work mode as following: Work Mode 1: When CS pin is connected to GND through a current sense resistor, CC loop will be enabled. The current limit will be set by the sensing resistor. R1 in Fig. 1 can also be used to program line drop compensation. Work Mode 2: When CS pin is connected to GND, The output voltage is set with a resistor divider from the output node to the FB pin. 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R_1 is the upper resistor, R_2 is the lower resistor)
EPAD		EPAD is connected to AGND internally. EPAD must be connected in PL8310D

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL8310D	**PL8310DIES08**	**ESOP-8**	**4000**	**8310D RAAYMD**

PL8310D: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	-0.3	36	V
	V_{EN} to GND	-0.3	6	
	V_{CS} to GND	-0.3	6	
	V_{FB} to GND	-0.3	6	
Output Voltages	V_{LED} to GND	-0.3	6	V
	V_{BST} to V_{SW}	-0.3	6	
	V_{SW} to GND	-1	V_{IN}+ 0.3	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+160	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2	4	kV
	CDM Charger device model		500	V

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	V_{IN} to GND	6.5	30	V
	FB	-0.3	3.3	V
Output Voltages	V_{OUT}	0.5	V_{IN}*D_{max}	V
Output Current	I_{OUT}	0	1.5	A
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information (Note 3)

Symbol	Description	ESOP-8	Unit
θ_{JA}	Junction to ambient thermal resistance	56	°C/W
θ_{JC}	Junction to case thermal resistance	45	

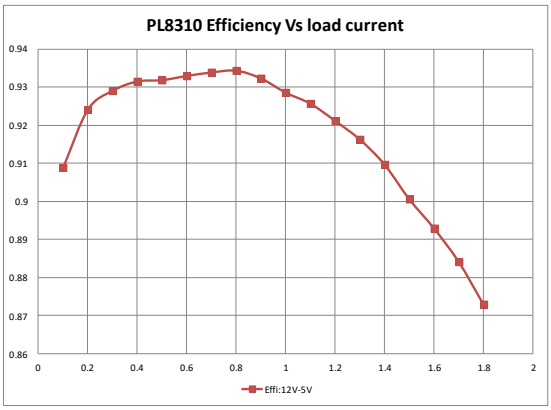
Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics (Typical at Vin = 12V, T_J=25°C, unless otherwise noted.)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
BUCK CONVERTER						
MOSFET						
I_{leak_sw}	High-Side Switch Leakage Current	V_{EN} = 0V, V_{SW}= 0V		0	10	μA
$R_{DS(ON)\_H}$	High-Side Switch On-Resistance	I_{OUT} = 1.5A, V_{OUT} = 3.3V		250		mΩ
$R_{DS(ON)\_L}$	Low-Side Switch On-Resistance	I_{OUT} = 1.5A, V_{OUT} = 3.3V		140		mΩ
SUPPLY VOLTAGE (VIN)						
V_{UVLO_up}	Minimum input voltage for startup				4.4	V
V_{UVLO_down}				4.3		V
V_{UVLO_hys}				0.3		
$I_{Q\text{-}NONSW}$	Operating quiescent current	V_{FB} =1.2V		1		mA
CONTROL LOOP						
F_{oscb}	Buck oscillator frequency			150		kHz
V_{FB}	Feedback Voltage	6.5V ≤ VIN ≤ 33V		0.9		V
V_{FB_OVP}	Feedback Over-voltage Threshold			1.1* V_{FB}		V
D_{max}	Maximum Duty Cycle(Note 4)			98		%
T_{on}	Minimum On Time(Note 4)			100		ns
PROTECTION						
I_{ocl_hs}	Upper Switch Current Limit	Minimum Duty Cycle		3.5		A
I_{ocl_ls}	Lower Switch Current Limit	From Drain to Source		1.2		A
V_{inovp}	Input Over voltage protection			33		V
Th_{sd}	Thermal Shutdown(Note 4)			155		°C
Th_{sdhys}	Thermal Shutdown Hysteresis(Note 4)			15		°C

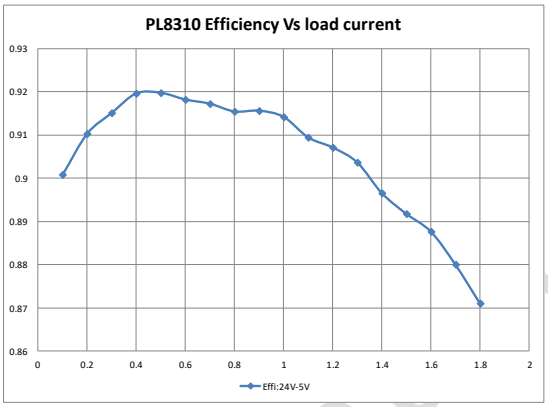
Note:
4) Guaranteed by design, not tested in production.

8 Typical Characteristics



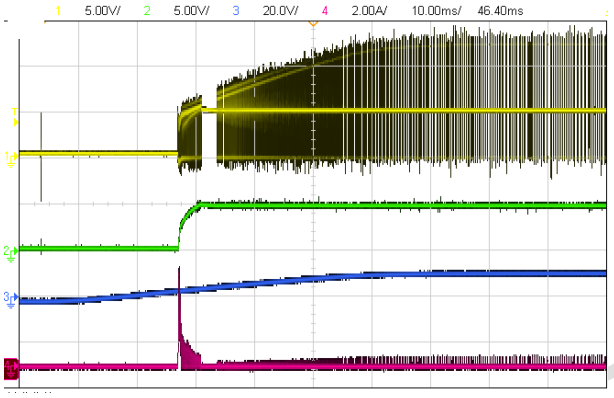
Vin = 12V, Vout = 5V

Fig. 4 Efficiency



Vin =24V, Vout = 5V

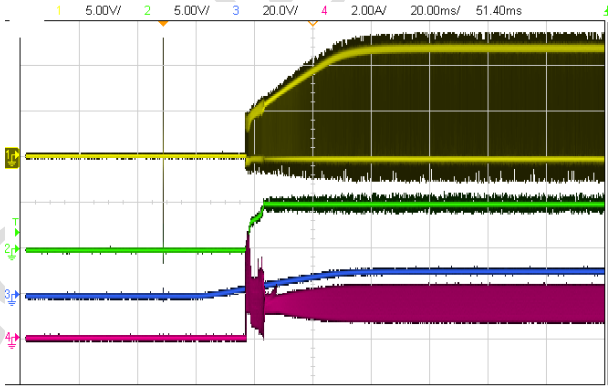
Fig. 5 Efficiency



Vin = 12V, Vo = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

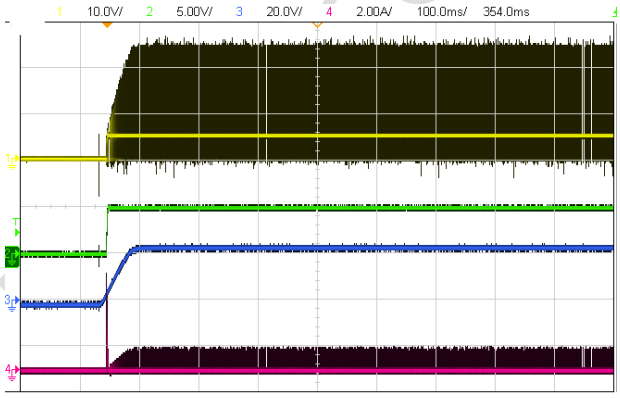
Fig. 6 Startup waveform, Iout = 0A



Vin = 12V, Vo = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

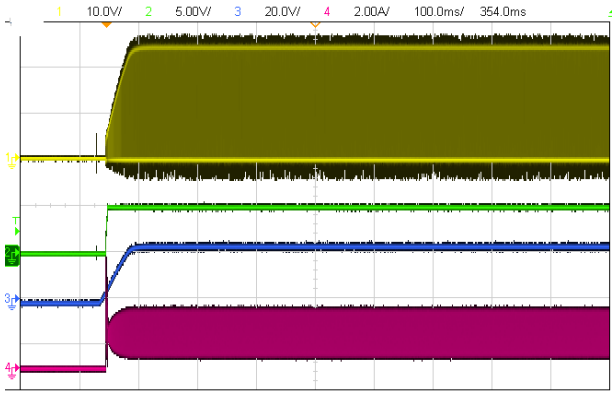
Fig. 7 Startup waveform, Iout = 1.5A



Vin = 24V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

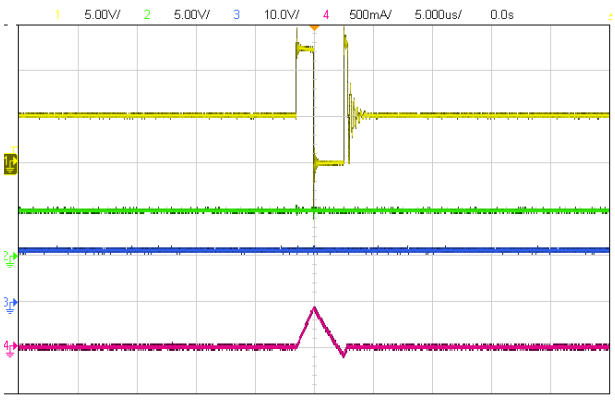
Fig. 8 Startup waveform, Iout = 0A



Vin = 24V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

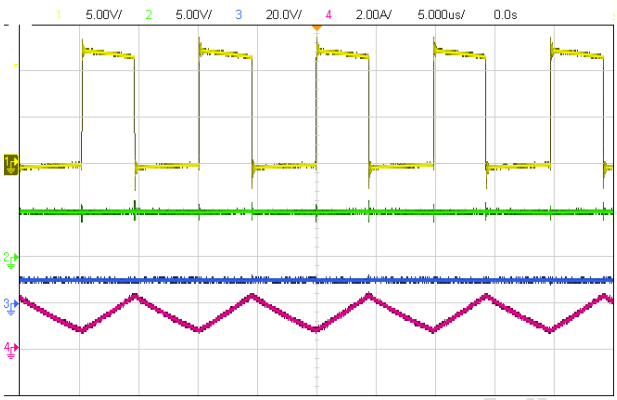
Fig. 9 Startup waveform, Iout = 1.5A



Vin = 12V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

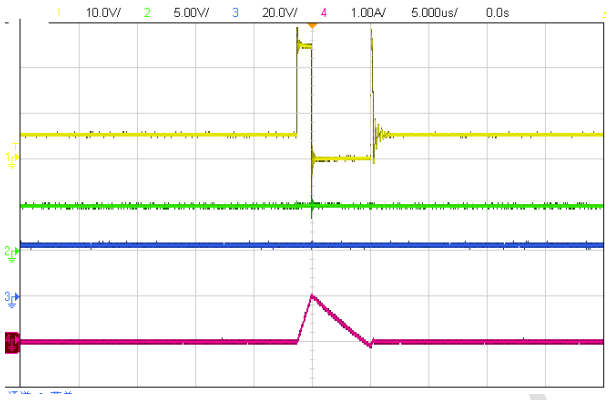
Fig. 10 Steady state waveform, Iout = 0A



Vin = 12V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

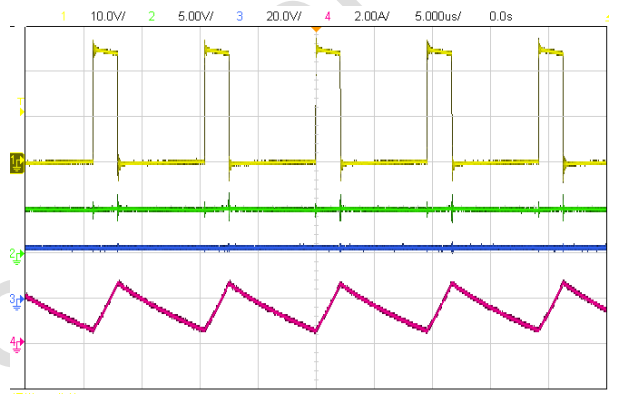
Fig. 11 Steady state waveform, Iout = 1.5A



Vin = 24V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

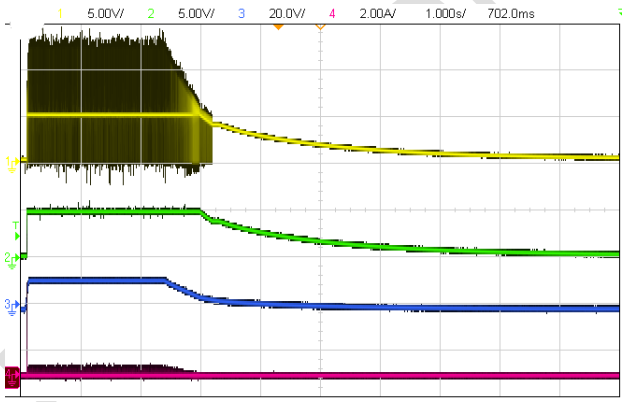
Fig. 12 Steady state waveform, Iout = 0A



Vin = 24V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

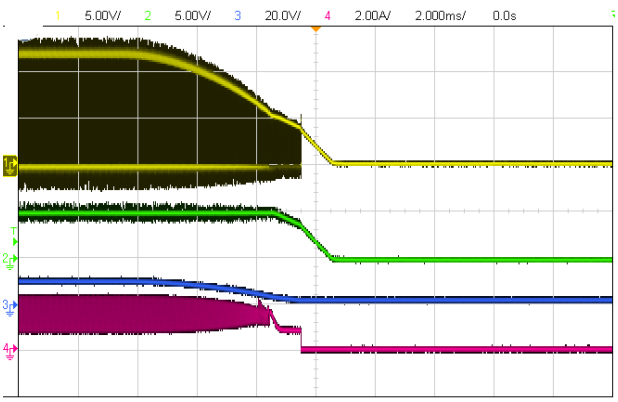
Fig. 13 Steady state waveform, Iout = 1.5A



Vin = 12V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

Fig. 14 Shutdown waveform, Iout = 0A



Vin = 12V, Vout = 5V

Ch1: SW Ch2:VOUT Ch3: VIN Ch4:IL

Fig. 15 Shutdown waveform, Iout = 1.5A

9 Detailed Description

9.1 Overview

PL8310D is an easy to use synchronous step-down DC-DC converter that operates from 4.5V to 36V supply voltage. It is capable of delivering up to 1.5A continuous load current with high efficiency and thermal performance in a very small solution size.

PL8310D also integrates input over voltage and output over voltage protection. This feature helps customers to design a safe DC-DC converter easily.

The switching frequency is fixed at 150 kHz switching frequency to minimize inductor size and improve EMI performance.

9.2 Functional Block Diagram

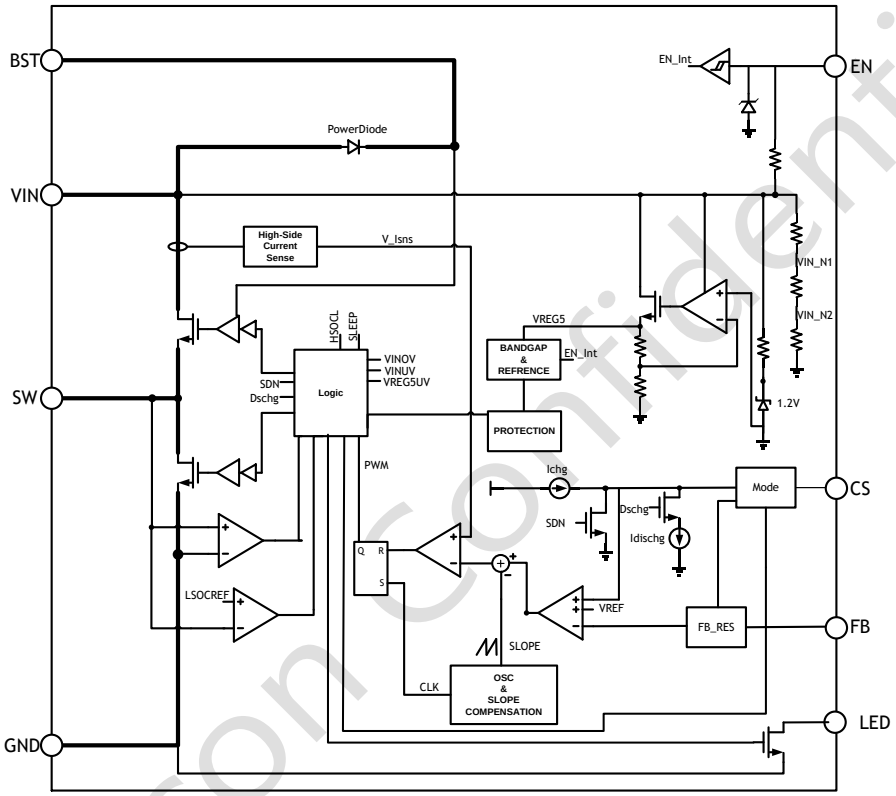


Fig.16 PL8310D Diagram

9.3 Peak Current Mode Control

PL8310D employs a fixed 150 kHz frequency peak current mode control. The output voltage is sensed by an external feedback resistor string on FB pin and fed to an internal error amplifier. The output of error amplifier will compare with high side current sense signal by an internal PWM comparator. When the second signal is higher than the first one, the PWM comparator will generate a turn-off signal to turn off high side switch. The output voltage of error amplifier will increase or decrease proportionally with the output load current. PL8310D has a cycle-by-cycle peak current limit feature inside to help maintain load current in a safe region.

9.4 Sleep Operation for Light Load Efficiency

PL8310D has an internal feature to help improving light load efficiency. When output current is low, PL8310D will go into sleep mode.

9.5 Setting Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. 1% resistance accuracy of this resistor divider is preferred. The output voltage value is set as equation 1 below (R_1 is the upper resistor, R_2 is the lower resistor).

$$V_{out}=V_{ref}\times\frac{R_1+R_2}{R_2} \quad (1)$$

V_{ref} is the internal reference voltage of PL8310D, which is 0.9V.

9.6 Setting Enable Threshold

When the voltage at EN pin exceeds the threshold, PL8310D begins to work. When keeping EN low (below threshold), PL8310D stops working. The quiescent current of PL8310D is very low to maintain a good shut down operation for system.
PL8310D has an internal pull up resistor to make sure IC work when EN pin is float. If an application requires to control EN pin, use open drain or open collector output logic circuit to interface with it.
When system needs a higher VIN UVLO threshold, the EN pin can be configured as shown in Figure 17 below.

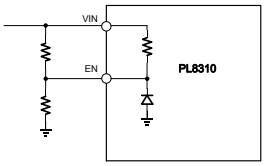


Fig.17 Adjustable VIN Under voltage Lockout

9.7 Slope Compensation

In order to avoid sub-harmonic oscillation at high duty cycle, PL8310D adds a slope compensation ramp to the sensed signal of current flowing through high side switch.

9.8 Error Amplifier

The error amplifier compares the FB voltage against the internal reference (V_{ref}) and outputs a current proportional to the difference between these two signals. This output current charges or discharges the internal compensation network to generate the error amplifier output voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control-loop design.

9.9 Bootstrap Voltage provided by internal LDO

PL8310D has an internal LDO to provide energy consumed by high side switch. At BST pin, PL8310D needs a small ceramic capacitor like 100nF between BST and SW pin to provide gate-drive voltage for high side switch. The bootstrap capacitor is charged when high side is off. In Continuous-Current-Mode, the bootstrap capacitor will be charged when low side is on. The bootstrap capacitor voltage will be maintained at about 5.3V. When IC works under sleep mode, what value the bootstrap capacitor is charged depends on the difference of Vin and output voltage. However, when the voltage on the bootstrap capacitor is below bootstrap voltage refresh threshold, PL8310D will force low side on to charge bootstrap capacitor. Connecting an external diode from the output of regulator to the BST pin will also work and increase the efficiency of the regulator when output is high enough.

9.10 High Side Over-Current Protection

In PL8310D, high-side MOSFET current is sensed. This sensed signal will compare the lower voltage between COMP pin voltage and over current threshold. High-side MOSFET will be turned off when the sensed current reaches the lower voltage. In normal operation, COMP pin voltage will be lower. If the over current threshold is lower, PL8310D enters over current protection mode.

9.11 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 155°C typically. When the junction temperature drops below 140°C, IC will start to work again.

9.12 Setting current limit

A current sensing resistor R3 can be used to adjust current limit. The following equation can be used to calculate the needed resistor value.

$$R_3=\frac{0.9}{I_{load}*15}\ \Omega \qquad (2)$$

9.13 Line drop compensation

When USB charging cable line is long and resistance is high, there will be some significant voltage drop on the cable. Portable device will see much lower input voltage. If the voltage across the load input terminals is too low, it will affect the charge time for the load. It is recommended to adjust the output voltage of charger to compensate this voltage drop. PL8310D has an configurable line drop compensation feature. The line drop compensation value can be programmed by the top feedback resistor R_1 in Fig 1. The line compensation voltage can be roughly calculated as following:

$$\Delta Vout=R_{cs}*I_{out}*15*R_1/200k\Omega \qquad (3)$$

R_{cs} is the sum of current sensing resistor on CS pin, all of the parasitic resistance on PCB board and GND pin. I_{out} is output load current going through R_{cs}. R1 is the top feedback resistor.

10 Application and Implementation

10.1 Inductor selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 25% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L=\frac{V_{OUT}}{f_s\times\Delta I_L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum peak current. The peak inductor current can be calculated by:

$$I_{L\_P}=I_{load}+\frac{V_{OUT}}{2\times f_s\times L}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Where I_{load} is the load current.

The choice of inductor material mainly depends on the price vs. size requirements and EMI constraints.

10.2 Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled with low side MOSFET to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2 – Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
SS25FA	50V/2A	Fairchild
B240A	40V/2A	Vishay

10.3 Input capacitors selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommend to use low ESR capacitors to optimize the performance. Ceramic capacitor is preferred, but tantalum or low-ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN}=I_{load}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2\times V_{OUT}$, where:

$$I_{CIN}=\frac{I_{load}}{2} \quad (7)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN}=\frac{I_{load}}{f_s\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

C_{IN} is the input capacitance.

10.4 Output capacitors selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended.

Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times f_s\times C_{OUT}}\right) \quad (9)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times f_s^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT}=\frac{V_{OUT}}{f_s\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulator. PL6320is optimized for a wide range of capacitance and ESR values.

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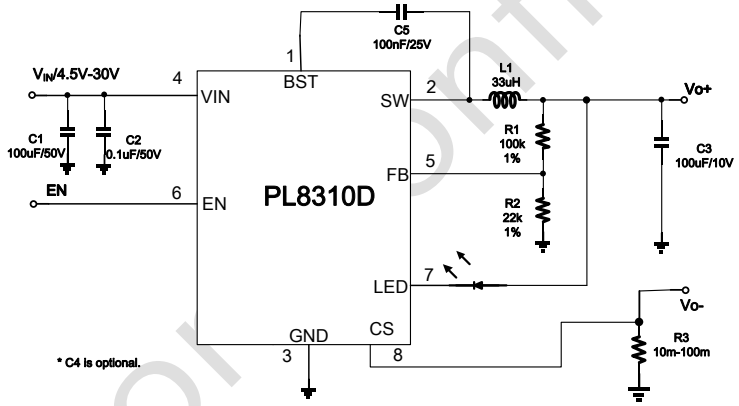
11 PCB Layout

11.1 Guideline

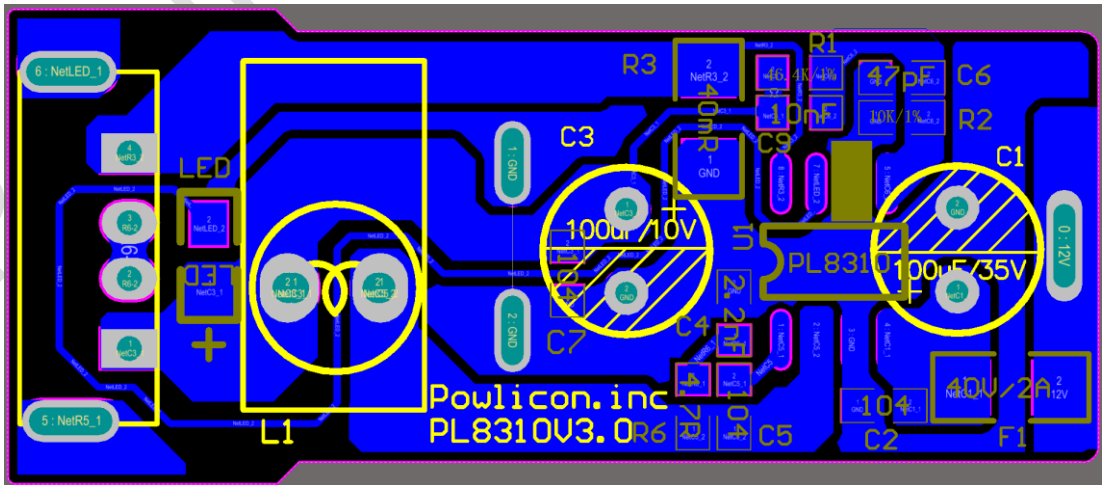
PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to FB pin. V_{out} sensing path should stay away from noisy nodes, such as SW and BST signals. The ground of R2 should be connected directly to GND pin by a single point. An optional 47pF capacitor C6 may be needed to improve the noise immunity for a poor placed PCB.
2. The input bypass capacitor C_1 and C_2 must be placed as close as possible to V_{IN} pin and GND pin. Grounding for both the input and output capacitors should consist of localized top side planes. Make the GND plane as big as possible for best thermal performance.
3. Place current sense resister R3 as close as possible to the chip and stay away from noisy nodes such as SW, BST.
4. Input capacitor, output capacitor, inductor and PL8310D should be placed evenly on the PCB board for the best thermal performance. Separate PL8310D from inductor as much as possible since they are the hottest components on the PCB.
5. R6, C4 may be needed to improve EMI in some design. The parameters for these components could be R6=4.7Ohm, C4=2.2nF. Connect R6 to SW and C4 to gnd. Place these two components close to SW pin and GND pin for the best EMI performance.
6. An external schottky diode may be needed to improve the current loading capability. Place the diode close to SW and GND pin as close as possible.

11.2 Example



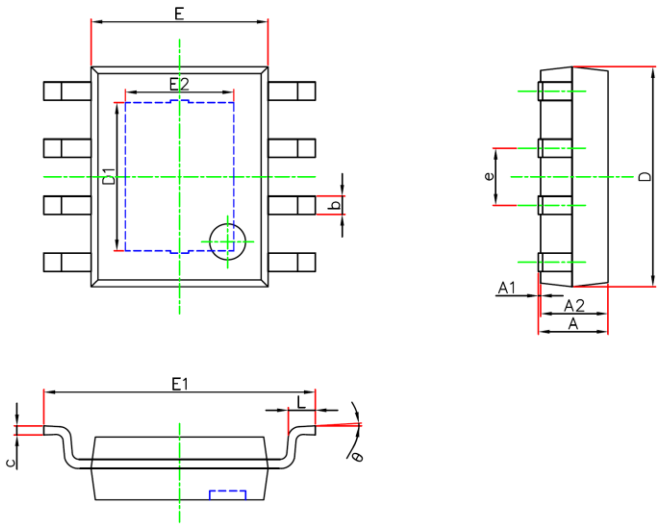
Work Mode 1: CS to GND with sensing resistor or short to GND directly
Fig.18 Schematic



C2, C6, C9 are optional, R6, C4 are used to improve EMI only
Work Mode 1: CS to GND with sensing resistor or short to GND directly
Fig.19 PCB Layout

12 Packaging Information

SOP8/PP(95×130) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°