High Efficiency 4-Switch Bidirectional Buck-Boost Controller

1 Features

- Bidirectional single Inductor Buck-Boost Controller for Step-Up/Step-Down DC/DC Conversion and battery charge management
- Bidirectional buck-boost operation to support battery charging and discharging using OTG signal
- Dynamical programming of input current, Output current and Output voltage using PWM signal or analog signal
- 1 Cell to 6 Cells battery charge management
- 2V to 32 V wide output range
- Comprehensive protection features including Output Short Protection (OSP), Cycle-by-Cycle input and output Peak Current Limit, thermal regulation, thermal shutdown, input UVLO, input OVP, output OVP etc.
- Adjustable Switching Frequency using resistor
- Frequency dithering for good EMI performance
- Integrated 2-A MOSFET Gate Drivers
- Input or Output Average Current Limiting with stable CC loop
- 5V/55mA low I_q LDO to power system MCU
- Available in QFN4x4-32 Package

2 Applications

- Automotive Start-Stop Systems
- Backup Battery and Super capacitor Charging
- Industrial PC Power Supplies
- USB Power Delivery

3 Description

PL5500 is a synchronous 4-switch bidirectional Buck-Boost controller capable of regulating the output voltage at above or below the input voltage. PL5500 operates over a wide input voltage range of 3.6 V to 32 V (36 V maximum) to support a variety of applications. PL5500 can operate at charger mode for 1, 2, 3, 4, 5 and 6 cells battery charge.

PL5500 employs Constant ON time control in buck, boost and buck-boost operation modes for superior load and line regulation. The switching frequency could be set to 150kHz, 300kHz, 600kHz or 1200kHz based on different resistor value between FREQ pin and GND pin. The device also features a programmable soft-start function and offers all kinds of protection features including cycle-by-cycle current limiting, input under voltage lockout (UVLO), output over voltage protection (OVP), input Over Voltage Protection, thermal shutdown and output short protection etc.

VADJ, IADJ pins are used to program output VBUS voltage and output current limit at battery discharging mode when OTG is high, which makes PL5500 an excellent option for USB Power Delivery (PD) application. PL5500 provides voltage control loop, constant current loop, thermal regulation loop, battery temperature sensing, which makes it a perfect solution for batter charge management.

4 Typical Application Schematic

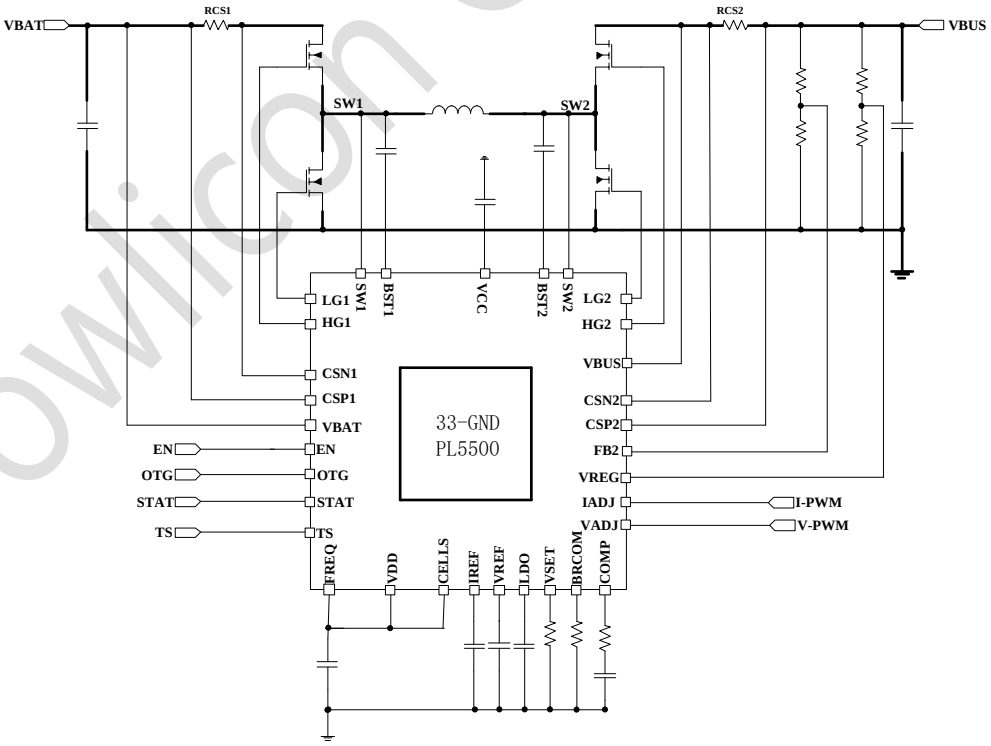


Fig. 1 Application Schematic

5 Pin Configuration and Functions

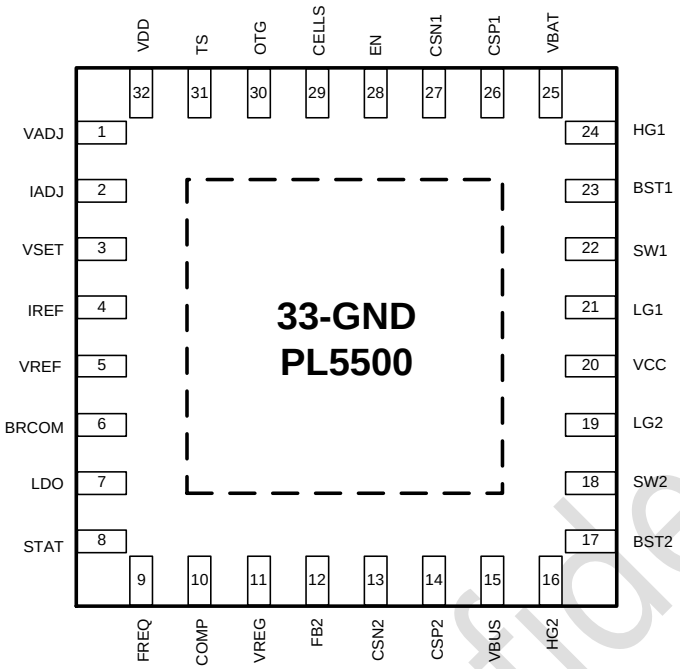


Fig. 2 Pin-Function (QFN4X4-32)

Pin		Description
Number	Name	
1	VADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on VREF pin. Connect this pin to VDD will force VREF to constant 2V.
2	IADJ	Connect a 0-2V analog voltage or a PWM signal to program voltage reference on IREF pin. Connect this pin to VDD will force IREF to 2V.
3	VSET	Connect a resistor between VSET and GND to program battery cell type (4.2V, 4.35V, 4.4V, 4.5V) when OTG is low and PL5500 is working in battery charging mode. When OTG is higher than 1.2V, voltage on VSET pin will be proportional to voltage difference between CSP2 and CSN2. Application processor can use this information to monitor discharging current in battery discharging mode.
4	IREF	Reference voltage for input and output current limiting loop.
5	VREF	Voltage reference for voltage control loop
6	BRCOM	Battery internal resistance compensation. The voltage on this pin will be proportional to voltage difference between CSP1 and CSN1. Application processor can use this information to monitor charging current in battery charging mode.
7	LDO	Low quiescent current 5V/55mA LDO. Directly powered from VBAT pin. LDO can be used as power supply for application processor such as MCU. When EN is low, only this LDO will be active to power MCU and keep low quiescent current for the whole system.
8	STAT	Charging status display when OTG=Low. PGOOD signal when OTG=High.
9	FREQ	Connect to GND to set the switching frequency at 150kHz. Connect this pin to VDD to set switching frequency at 300kHz. Connect to a resistor divider between VDD and GND to set frequency to 600k and 1200k Hz.
10	COMP	Error Amplifier output.
11	VREG	Add a resistor divider to program VBUS regulation voltage. When VBUS is pulled down to be close to VREG setting point due to heavy charging current in battery charging mode, the VREG regulation loop will take over the control and lower down charging current to keep VBUS from being further pulled down. VREG is not active in discharging mode.
12	FB2	VBUS voltage feedback. Connect a resistor divider between VBUS and GND to FB2 to program VBUS voltage in battery discharging mode.
13	CSN2	The minus input of output current sense.
14	CSP2	The positive input of output current sense.
15	VBUS	VBUS voltage
16	HG2	High side MOSFET driver 2.

17	BST2	Boost pin for high side MOSFET driver 2.
18	SW2	Connect this pin to the Switching point 2 of the power stage.
19	LG2	Low side MOSFET driver output 2.
20	VCC	6.6V power supply for high side and low side driver
21	LG1	Low side MOSFET driver output1.
22	SW1	Connect this pin to the Switching point1 of the power stage.
23	BST1	Boost pin for high side MOSFET driver1.
24	HG1	High side MOSFET driver1.
25	VBAT	Battery voltage or Input voltage.
26	CSP1	The positive input of input current sense.
27	CSN1	The minus input of input current sense.
28	EN	Logic High will enable the converter. Logic Low will disable the whole PL5500 except LDO. Only LDO is working to power system MCU when EN is low. EN is pulled high internally by a high value resistor.
29	CELLS	Connect a resistor divider between VDD and GND to program battery cells.
30	OTG	Connect OTG to 0 to set PL5500 in battery charging mode. Connect OTG to LDO to set PL5500 in battery discharging mode.
31	TS	Batter temperature sense
32	VDD	5.4V power supply for PL5500 control core.

6 Device Marking Information

Part Number	Order Information	Package	Package Qty	Top Marking
PL5500	**PL5500IQN32**	**QFN4x4 - 32**	**4000**	**5500 RAAYMD**

PL5500: Part Number
RAAYMD: RAA: LOT NO.; YMD: Package Date

7 Specifications

7.1 Absolute Maximum Ratings(Note1)

PARAMETER	MIN	MAX	Unit
VBAT, VBUS, CSN1, CSN2, CSP1, CSP2, SW1, SW2	-0.3	40	V
HG1, BST1 to SW1	-0.3	7	
HG2, BST2 to SW2	-0.3	7	
LG1, LG2, VCC to GND	-0.3	7	
CSP1 to CSN1	-0.3	0.6	
CSP2 to CSN2	-0.3	0.6	
VBAT to CSP1, CSN1	-0.3	0.6	
VBUS to CSP2, CSN2	-0.3	0.6	
Other Pins to GND	-0.3	6	

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{ST}	Storage Temperature Range	-65	150	°C
T_J	Junction Temperature		+150	°C
T_L	Lead Temperature		+260	°C
V_{ESD}	HBM Human body model	2		kV

7.3 Recommended Operating Conditions (Note 2)

	PARAMETER	MIN	MAX	Unit
Input Voltages	VBAT，VBUS	3.6	32	V
Temperature	Operating junction temperature range, T_J	-40	+125	°C

7.4 Thermal Information(Note 3)

Symbol	Description	QFN4X4-32	Unit
θ_{JA}	Junction to ambient thermal resistance	44	°C/W
θ_{JC}	Junction to case thermal resistance	9	

Notes:
1) Exceeding these ratings may damage the device.
2) The device function is not guaranteed outside of the recommended operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

7.5 Electrical Characteristics (Typical at VBAT = 12V, T_J =25°C, unless otherwise noted.)

Supply voltages	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VBAT	Battery voltage		3.6		32	V
$I_{Q\_}$ VBAT	VBAT Shutdown Current	EN=0V, VBAT=7.2V		15		uA
	VBAT Supply Current	No Switching, FB=2.1V		1000		uA
VBUS	Bus line voltage		3.6		32	V
$I_{Q_}$VBUS	VBUS Shutdown Current	EN=0V, VBUS=7.2V		15		uA
	VBUS Supply Current	No Switching, battery fully charged		1200		uA
V_{VCC}	Driver power supply voltage	VBAT =15V		6.6		V
V_{VDD}	Control core power supply voltage	VBAT =15V		5.4		V
V_{LDO}	LDO output voltage	VBAT =15V		5		V
I_{LDO}	LDO output current	V_{LDO} =5V			55	mA
UVLO/EN						
$VBAT_{\_UV}$	VBAT UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
$VBUS_{\_UV}$	VBUS UVLO Rising			3.5		V
	UVLO Hysteresis			300		mV
V_{EN_UV}	Operation Threshold		1.1	1.2	1.3	V
	Hysteresis			200		mV
OTG						
V_{TH_OTG}	OTG high voltage threshold			1.2		V
V_{HY_OTG}	OTG Hysteresis		200			mV
VREF						
V_{VREF_Dischg}	VREF voltage in discharge mode	VADJ connected to VDD		2		V
V_{VREF_chg}	VREF voltage in charge mode	VADJ connected to VDD		1.8		V
Battery charge setting						
V_{cell_num}	Battery cells number setting. V_{cell} is set by VSET pin.	VCELLS=0-0.9V		1*V_{cell}		V
		VCELLS=4.5-5.5V		2*V_{cell}		V
		VCELLS=0.9-1.8V		3*V_{cell}		V
		VCELLS=1.8-2.7V		4*V_{cell}		V
		VCELLS=2.7-3.6V		5*V_{cell}		V
		VCELLS=3.6-4.5V		6*V_{cell}		V
V_{TH_TRKL}	Trickle charge threshold. VBAT voltage			3		V
V_{HY_TRKL}	Trickle charge Hysteresis. VBAT voltage			0.5		V
V_{RECHAG}	Battery recharge voltage			4		V
$VBAT_{\_FULL}$	Batter full charge voltage	V_{VSET} :0.4-0.9V Rset:220k		4.2		V
		V_{VSET} :0.9-1.9V Rset:430k		4.35		V
		V_{VSET} :1.9-5.5V, short VSET pin to VDD.		4.4		V
		V_{VSET} :0-0.4V, short VSET pin to GND.		4.5		V
V_{REG}	Charge Input regulation voltage	VREG		1.2		V
Control loop						
V_{FB2}	VFB2 regulation voltage in discharging mode	FB2 voltage		2		V
G_{mEA}	Error amplifier gm			450		uS
I_{SINK}	COMP sink/source current	VFB=VREF+100mV		15		uA
I_{SOURCE}	COMP source current	VFB=VREF-100mV		20		uA
I_{FB2}	FB2 bias current	FB2 in regulation			100	nA
Frequency						
F_{SW}	Switching Frequency	FREQ 0-0.4V, short FREQ pin to GND.		150		KHz
		FREQ 1.8-5.4V, short FREQ pin to VDD.		300		KHz
		FREQ 0.4-0.85V		600		KHZ
		FREQ 0.85-1.8V		1200		KHZ

Current Limit				
I_{CCLIM_BAT}	Battery average current Limit, V_{CSP1}- V_{CSN1}	Discharging mode	80	mV
		Charging mode	40	mV
I_{CCLIM_BUS}	Bus average current Limit, V_{CSP2}- V_{CSN2}	Discharging mode	40	mV
		Charging mode	80	
NMOS Driver				
$I_{HDRV1,2}$ (Note 4)	Driver peak source current	VBST-VSW=6.6V	2	A
	Driver peak sink current	VBST-VSW=6.6V	2	A
$I_{LDRV1,2}$ (Note 4)	Driver peak source current	VCC=6.6V	2	A
	Driver peak sink current	VCC=6.6V	2	A
V_{BSTUV}	UVLO		2	V
	UVLO Hysteresis		300	mV
Output Protection				
V_{OVP}	Output over voltage threshold		110	%
V_{UVP}	Output under voltage threshold		50	%
VADJ, IADJ				
V_{TH_VADJ} (Note 4)	VPWM low voltage		0.4	V
	VPWM high voltage		2.5	V
V_{TH_IADJ} (Note 4)	IPWM low voltage		0.4	V
	IPWM high voltage		2.5	V
T_{SD} (Note 4)	Thermal Shutdown Threshold		150	°C
T_{HYS} (Note 4)	Thermal Shutdown Hysteresis		20	°C

Notes:
4) Guaranteed by design.

8 Typical Characteristics

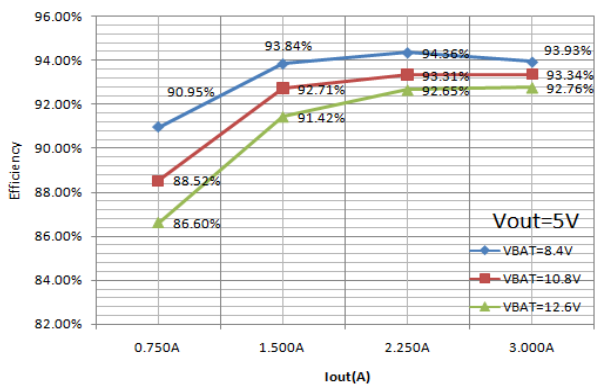


Fig. 3 Efficiency

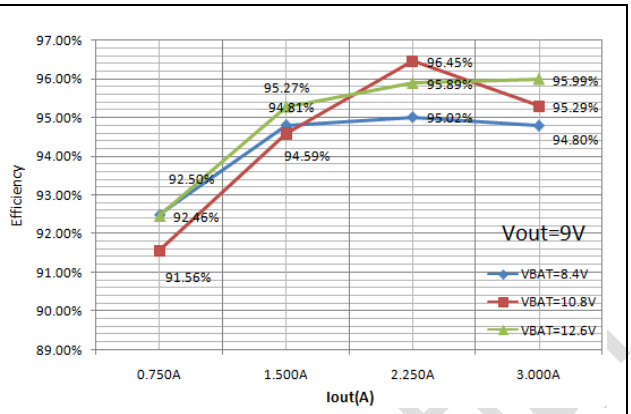


Fig. 4 Efficiency

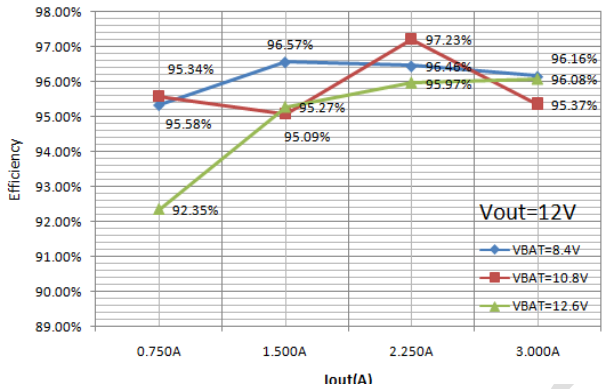


Fig. 5 Efficiency

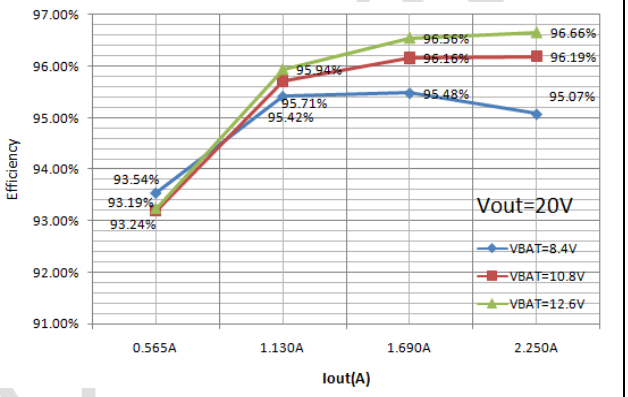
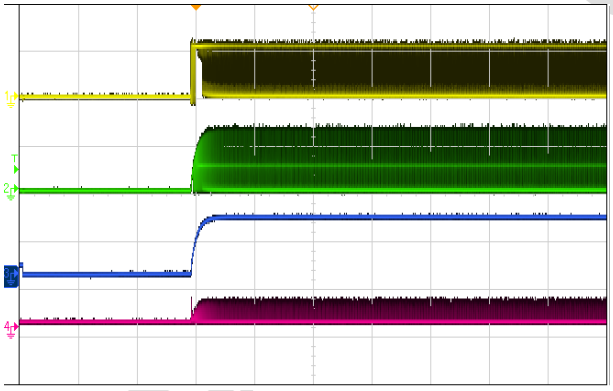


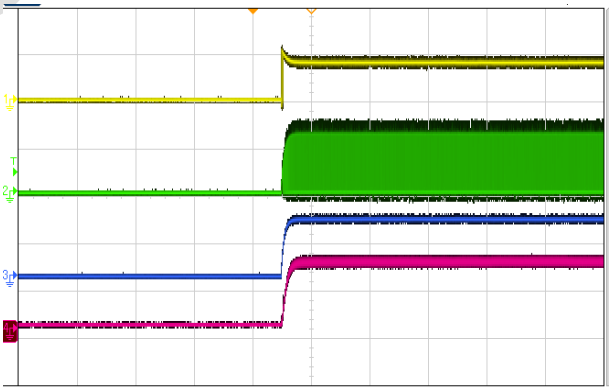
Fig. 6 Efficiency



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=4.5V Vout=12V

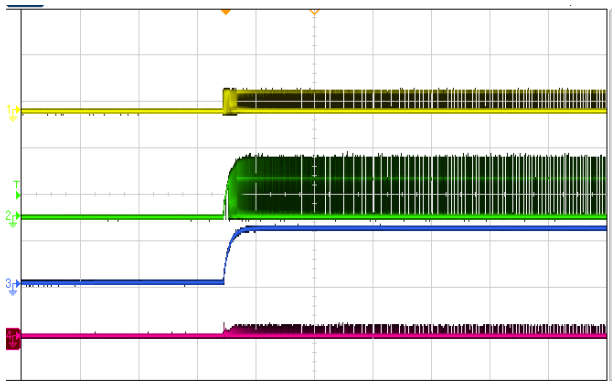
Fig.7 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=4.5V Vout=12V

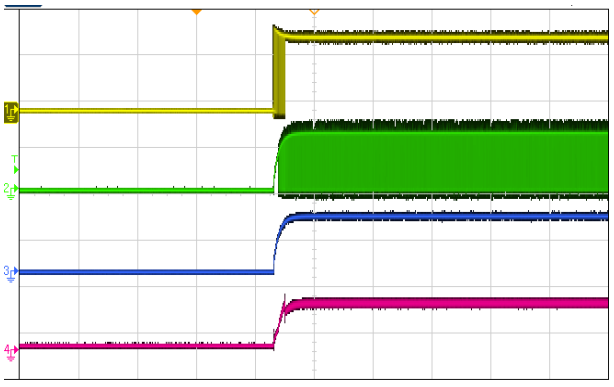
Fig.8 Start up waveform, Iout =2A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

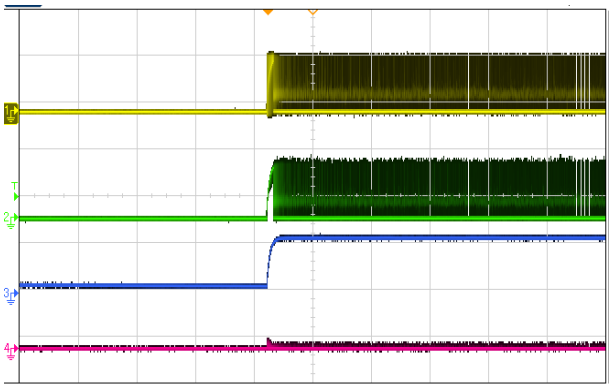
Fig.9 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

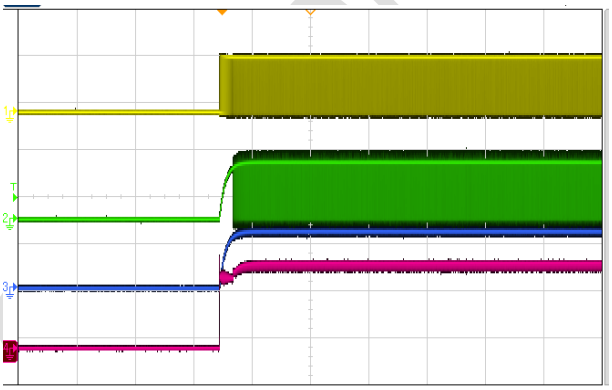
Fig.10 Start up waveform, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

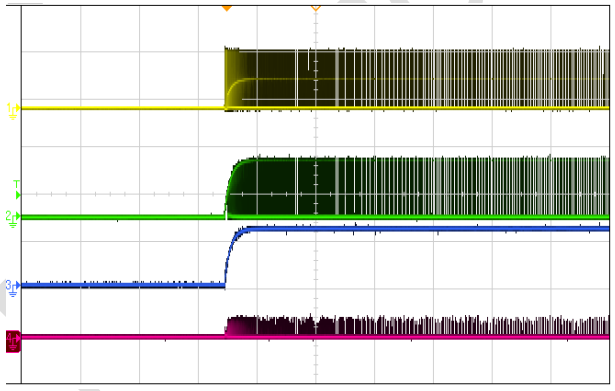
Fig.11 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

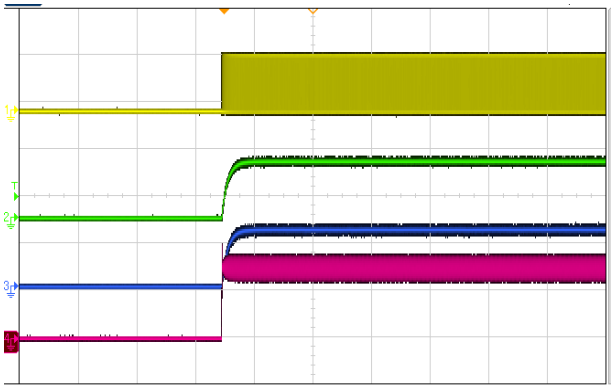
Fig.12 Start up waveform, Iout =3A



CH1:SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

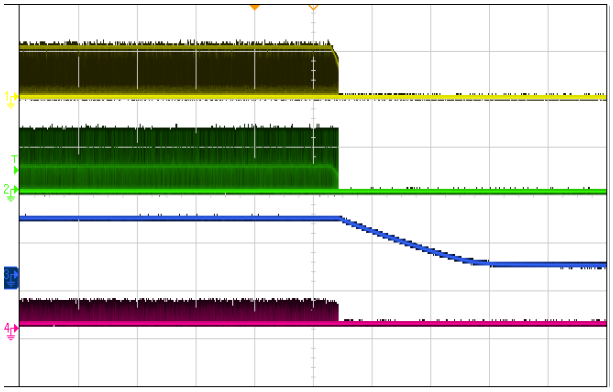
Fig.13 Start up waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

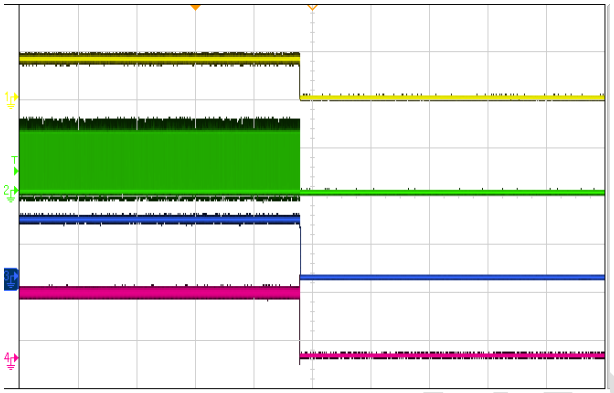
Fig.14 Start up waveform, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=4.5V Vout=12V

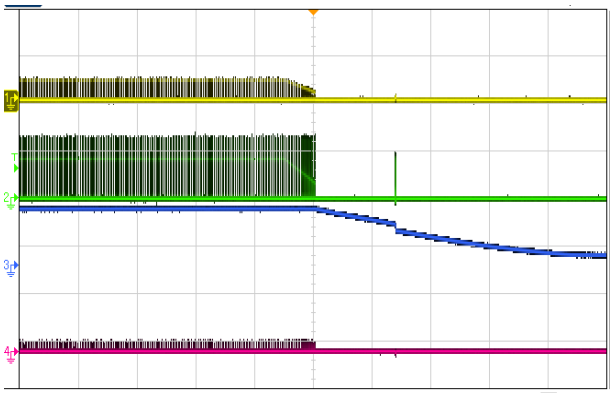
Fig.15 Shut down waveform, Iout =0A



CH1: SW1 CH2:Vout CH3:SW CH4:IL

Vin=4.5V Vout=12V

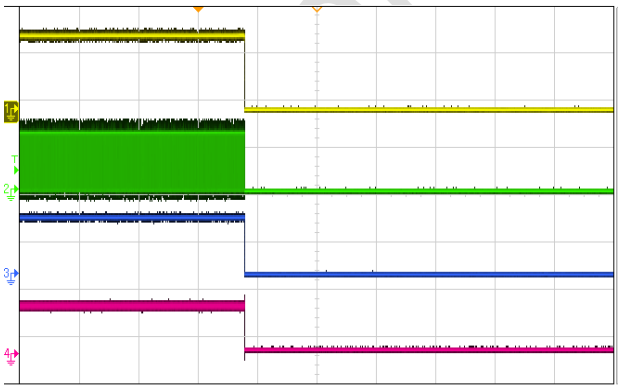
Fig.16 Shut down waveform, Iout =2A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

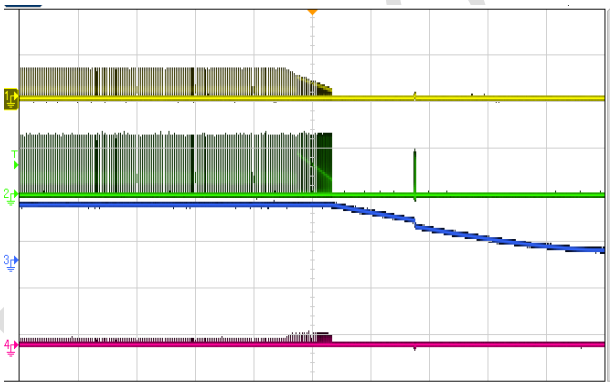
Fig.17 Shut down waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

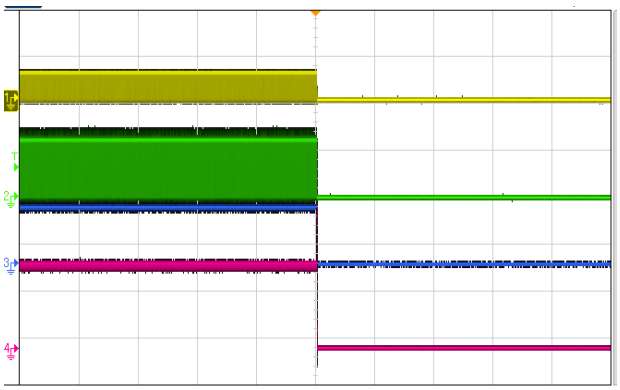
Fig.18 Shut down waveform, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

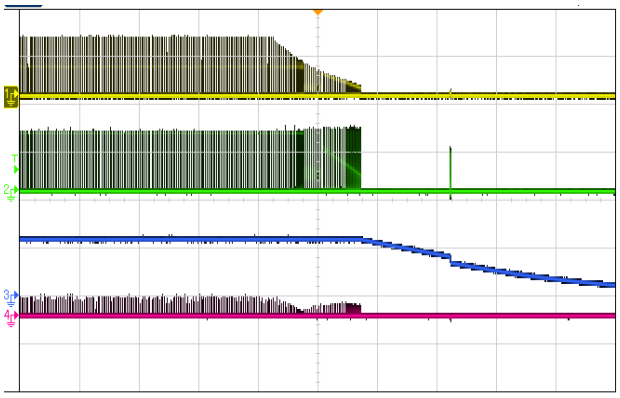
Fig.19 Shut down waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

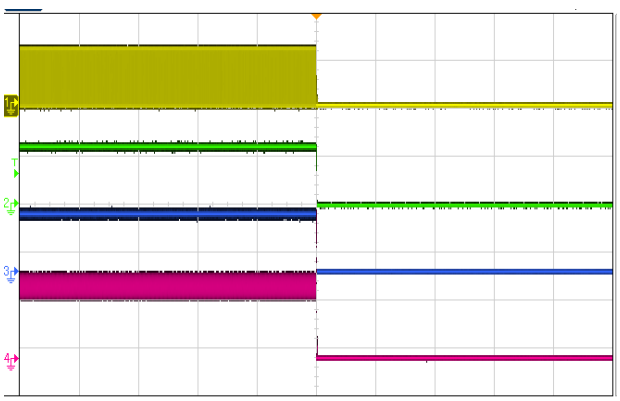
Fig.20 Shut down waveform, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

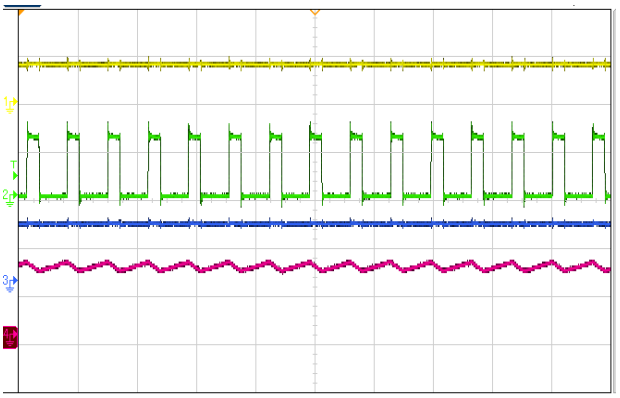
Fig.21 Shut down waveform, Iout =0A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

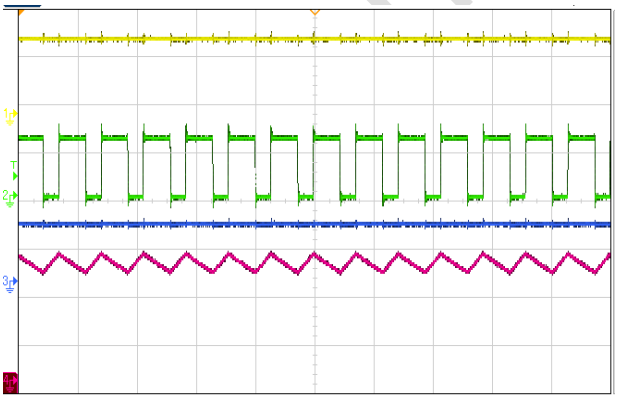
Fig.22 Shut down waveform, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=4.5V Vout=12V

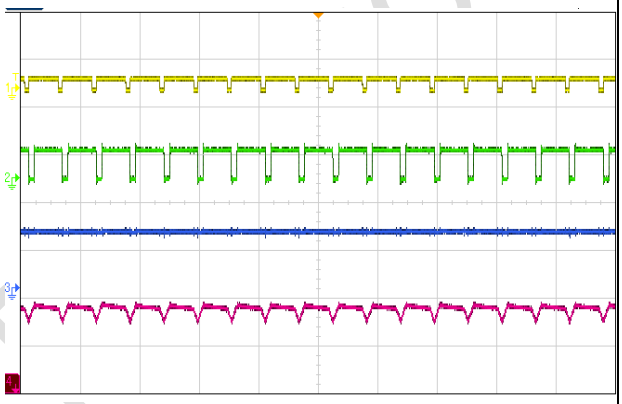
Fig.23 Steady State, Iout =2A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

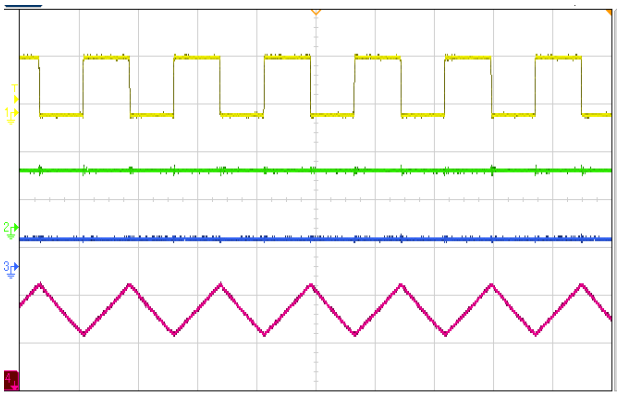
Fig.24 Steady State, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

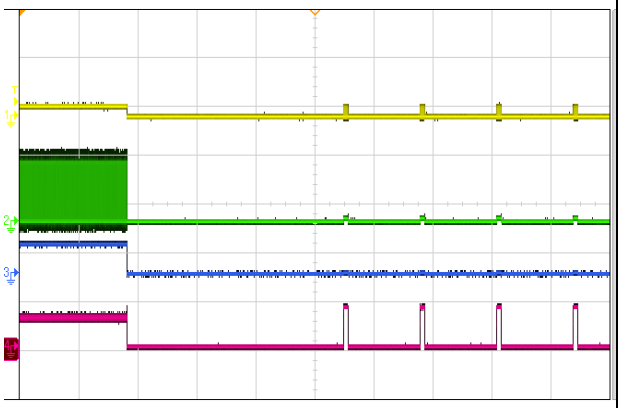
Fig.25 Steady State, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

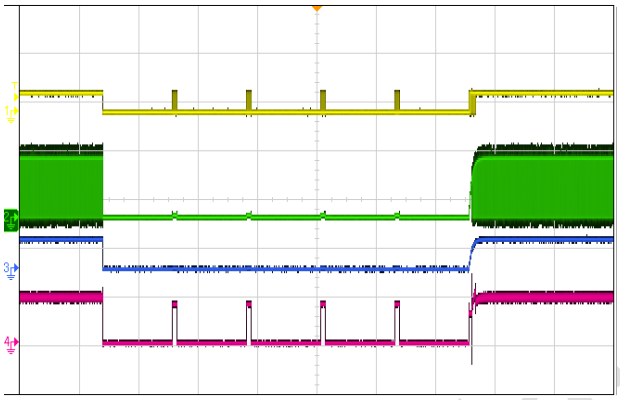
Fig.26 Steady State, Iout =3A



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=4.5V Vout=12V

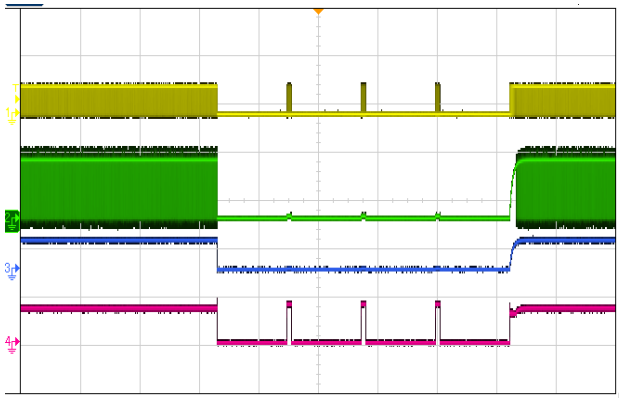
Fig.27 Short Circuit waveform



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=8.4V Vout=12V

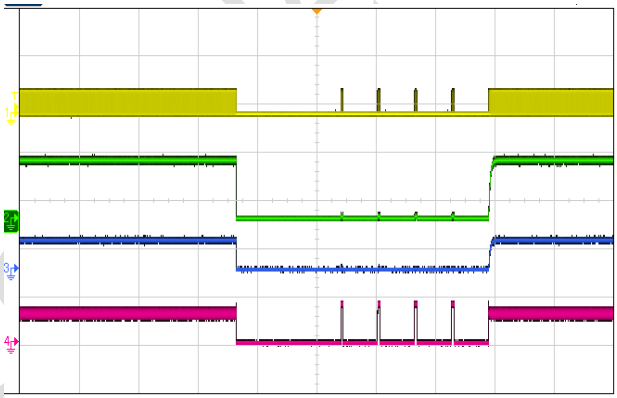
Fig.28 Short Circuit waveform



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=12V Vout=12V

Fig.29 Short Circuit waveform



CH1: SW1 CH2:SW2 CH3:Vout CH4:IL

Vin=24V Vout=12V

Fig.30 Short Circuit waveform

9 Detailed Descriptions

9.1 Overview

PL5500 is a synchronous 4-switch bidirectional Buck-Boost controller capable of regulating the output voltage at, above, or below the input voltage. PL5500 operates over a wide input voltage range of 3.6 V to 32 V (36 V maximum) to support a variety of applications. PL5500 can operate at charger mode for 1, 2, 3, 4, 5 and 6 cells battery charge. It operates in buck mode when V_{IN} is greater than V_{OUT} and in the boost mode when V_{IN} is less than V_{OUT}. When V_{IN} is close to V_{OUT}, the device operates in a proprietary buck-boost mode. The control scheme provides smooth operation for any input/output combination within the specified operating range. In discharging mode with OTG=high, V_{IN} is VBAT, V_{OUT} is VBUS. In charging mode with OTG=low, V_{IN} is VBUS, V_{OUT} is VBAT.

9.2 Functional Block Diagram

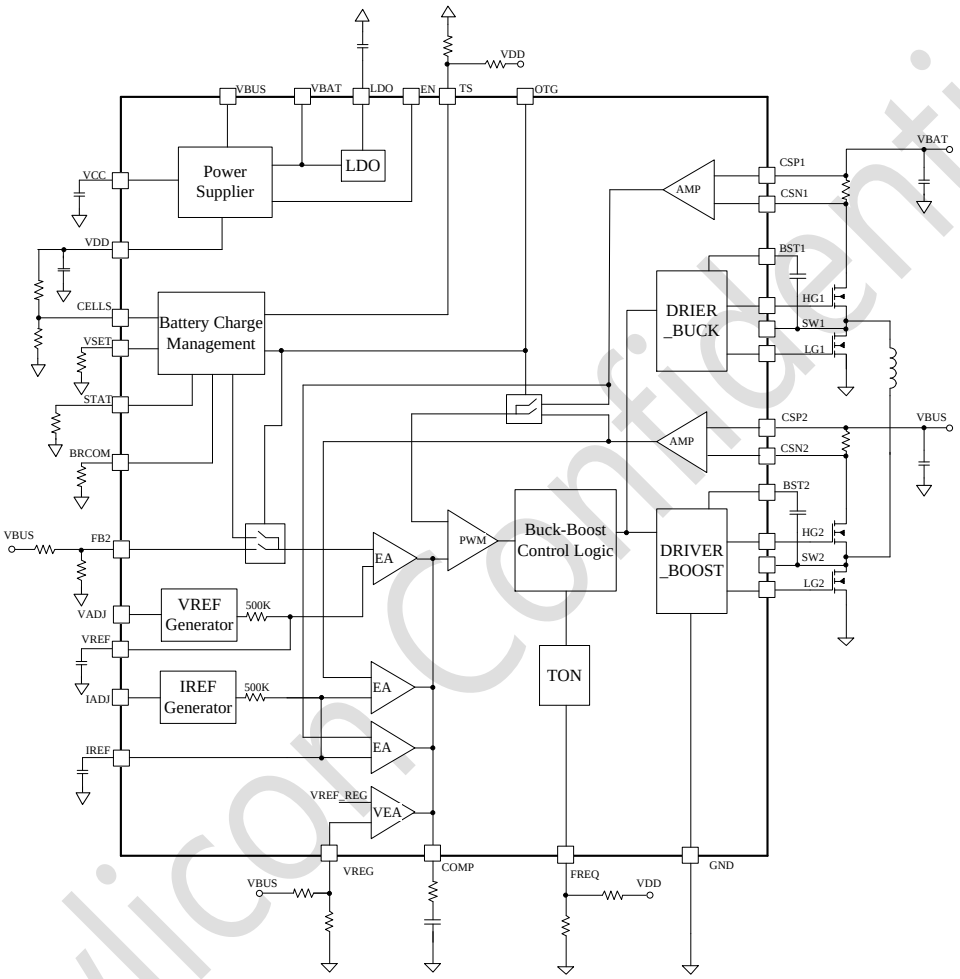


Fig. 31 PL5500 Block Diagram

9.3 Enable/UVLO

When EN is greater than 1.2V operating threshold, the control loop starts to work and regulate output to target voltage. When EN pin is below the standby threshold (1.1V typical), PL5500 stops working with only LDO is active to power MCU. EN is pulled high to 4V internally using a 2Meg resistor.

9.4 Over current Protection and short circuit protection

PL5500 provides cycle-by-cycle current limit to protect against over current and short circuit conditions. When VOUT is drop to UV threshold, PL5500 will go into hiccup mode to lower down power consumption.

9.5 Average Input/Output Current Limiting

PL5500 provides optional average current limiting capability to limit either the input or the output current. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the CSP1 and CSN1 pins monitors the voltage across the sensing resistor and compares it with an internal 40 mV reference. If the drop across the sense resistor is greater than 40 mV, the gm amplifier regulates COMP voltage to lower down input or output current. The target constant current is given by Equation 1:

$$I_{CL(AVG)} = \frac{40\ mV}{R_{SNS}} \quad (1)$$

The average current loop can be disabled by shorting CSP1 to CSN1 or CSP2 to CSN2.

9.6 Frequency Setting (FREQ) and frequency dithering

PL5500 switching frequency can be programmed at 150 kHz, 300 kHz or 600 kHz and 1200 kHz by voltage at FREQ pin to GND. When FREQ is connected to AGND, the switching frequency is set at 150 kHz. When FREQ is connected to VDD, the switching frequency is set at 300 kHz. A voltage divider between VDD and GND pin can be used to program switching frequency if 600 kHz or 1200 kHz is required.

9.7 Integrated Gate Drivers

PL5500 provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pins. Each driver is capable of sourcing 2 A and sinking 2 A peak current. In buck operation, LG1 and HG1 are switched by the PWM controller while HG2 remains continuously on. In boost operation, LG2 and HG2 are switched while HG1 remains continuously on. In DCM buck operation, LG1 and HG2 are turned off when the inductor current drops to zero (diode emulation).

The gate drive output HG2 remains off before the first high side switch is turned on to prevent reverse current flow from a pre-biased output..

9.8 Thermal Shutdown

PL5500 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 160°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

9.9 Thermal sensing TS

PL5500 use TS pin to sense battery temperature. A voltage divider can be used at TS pin to program the protection trigger point in charging mode or discharging mode.

9.10 Battery internal resistor compensation

BRCOMP pin is used to compensate battery internal resistance during high current charging period. A resistor between BRCOMP pin and GND is used to program voltage compensation as the following equation:

$$\Delta Vbat = \frac{Rcs * Ibat * Aisense * 8k}{Rbrcom} \quad (2)$$

$\Delta Vbat$ is the compensated batter voltage change. Rcs is current sensing resistor at VBAT side. Ibat is battery charging current. Aisense is current sensing gain at VBAT side, which is normally around 50. Rbrcom is resistor value between BRCOM pin and GND.

9.11 Status display STAT and power good signal

PL5500 use STAT pin as charging status display in battery charging mode and power good signal in discharging mode. When single battery voltage is less than 3V, STAT will send out a PWM signal at 0.6s period with 50% duty cycle. When

battery voltage is higher than 3V, STAT pin will be constant low to indicate high current charging status. When battery voltage is higher than 4V and charging current is lower than the termination current level, STAT will send out constant high signal to indicate the battery is charged fully.

In discharging mode, STAT will act as a power good signal. STAT will be constant high when FB voltage is not in OV or UV status.

9.12 VREF and IREF

VREF pin is the final reference voltage used in the voltage regulation loop. When VADJ is connected to VDD, VREF will be 2V in discharging mode and 1.8V in charging mode. When VADJ is connected to a PWM signal, PWM signal will first be chopped to 2V and filter out using an internal resistor and external capacitor on VREF pin. The capacitor on VREF pin is also acting as soft-start capacitor at power up or in output voltage transition period. It is recommend using a relatively large capacitor such as 470nF for VREF pin and IREF pin.

The same mechanism works for IADJ and IREF pin.

10 Applications and Implementation

The typical application on the first page is a basic PL5500 application circuit. External component selection is driven by the load requirement, and begins with the selection of RS1, RS2 and the inductor value. Next, the power MOSFETs need to be selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 32V.

10.1 R_{CS} Selection

As shown in Figures 32, input/output current sense resistor RCS1/RCS2 should be placed between the bulk capacitor for VBAT/VBUS and the decoupling capacitor. A low pass filter formed by RF and CF is recommended to reduce the switching noise and stabilize the current loop. If input/output current limit is not desired, then CSP1/CSN1 and CSP2/CSN2 pins should be shorted to either VBAT or VBUS.Place CSP1/CSN1, CSP2/CSN2 symmetrically and keep them away switching signals such as BST1, BST2, SW1, SW2, VBAT, VBUS etc.

10.2 Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple, the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 * (V_{OUT} - V_{IN(MIN)}) * 1000}{f * \Delta I_L * V_{OUT}^2} uH \quad (3)$$

$$L_{BUCK} > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 1000}{f * \Delta I_L * V_{IN(MAX)}} uH \quad (4)$$

where: f is operating frequency, kHz

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

ΔI_L is maximum inductor ripple current, A, usually select 20~40% maximum output current.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

10.3 C_{IN} and C_{OUT} Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{CIN} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

This input current has a maximum at $V_{IN} = 2V_{OUT}$, $I_{CIN(MAX)} = I_{OUT(MAX)}/2$.

In the boost region, C_{OUT} must be capable of reducing the output voltage ripple because of the discontinuous output current. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{(BOOST,Cap)} = \frac{I_{OUT(MAX)} * (V_{OUT} - V_{IN(MIN)})}{C_{OUT} * V_{OUT} * f} V \quad (6)$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{(BOOST,ESR)} = I_{OUT(MAX,BOOST)} * ESR \quad (7)$$

In buck mode, V_{OUT} ripple is given by:

$$\Delta V_{OUT} \leq \Delta I_L * \left(ESR + \frac{1}{8*f*C_{OUT}} \right) \quad (8)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

10.4 Power MOSFET Selection and Efficiency Considerations

PL5500 requires four external N-channel power MOSFETs, two for the top switches (switches Q1 and Q3, shown in Figure 32) and two for the bottom switches (switches Q2 and Q4, shown in Figure 32). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,\ DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$. The drive voltage is set by the 6.6V VCC supply to make the MOSFET's selection more flexible.

10.5 Output voltage setting

The PL5500 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The 1% resistance accuracy of this resistor divider is preferred. The resultant feedback signal is compared with the internal precision 2V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 2V * \left(1 + \frac{R_1}{R_2}\right) \quad (9)$$

Where R_1 is the upper resistor and R_2 is the lower resistor in the feedback network.

11 PCB Layout

11.1 Guideline

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistor R1 and R2, should be kept close to the FB2 pin. Keep VBUS sensing path away from noisy nodes and preferably through a layer on the other side of shielding layer.
2. The input /output bypass capacitor must be placed as close as possible to the VBAT/VBUS pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the VBAT and VBUS pin to reduce the high frequency injection current.
3. The inductor L should be placed close to the SW1and SW2 pin to reduce magnetic and electrostatic noise.
4. Current sensing pairs (CSP1,CSN1), (CSP2,CSN2) need to be placed carefully, Layout the lines symmetrically and keep them away from noisy nodes such as BST1,BST2, SW1, SW2, HG1,HG2, LG1,LG2 etc. Connect these nodes directly to the two terminals of current sensing resistors Rcs1, Rcs2 to form an accurate Kelvin connection.

11.2 Application Examples

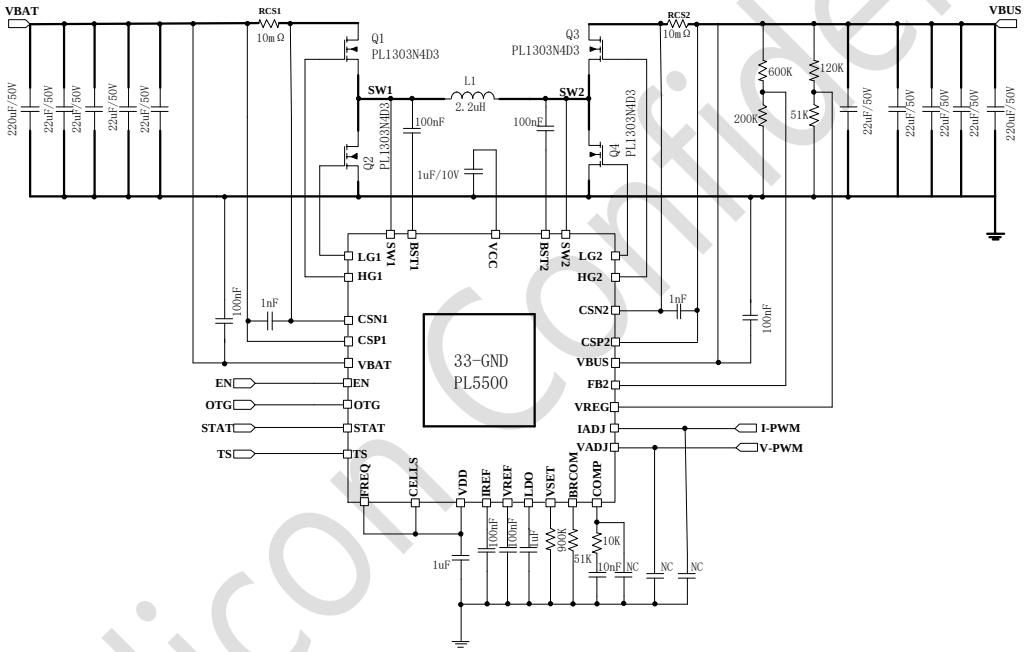


Fig. 32 Schematic

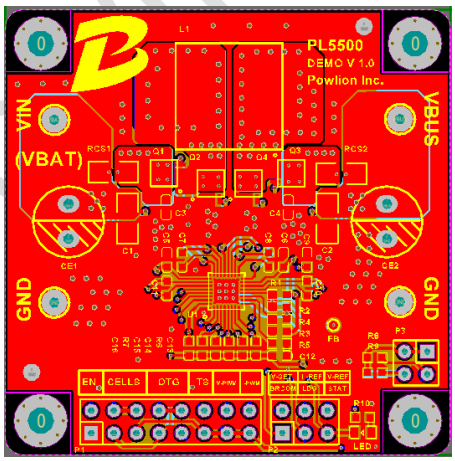


Fig. 33 Toplay

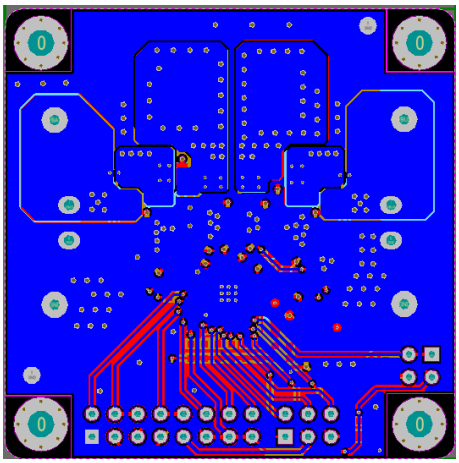
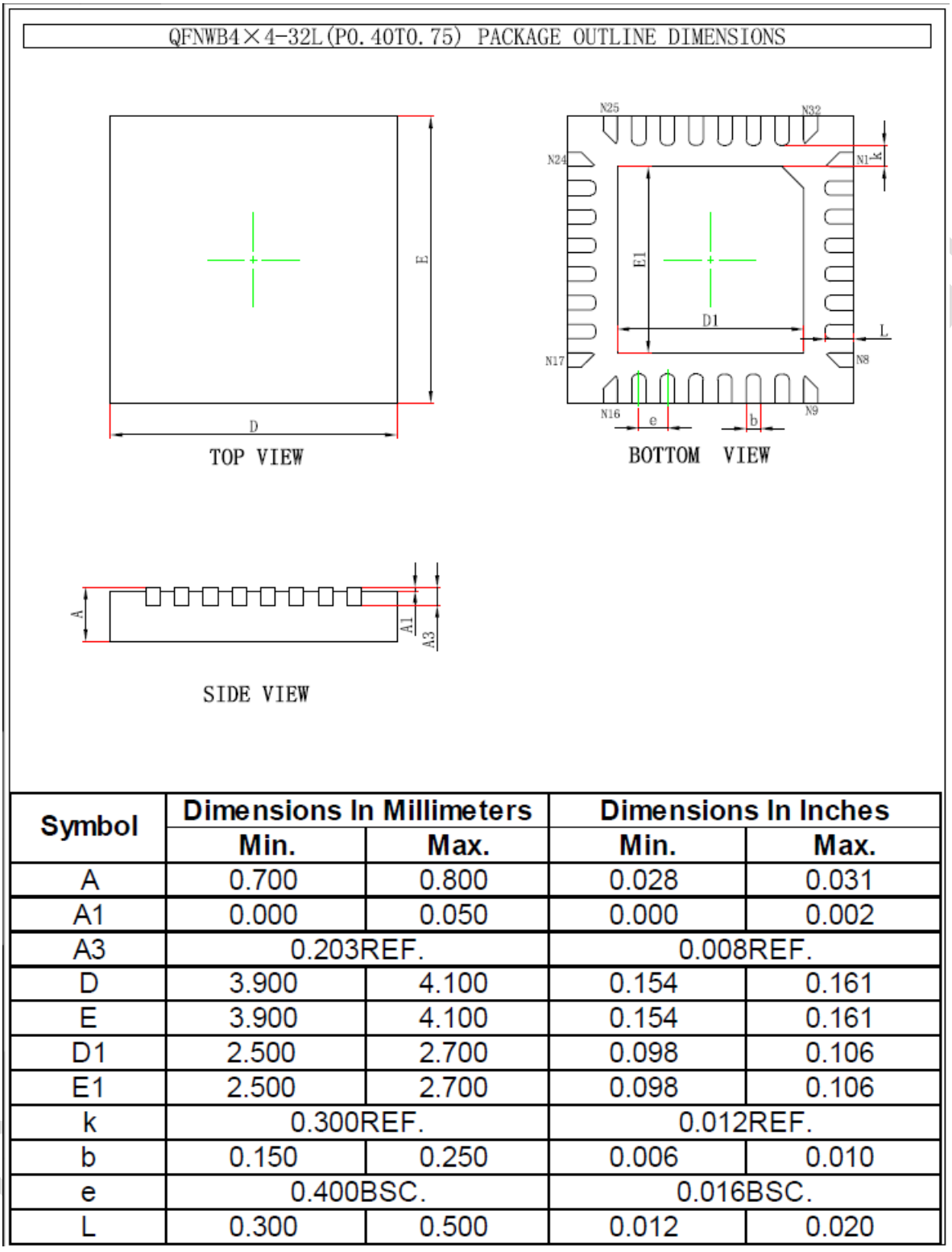


Fig. 34 Bottomlay

12 Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.500	2.700	0.098	0.106
E1	2.500	2.700	0.098	0.106
k	0.300REF.		0.012REF.	
b	0.150	0.250	0.006	0.010
e	0.400BSC.		0.016BSC.	
L	0.300	0.500	0.012	0.020