VA2208

15W Filterless Stereo Class D Audio Amplifier

General Description

The VA2208 is a cost-effective filter-less Class D stereo audio power amplifier that operates in wide range of various power supplies. VA2208 provide volume control with four selectable gain settings (20dB, 26dB, 32dB, 36dB). VA2208 can output 15W per channel into 8Ω load with lower supply current and fewer external components for driving bridged-tied stereo speaker directly. With the function of power limit, the speakers could be operated safely and the input signal would be also normalized.

VA2208 operates with high efficiency energy conversion up to 88% (8Ω Load) so that the external heat sink can be eliminated while playing music.

VA2208 also integrates Anti-Pop, Output Short & Over-Heat Protection Circuitry to ensure device reliability. This device also provides the DC detect and protection scheme to prevent the damage of speaker voice coils.

The VA2208 is available in small TSSOP-28 green package with exposed pad.

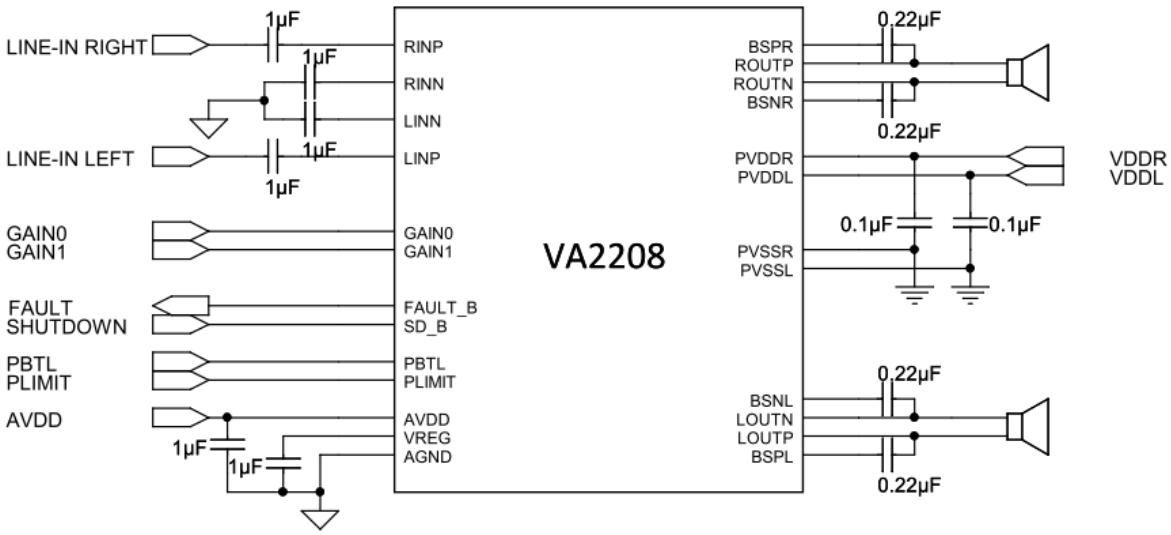
Features

- Operation Voltage from 8V to 26V
- Maximum 88% Efficiency with an 8Ω Speaker
- 15W@8Ω Load with THD+N =10% at 16V
- 10W@8Ω Load with THD+N =10% at 13V
- Four Selectable Gain Settings
- Scalable Power Limit Function
- Speaker DC Detection and Protection
- Parallel BTL Speaker Driving Connection
- Thermal Protection with Auto-Recovery
- Speaker Protection Circuitry
- Short Circuit and Thermal Protection
- RoHS 2.0 compliant TSSOP-28 Green Package with Exposed Pad

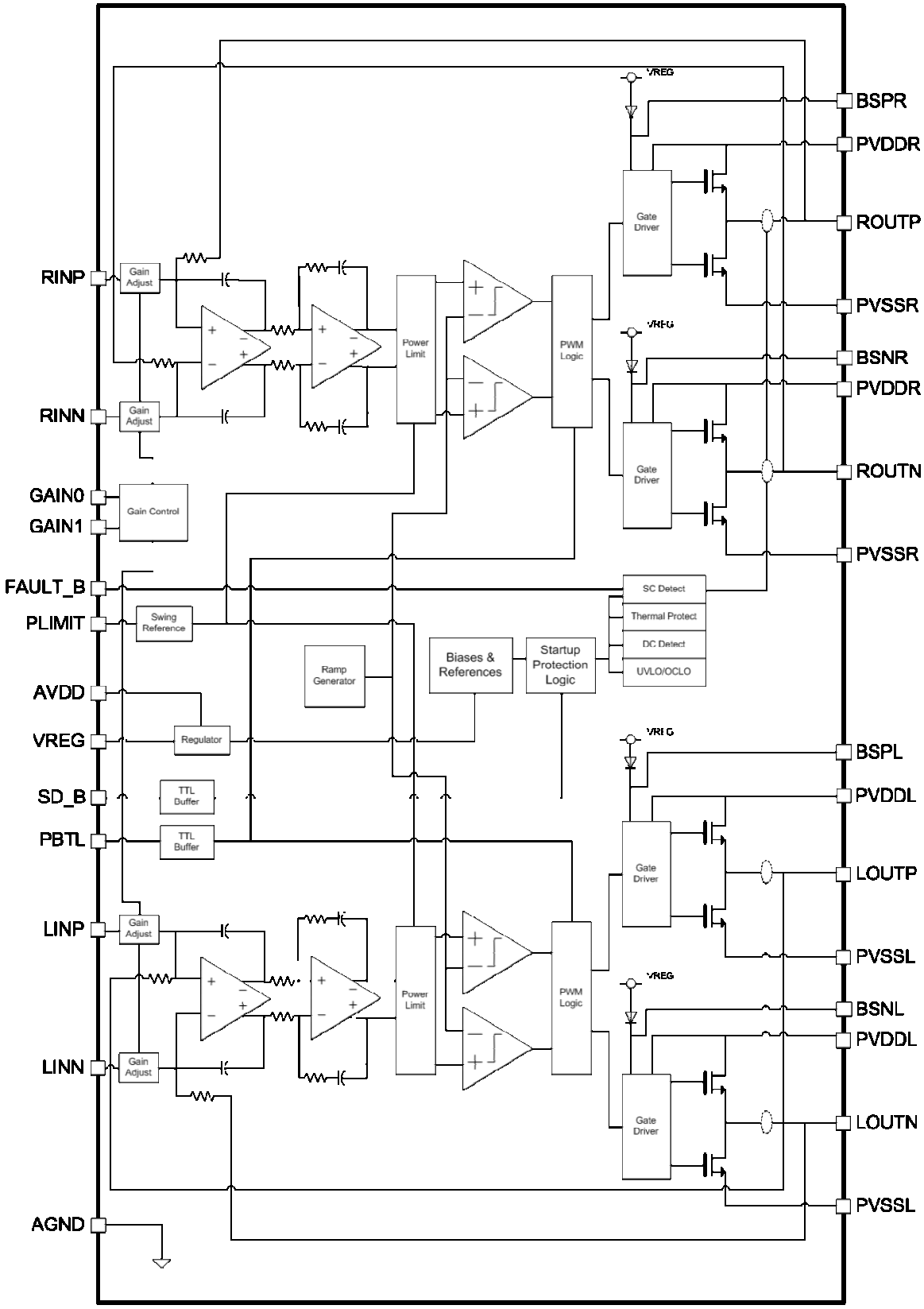
Applications

- LCD TV
- Multimedia Speakers
- Sound Bar

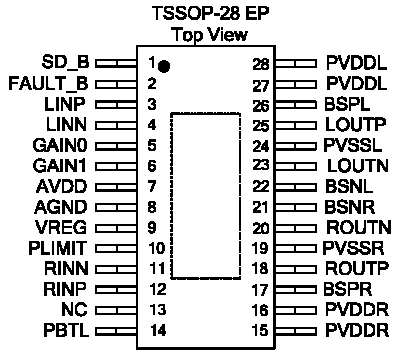
Typical Application



Functional Block Diagram



Pin Assignments And Descriptions



Pin No.	Pin	I/O/P	Function Description
1	SD_B	I	Shutdown control terminal. Low active. TTL Logic levels with compliance to AVDD.
2	FAULT_B	O	Protection Flag Indicator (Open Drain). Connecting FAULT_B and SD_B can be set to auto-recovery. Otherwise need to reset by cycling AVDD.
3	LINP	I	Left channel positive audio signal input.
4	LINN	I	Left channel negative audio signal input.
5	GAIN0	I	Gain selection least significant bit.
6	GAIN1	I	Gain selection most significant bit.
7	AVDD	P	Analog Power Supply.
8	AGND	P	Analog Ground.
9	VREG	O	Regulated Voltage. Nominal voltage is 5.5V.
10	PLIMIT	I	Power Limit Level Adjust. Connect a resistor divider from VREG to GND to set power limit. Connect to VREG directly for no power limit.
11	RINN	I	Right channel negative audio signal input.
12	RINP	I	Right channel positive audio signal input.
13	NC	-	No internal connection.
14	PBTL	I	Parallel BTL mode switch.
15,16	PVDDR	P	Right channel power supply.
17	BSPR	I	Bootstrap I/O for right channel positive high-side switch.
18	ROUTP	O	Right channel positive output.
19	PVSSR	P	Right channel power ground.
20	ROUTN	O	Right channel negative output.
21	BSNR	I	Bootstrap I/O for right channel negative high-side switch.
22	BSNL	I	Bootstrap I/O for left channel negative high-side switch.
23	LOUTN	O	Left channel negative output.
24	PVSSL	P	Left channel power ground.
25	LOUTP	O	Left channel positive output.
26	BSPL	O	Bootstrap I/O for left channel positive high-side switch.
27,28	PVDDL	P	Left channel power supply.

Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (* 1)

Symbol	Parameter	Limit	Unit
V_{DD}(PVDDR, PVDDL, AVDD)	Supply voltage	-0.3 to 30	V
V_I (GAIN0, GAIN1, PBTL, FALUT_B, SD_B)	Input voltage	-0.3 to V_{DD}+0.3	V
V_I (PLIMIT)	Input voltage	-0.3 to V_{REG}+0.3	V
V_I (LINN, RINN, LINP, RINP)	Input voltage	-0.3 to 6.5	V
T_A	Operating free-air temperature range	-40 ~ +85	°C
T_J	Operating junction temperature range(* 2)	-40 to +150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
$R_{(LOAD)}$	Minimum load resistance	8 (V_{DD}>15V) 4 (V_{DD}≤15V)	Ω
θ_{JC}	Thermal Resistance (Junction to Case)	8	°C/W
θ_{JA}	Thermal Resistance (Junction to Air)	45	°C/W
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V

(*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

Symbol	Parameter	Test Condition	Specification		Unit
			Min	Max	
V_{DD}	Supply voltage	PVDDL, PVDDR, AVDD	8	26	V
V_{IH}	High level input voltage (GAIN0, GAIN1, PBTL, SD_B)	V_{DD}=24V	2		V
V_{IL}	Low level input voltage (GAIN0, GAIN1, PBTL, SD_B)	V_{DD}=24V		0.8	V
V_{OL}	Low level output voltage (FAULT_B)	V_{DD}=24V, $R_{PULL-HIGH}$=100kΩ		0.8	V
T_A	Operating free-air temperature		-40	85	°C

Electrical Characteristics

T_A = 25℃, V_{DD} = 12V, R_L=8Ω, GAIN=20dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I=0V			1.5	15	mV
I_Q	Quiescent current	SD_B=2V, No load, w/o L/C			25	40	mA
I_{SD}	Shutdown current	SD_B=0.4V, No load			300	450	μA
t_{ON}	Shutdown turn-on time	SD_B=2V			20		ms
t_{OFF}	Shutdown turn-off time	SD_B=0.8V			2		μs
f_{OSC}	Internal oscillation frequency				260		kHz
A	Amplifier gain	GAIN1=0.8V, GAIN0=0.8V			20		dB
		GAIN1=0.8V, GAIN0=2V			26		
		GAIN1=2V, GAIN0=0.8V			32		
		GAIN1=2V, GAIN0=2V			36		
$R_{DS(ON)}$	Drain-Source ON resistance[1]	V_{DD}=12V, I_{OUT}=500mA	High Side		240		mΩ
			Low Side		240		
V_{REG}	Regulator output	I_{VREG} = 100μA, V_{DD}=8~25V		5.25	5.5	5.75	V
t_{DC-DET}	DC detect time				450		ms

(1) Design center value.

Electrical Characteristics

T_A = 25℃, V_{DD} = 24V, R_L=8Ω, GAIN=20dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I=0V			1.5	15	mV
I_Q	Quiescent current	SD_B=2V, No load, w/o L/C			35	50	mA
I_{SD}	Shutdown current	SD_B=0.4V, No load			350	500	μA
t_{ON}	Shutdown turn-on time	SD_B=2V			20		ms
t_{OFF}	Shutdown turn-off time	SD_B=0.8V			2		μs
f_{OSC}	Internal oscillation frequency				260		kHz
A	Amplifier gain	GAIN1=0.8V, GAIN0=0.8V			20		dB
		GAIN1=0.8V, GAIN0=2V			26		
		GAIN1=2V, GAIN0=0.8V			32		
		GAIN1=2V, GAIN0=2V			36		
$R_{DS(ON)}$	Drain-Source ON resistance[1]	V_{DD}=12V, I_{OUT}=500mA	High Side		240		mΩ
			Low Side		240		
V_{REG}	Regulator output	I_{VREG} = 100μA, V_{DD}=8~25V		5.25	5.5	5.75	V
t_{DC-DET}	DC detect time				450		ms

(1) Design center value.

Operating Characteristics

V_{DD}=12V, A_V=20dB, T_A = 25℃ unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
P_O	Output power	THD+N=10%, f=1kHz, R_L=8Ω, V_{DD}=13V			10		W
THD+N	Total harmonic distortion plus noise	V_{DD}=12V, P_O=5W, R_L=8Ω, f=1kHz			0.07		%
$\|K_{SVR}\|$	Supply ripple rejection ration	Input AC-Grounded, C_i=1μF, f=1kHz			70		dB
|SNR|	Signal-to-Noise ratio	A-weighted, THD+N=1%, R_L=8Ω			97		dB
V_n	Output voltage noise	V_{DD}=12V, f=20Hz to 20kHz, Input AC-Grounded, C_i=1μF	No Weight		100		μV_{RMS}
			A-Weighted		80		
|CMRR|	Common mode rejection ratio	V_{DD}=12V, V_{IC}=1V_{PP}	f=120Hz		66		dB
Crosstalk	Channel separation	V_O=1W, f=1kHz, Gain=20dB			102		dB

Operating Characteristics

V_{DD}=24V, A_V=20dB, T_A = 25℃ unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
P_O	Output power	THD+N=10%, f=1kHz, R_L=8Ω, V_{DD}=16V			15		W
THD+N	Total harmonic distortion plus noise	V_{DD}=24V, P_O=10W, R_L=8Ω, f=1kHz			0.08		%
$\|K_{SVR}\|$	Supply ripple rejection ration	Input AC-Grounded, C_i=1μF, f=1kHz			68		dB
|SNR|	Signal-to-Noise ratio	A-weighted, THD+N=1%, R_L=8Ω			99		dB
V_n	Output voltage noise	V_{DD}=12V, f=20Hz to 20kHz, Input AC-Grounded, C_i=1μF	No Weight		100		μV_{RMS}
			A-Weighted		80		
|CMRR|	Common mode rejection ratio	V_{DD}=12V, V_{IC}=1V_{PP}	f=120Hz		66		dB
Crosstalk	Channel separation	V_O=1W, f=1kHz, Gain=20dB			101		dB

Functional Descriptions

Gain Settings

The gain of the VA2208 can be set by GAIN0 and GAIN1 pins. The gain ratios listed in Table 1 are implemented by changing the taps on the feedback resistors in the preamplifier stage.

The input resistance is depended on the gain setting. Since the gain setting is determined by the ratio of the internal feedback resistive network, the variation of the gain is small. But the absolute value of the input resistance may shift by ±20% at the same gain. In actual design cases, 80% of nominal value should be assumed as the input resistance of VA2208 in the input network of whole amplifier.

Gain 1	Gain 0	Gain Ratio	Resistance	Range
1	1	36dB	9kΩ	7.2kΩ~10.8kΩ
1	0	32dB	15kΩ	12kΩ~18kΩ
0	1	26dB	30kΩ	24kΩ~36kΩ
0	0	20dB	60kΩ	48kΩ~72kΩ

Table 1. Gain Setting

Amplifier Input Impedance

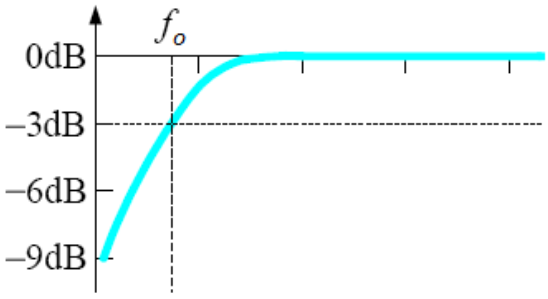


Figure 1. Cut-off Point of High-pass Filter

In most cases, no extra resistor needs to be added on the input of VA2208. The actual input resistor is already determined while selecting the gain. If a single capacitor is used in the input high-pass filter, the cut-off frequency fo may vary with the change of gain setting. The -3dB point of the cut-off frequency can be calculated by the following equation,

$$fo = \frac{1}{2\pi \times R_I \times C_I} \quad \text{(Hz)} \quad \text{Equation (2)}$$

,where the R_I values is given in Table 1.

Shutdown Operation

The VA2208 employs a state of shutdown mode to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier.

Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

VREG Supply

The V_{REG} Supply is used to bias the gates of the output full-bridge upper half MOSFETs. It could be used to supply the PLIMIT pin and related voltage divider circuit. Add at least 1μF capacitor to ground at this pin.

Speaker Protection

Due to the nature of Class D amplifiers, the speakers may have DC current if the audio inputs get DC voltage in any case. An output DC fault will make FAULT_B pin in low state and shuts down the audio amplifier and change the state of output into

Functional Descriptions (cont.)

high impedance.

To resolve the case of DC input, it is good to treat it as very low frequency sine wave much lower than audio band such as 2Hz. Based on this criteria, a DC detect fault shall be issued when the output differential duty-cycle of either channel exceeds 14% for more than 500ms at the same polarity. This feature protects the speakers away from large currents.

The minimum differential input DC voltages required to trigger the DC detection fault are listed in Table 2.

A_V (dB)	V_{IN} (mV, Differential)
36	17
32	28
26	56
20	112

Table 2. DC detect fault threshold

To resume the normal operation, it is necessary to power off the amplifier and then power on, cycling SD_B can not resume normal operation.

Parallel BTL Mode for Mono Operation

VA2208 offers the feature of Stereo operation with two outputs of each channel connected directly. If the PBTL pin (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this mono mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. Parallel BTL mode can increase more output power compare to the stereo mode single channel's output power. For normal BTL operation, connect the PBTL pin to ground.

Short Circuit Protection

VA2208 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULT_B pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD_B pin through the low state.

Connect FAULT_B to SD_B pin, the over current protection will be auto recovery.

Thermal Protection

Thermal protection on the VA2208 prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±20°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 50°C. VA2208 will be back to normal operation at this point with no external system interaction.

Thermal protection fault will not be reported on the FAULT_B terminal.

Power Limit Operation

The voltage at PLIMIT terminal (pin 10) can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from VREG to ground to set the voltage at the PLIMIT terminal. An external reference may also be used if precise limitation is required. Also add a

Functional Descriptions (cont.)

1μF capacitor from this pin to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to power rail. This "virtual" rail is about 5.2 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$

where R_S is the total series resistance including $R_{DS(ON)}$ and any resistance in the output filter. R_L is the load resistance. V_P is the peak amplifier of the output possible within the supply rail.

V_{DD}(V)	R_L(Ω)	PLIMIT(V)	Po@THD+N (W)	
			10%	1%
12	8	0.93	1.328	1.005
12	8	1.107	1.923	1.452
12	8	1.33	2.955	2.118
12	8	1.434	3.527	2.536
24 (Heat Sink)	8	1.612	3.746	2.994
24 (Heat Sink)	8	1.899	5.267	3.999
24 (Heat Sink)	8	2.238	7.069	5.677
24 (Heat Sink)	8	2.683	10.77	8.299
12	4	0.89	1.972	1.518
12	4	1.117	3.123	2.406
12	4	1.285	4.144	3.175
12	4	1.408	5.007	3.839

Table 3. PLIMIT value vs. Output Power

Due to the VREG driving ability limitation, it is not recommended to use this pin to drive other circuits except PLIMIT resistor network. The recommended resistor network is shown on Figure 2.

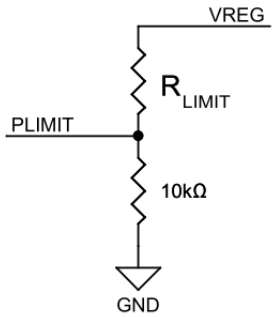


Figure 2. PLIMIT Pin Voltage Divider

Use the simple voltage divider to determine the voltage on PLIMIT pin from VREG pin by the following equation:

$$V_{PLIMIT} = V_{VREG} \frac{10k\Omega}{10k\Omega + R_{LIMIT}}$$

In order to maintain the regulation of VREG pin well please apply higher resistor value such as 10kΩ on low side resistor but should not exceed 50kΩ.

Application Information

Output Filter

Design the VA2208 without the filter if the traces from amplifier to speaker are short (< 10cm), where the speaker is in the same enclosure as the amplifier is a typical application for class D without a filter. Many applications require a ferrite bead filter at least. The ferrite filter reduces EMI above 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies, be aware of its maximum current limitation.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

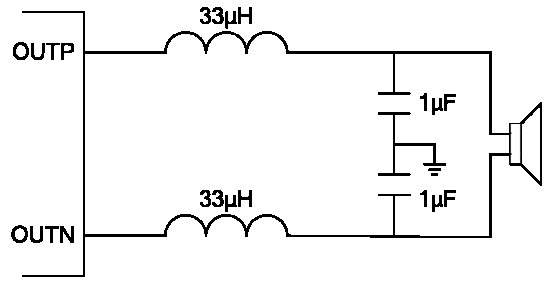
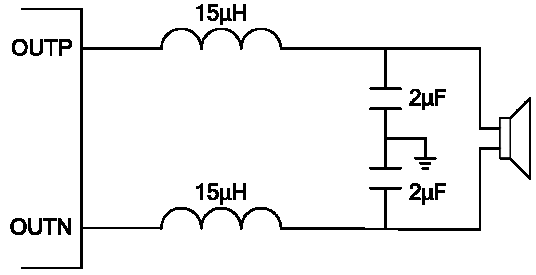


Figure 3. Typical LC Output Filter, Speaker Impedance=8Ω



Figurere 4. Typical LC Output Filter, Speaker Impedance=4Ω

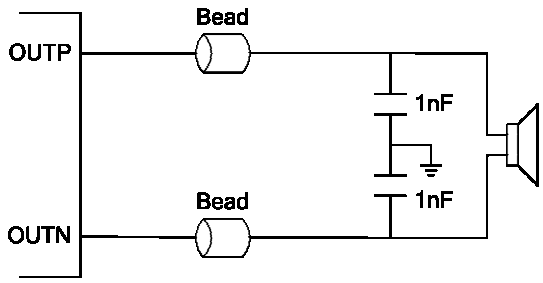


Figure 5. Typical Ferrite Chip Bead Output Filter, Speaker Impedance=8Ω

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the VA2208 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH per amp to avoid this. Also note that smaller inductors than 33µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power.

Like the selection of the inductor in LC filters, the capacitor must be selected carefully, too. A significant change in capacitance at the peak output voltage of the VA2208 will cause increased distortion. LC filter capacitors should be double of DC voltage ratings of the peak application voltage (the power supply voltage) at least. In general, it is strongly recommended using capacitors with good temperature performance like X5R series.

Output Snubbers

In Figure 6, the 330pF capacitors in series with 10Ω resistors connected with the outputs of the VA2208 are snubber circuits. They smooth switching transitions and reduce overshoot and ringing. With these networks, THD+N can be improved at lower power levels and EMC can be reduced 2~4 dB at middle frequencies. They increase quiescent current by 3mA~11mA depends on supply voltage.

Application Information (cont.)

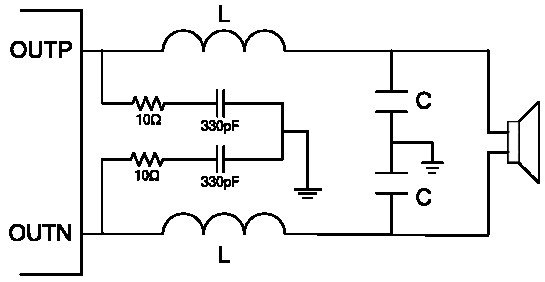


Figure 6. Output Snubber Circuits

Low ESR Capacitors

Low ESR capacitors are high recommended for this application. In general, a practical capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

Boot-Strap Capacitors

The full H-bridge output stages use only MOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22μF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding boot-strap input. Specifically, one 0.22μF capacitor must be connected from OUTP to BSP, and one 0.22μF capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Decoupling Capacitors

VA2208 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improves EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1μF to 10μF, placed as close as possible to PVDDR and PVDDL pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 470μF or greater placed near the audio power amplifier is suggested. The 470μF capacitor also serves as local storage capacitor for supplying current during heavy power output on the amplifier outputs. The PVDDR and PVDDL terminals provide the power to the output transistors, so a 470μF or larger capacitor should be placed by PVDDR and PVDDL terminals as near as possible. A 10μF ceramic capacitor on each PVDDR/PVDDL terminal is also recommended.

PCB Layout Guidelines

The VA2208 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D amplifier switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following guidelines will help to increase EMI/EMC compatibility.

1. The high frequency decoupling capacitors should be placed as close to the PVDDL/PVDDR and AVDD terminals as possible. Large (100μF or greater) bulk power supply decoupling capacitors should be placed near the

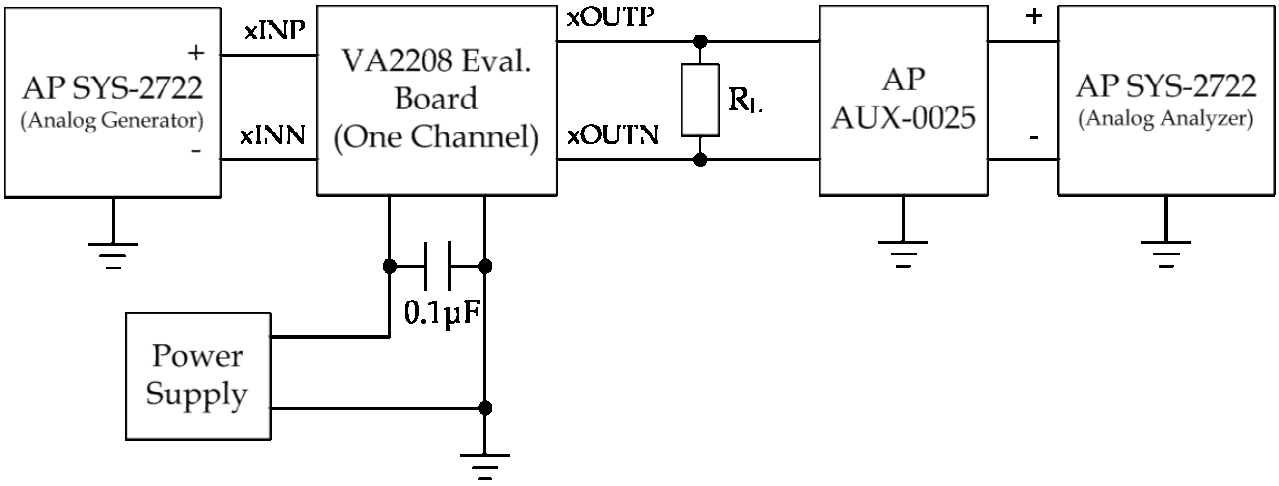
Application Information (cont.)

VA2208 on the PVDDL and PVDDR supplies. Place high-frequency bypass capacitors (such as 1μF MLCC type) should be placed as close to the VREG pin as possible to increase stability. These capacitors can be connected to the thermal pad directly for an excellent ground connection. Consider adding some small, good quality low ESR ceramic capacitors between 1nF and 10nF and larger mid-frequency capacitors of value between 0.1μF and 1μF also of good quality to the PVDDL and PVDDR connections at each end of the chip.

2. Keep the current loop from each of the outputs through the ferrite bead and the small filter capacitor and back to PVSSL/PVSSR as small and tight as possible. The area of this current loop determines its effectiveness as an antenna.
3. Grounding. The AVDD (pin 7) decoupling capacitor should be grounded to analog ground (AGND). The PVDDL/PVDDR decoupling capacitors should connect to PVSSL/PVSSR. Analog ground and power ground should be connected at the thermal pad. The VA2208 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF placed as close as possible to the device AVDD pin, ground connection or star ground for the VA2208.
4. Output Filter. The ferrite EMI filter (Figure 4) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 3) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.

Typical Characteristic

Test Setup Connection Diagram



* Remove all L/C (BEAD) filter components on board before performing all measurements.

** Connection diagram is for one-channel configuration.

Figure No.	Description	Output Load
7	Frequency Response (12V)	8Ω
8	Frequency Response (24V)	
9	THD+N vs. Frequency (12V)	
10	THD+N vs. Frequency (24V)	
11	Crosstalk (12V/1W)	
12	Crosstalk (24V/1W)	
13	Noise FFT	
14	Efficiency	
15	THD+N vs. Output Power (12V)	
16	THD+N vs. Output Power (24V)	
17	PLIMIT voltage vs. Output Power (12V)	
18	Frequency Response (12V)	4Ω
19	THD+N vs. Frequency (12V)	
20	THD+N vs. Output Power (12V)	
21	Crosstalk (12V/1W)	
22	Noise FFT	
23	Efficiency	
24	PLIMIT voltage vs. Output Power	

Typical Characteristic (cont.)

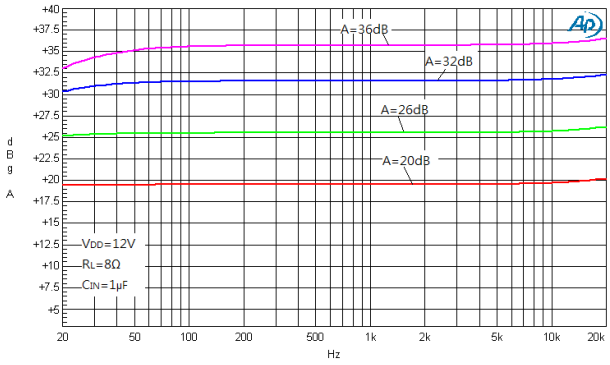


Figure 7. Frequency Response

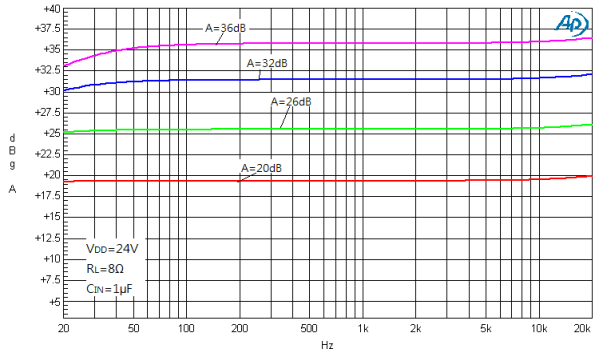


Figure 8. Frequency Response

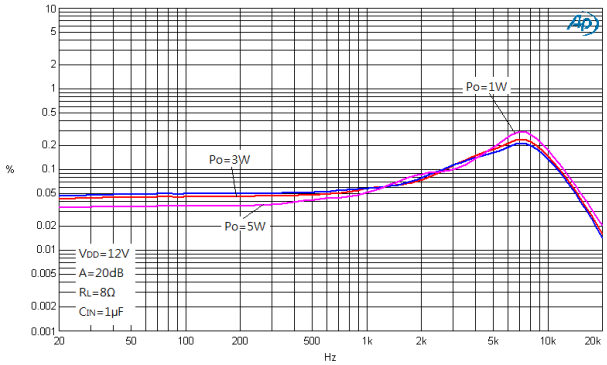


Figure 9. THD+N vs. Frequency

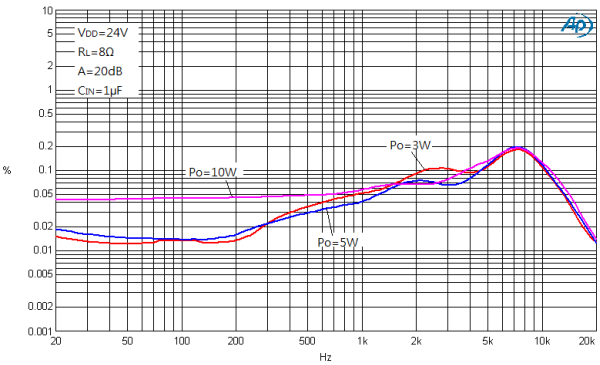


Figure 10. THD+N vs. Frequency

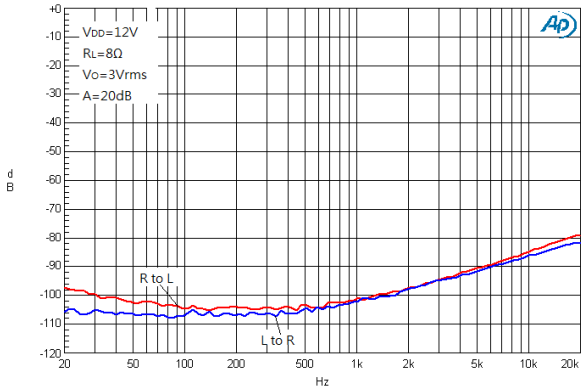


Figure 11. Crosstalk

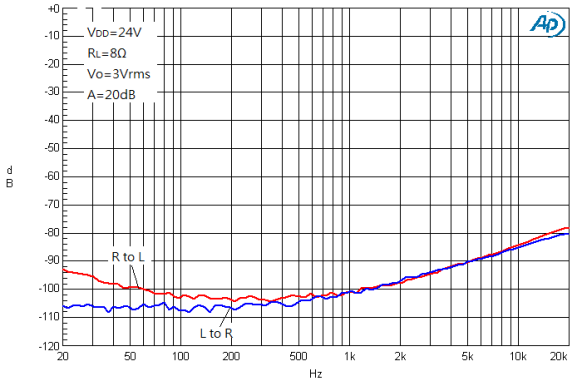


Figure 12. Crosstalk

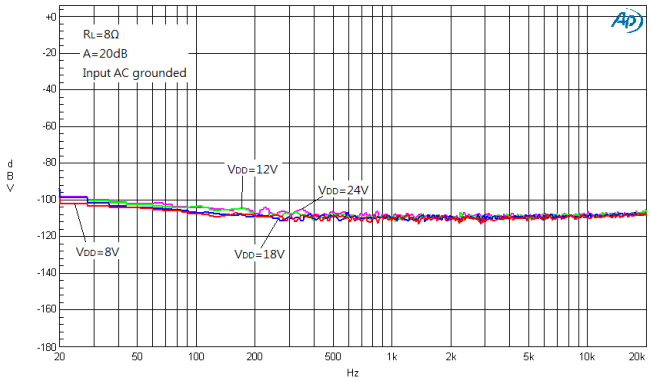


Figure 13. Noise FFT

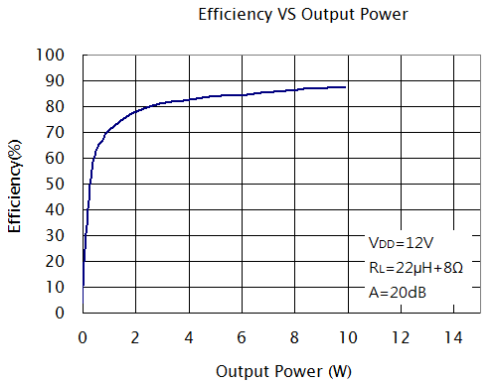


Figure 14. Efficiency

Typical Characteristic (cont.)

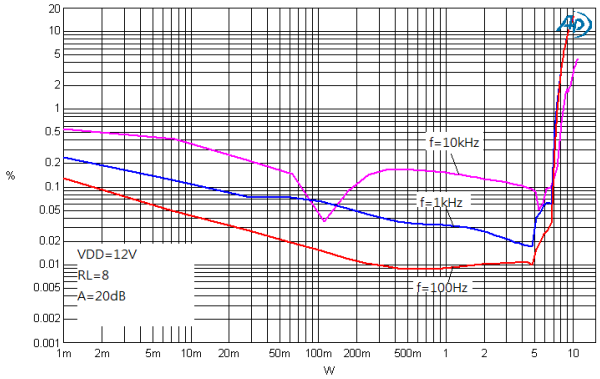


Figure 15. THD+N vs. Output Power

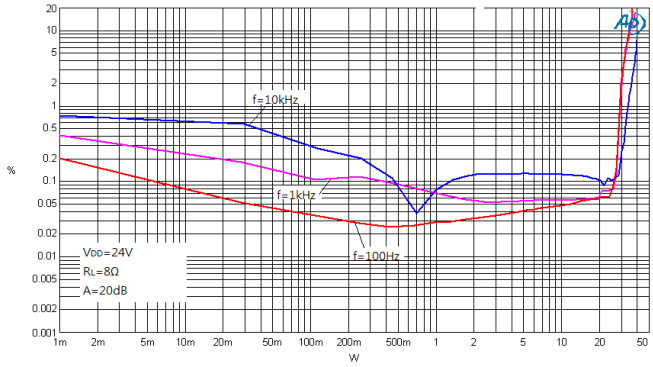


Figure 16. THD+N vs. Output Power

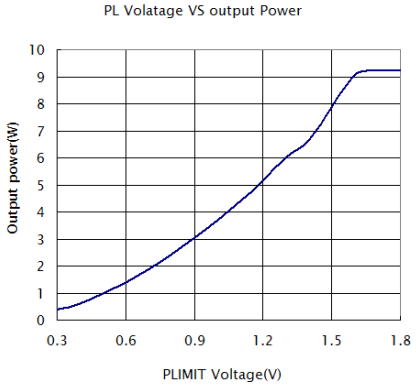


Figure 17. PLIMIT voltage vs. Output Power

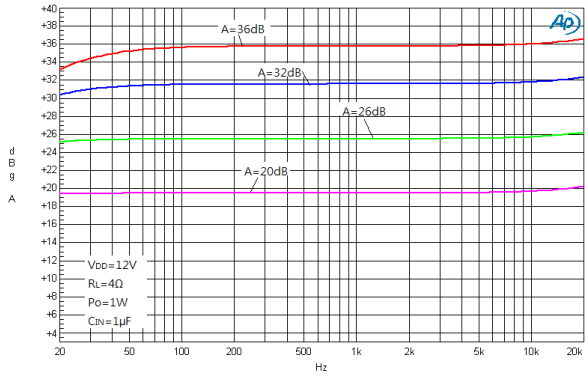


Figure 18. Frequency Response

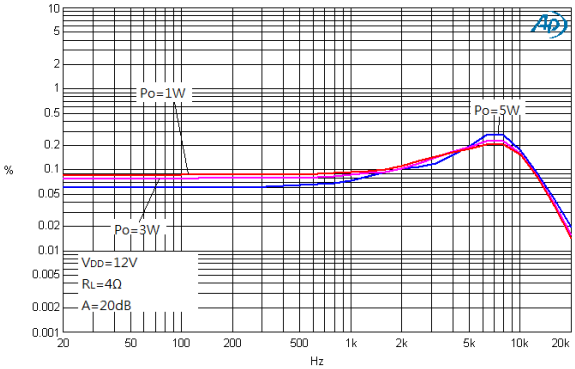


Figure 19. THD+N vs. Frequency

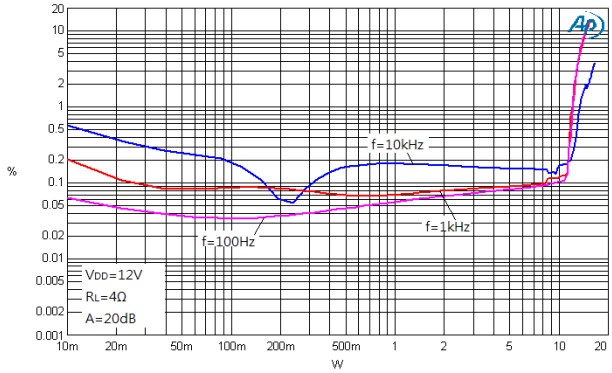


Figure 20. THD+N vs. Output Power

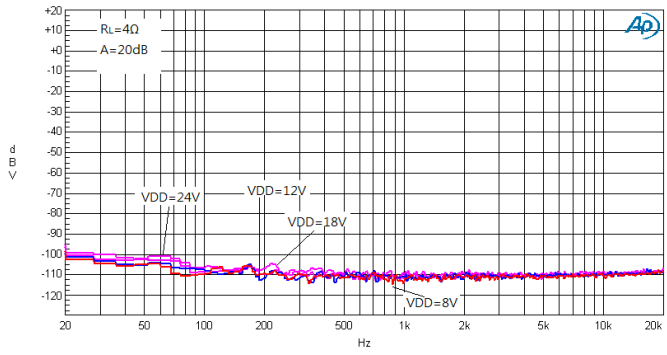


Figure 21. Noise FFT

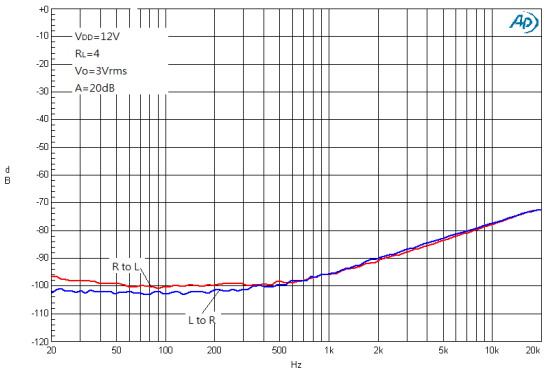


Figure 22. Crosstalk

Typical Characteristic (cont.)

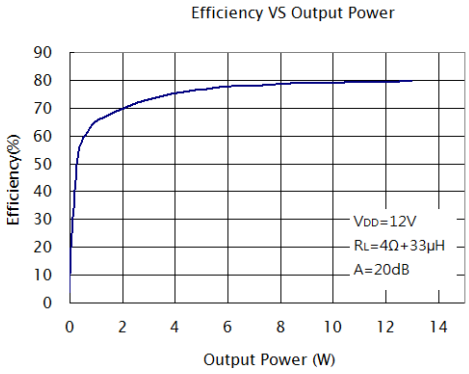


Figure 23. Efficiency

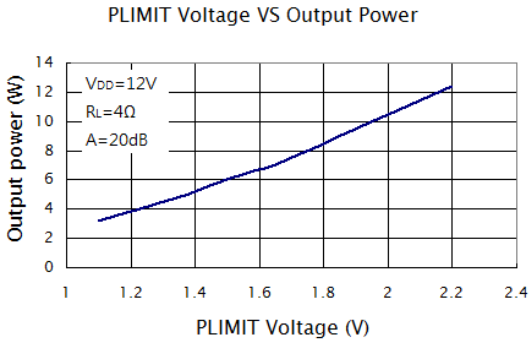


Figure 24. PLIMIT voltage vs. Output Power

Application Circuit

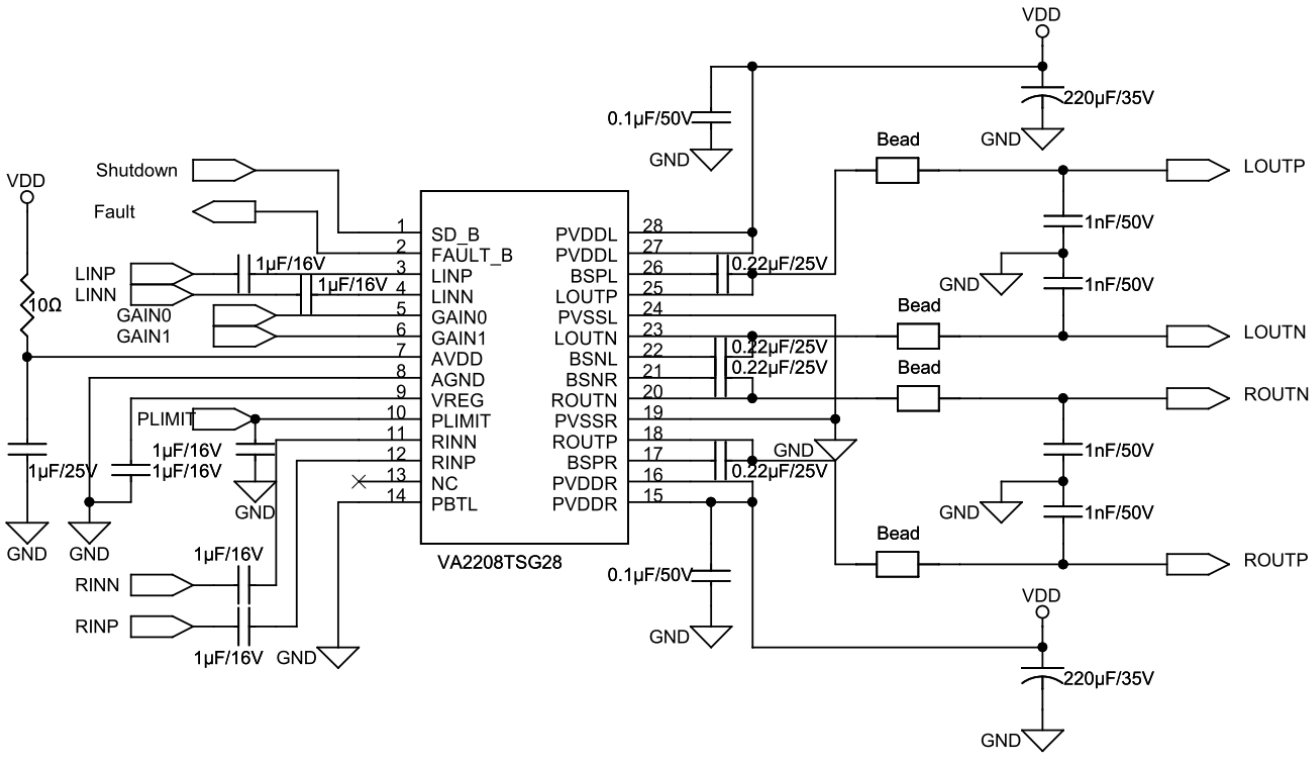


Figure 25. VA2208 Stereo Reference Application Circuit

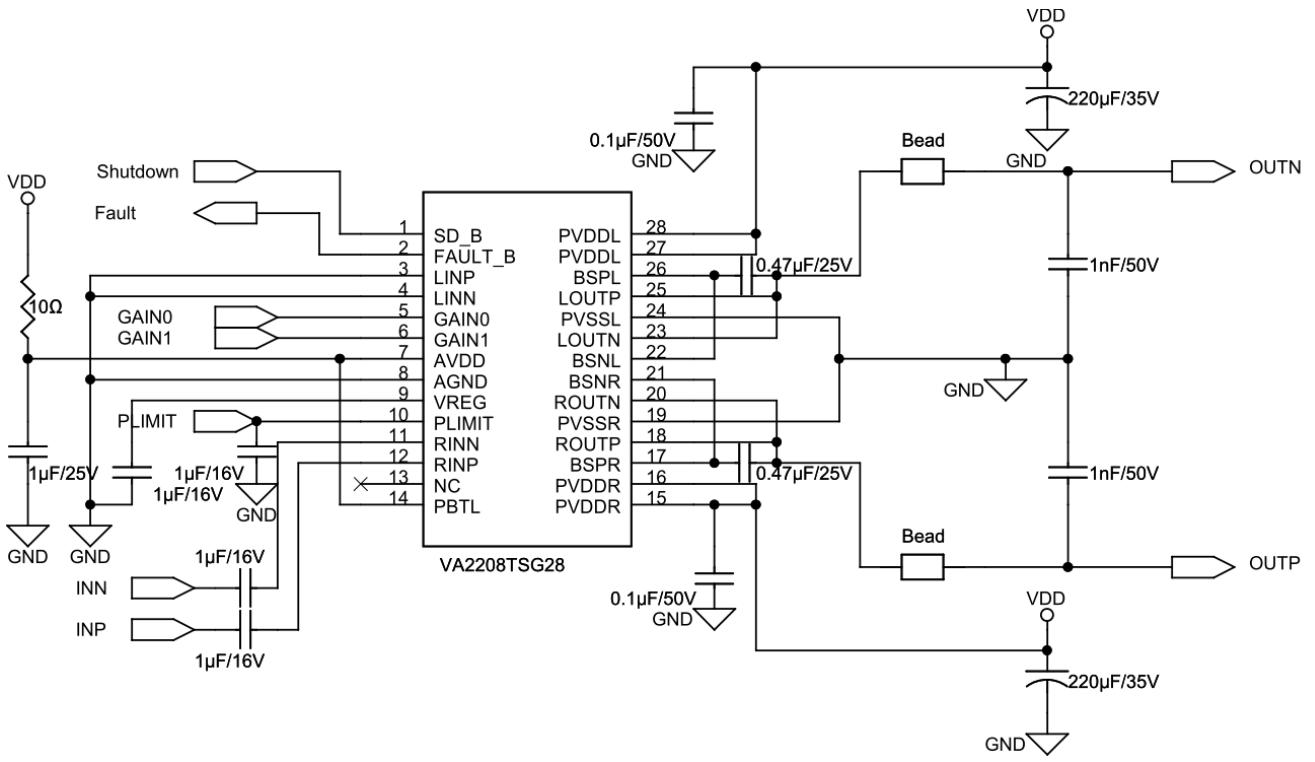
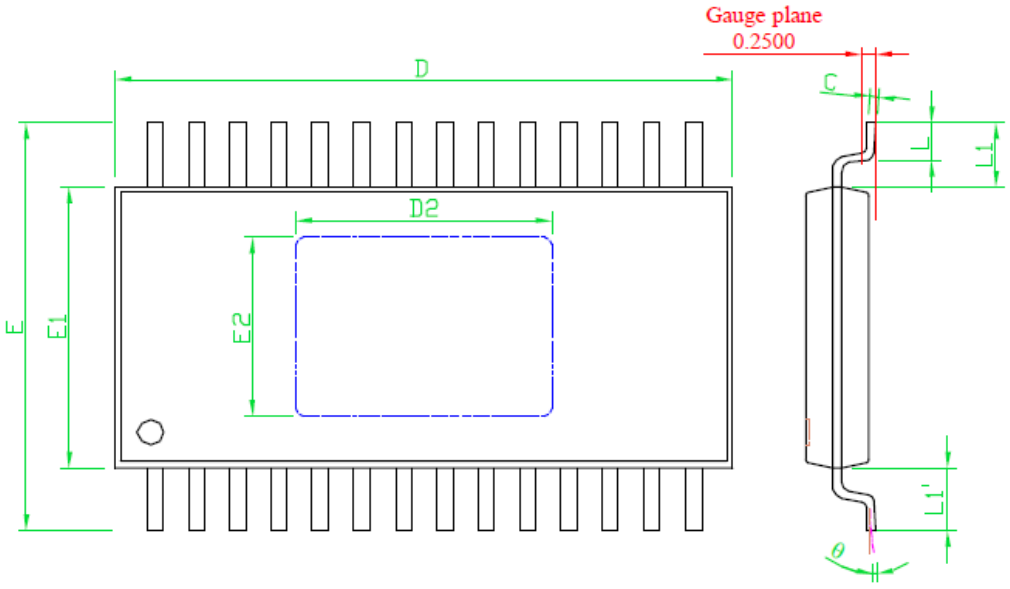
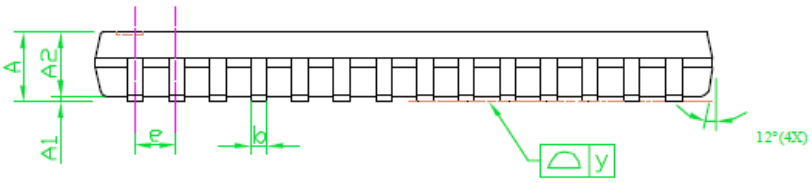


Figure 26. VA2208 Mono Reference Application Circuit

Package Information

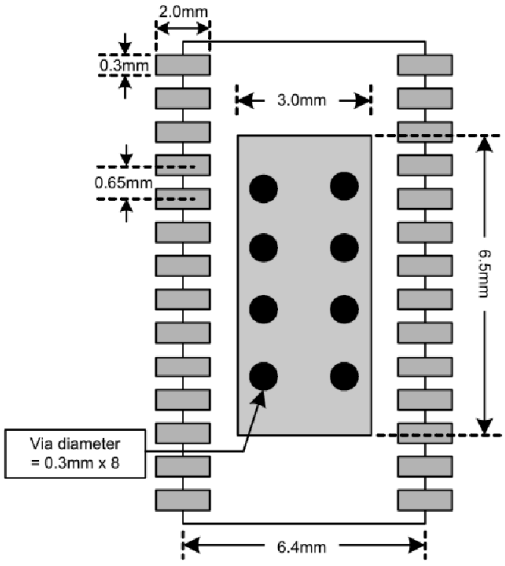
TSSOP-28





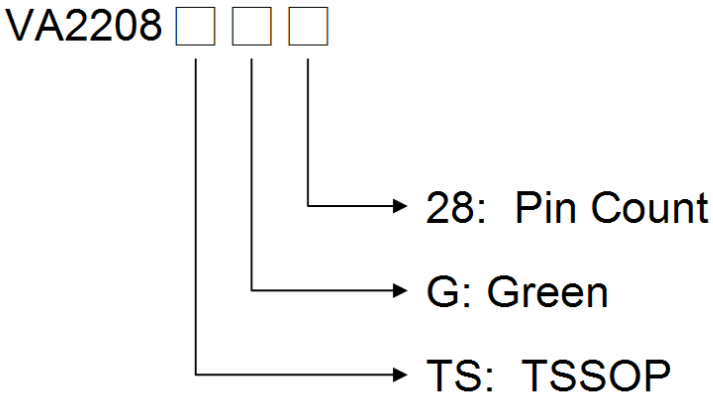
NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE ±0.1 mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. REFER TO JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.15	—	—	0.045
A1	0.00	—	0.10	0.000	—	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
C	0.09	—	0.20	0.004	—	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
D2	3.70	3.80	3.90	0.146	0.150	0.154
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	2.80	2.90	0.106	0.110	0.114
e	—	0.65	—	—	0.026	—
L	0.45	0.60	0.75	0.018	0.024	0.030
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°
⚠ |L1-L1'|	—	—	0.12	—	—	0.005
⚠ L1	1.00REF			0.039REF		



Recommended PCB Layout Land Pattern

Ordering Information



Part No.	Q`ty/Reel
VA2208TSG28	2,500

Contact Information

Viva Electronics Incorporated
10F-1, No. 32, Gaotie 2nd Rd., Zhubei City, Hsinchu County, Taiwan, R.O.C.
Tel: 886-3-6579508
Fax: 886-3-6579509
WWW: http://www.viva-elec.com.tw
Sales: sales@viva-elec.com.tw
FAE Support: fae@viva-elec.com.tw