SC8906 High Efficiency, Synchronous, Buck-Boost Charger Converter with Four Integrated MOSFET

1 Descriptions

SC8906 is a synchronous buck-boost charger converter. Four switches are integrated to simplify the system design. SC8906 employs current-mode control and can support very wide input and output voltage range. It can support applications from 2.7V to 22V VBUS range. It is able to effectively manage charging for 2~4 cell batteries no matter input/output voltage is higher, lower or equal to battery voltage.

SC8906 supports input current limit, DPM (dynamic power management) function, and fast charging detecting. Charging voltage and current limit can be adjusted by external resistor.

SC8906 supports internal current limit, under voltage protection, over voltage protection, output short protection and over temperature protections to ensure safety under abnormal conditions.

The IC is in a 21 pin 4x4 QFN package.

2 Features

- Buck-Boost Battery Charger for 2 to 4 Cell Batteries 4.2V/4.35V/4.4V for 2 and 3 cells, 4.2V/4.35V for 4 cells
- Charging Management: Trickle Charging, CC Charging, CV Charging, Charging Termination, Auto Recharge
- Integrated Switches, 10 mΩ for Q1/4, 20 mΩ for Q2/3
- Wide VBAT Range: 2.7 V to 22 V, 25V sustainable
- Wide VBUS Range: 2.7 V to 22 V, 25V sustainable
- DP / DM Handshaking for Fast Charging Mode
- Safety Timer
- Programmable Current Limit
- NTC Battery Temperature Protection
- Charging Status Indication
- Current Monitor
- Under Voltage Protection, Over Voltage Protection, Over Current Protection
- Short Protection and Thermal Shutdown Protection
- QFN-21 4 x 4 Package

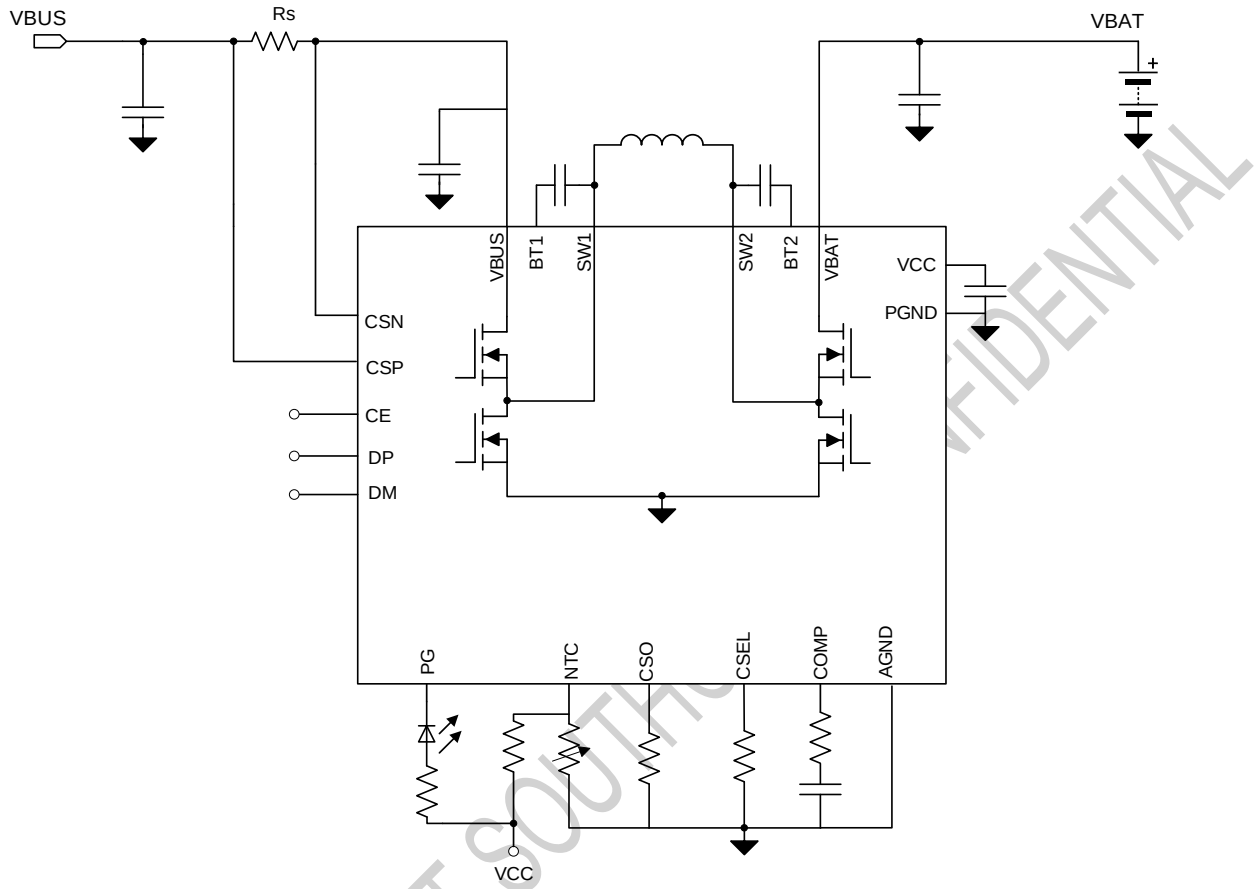
3 Applications

- Power Bank with Fast Charge Function
- USB Power Delivery
- Battery Chargers

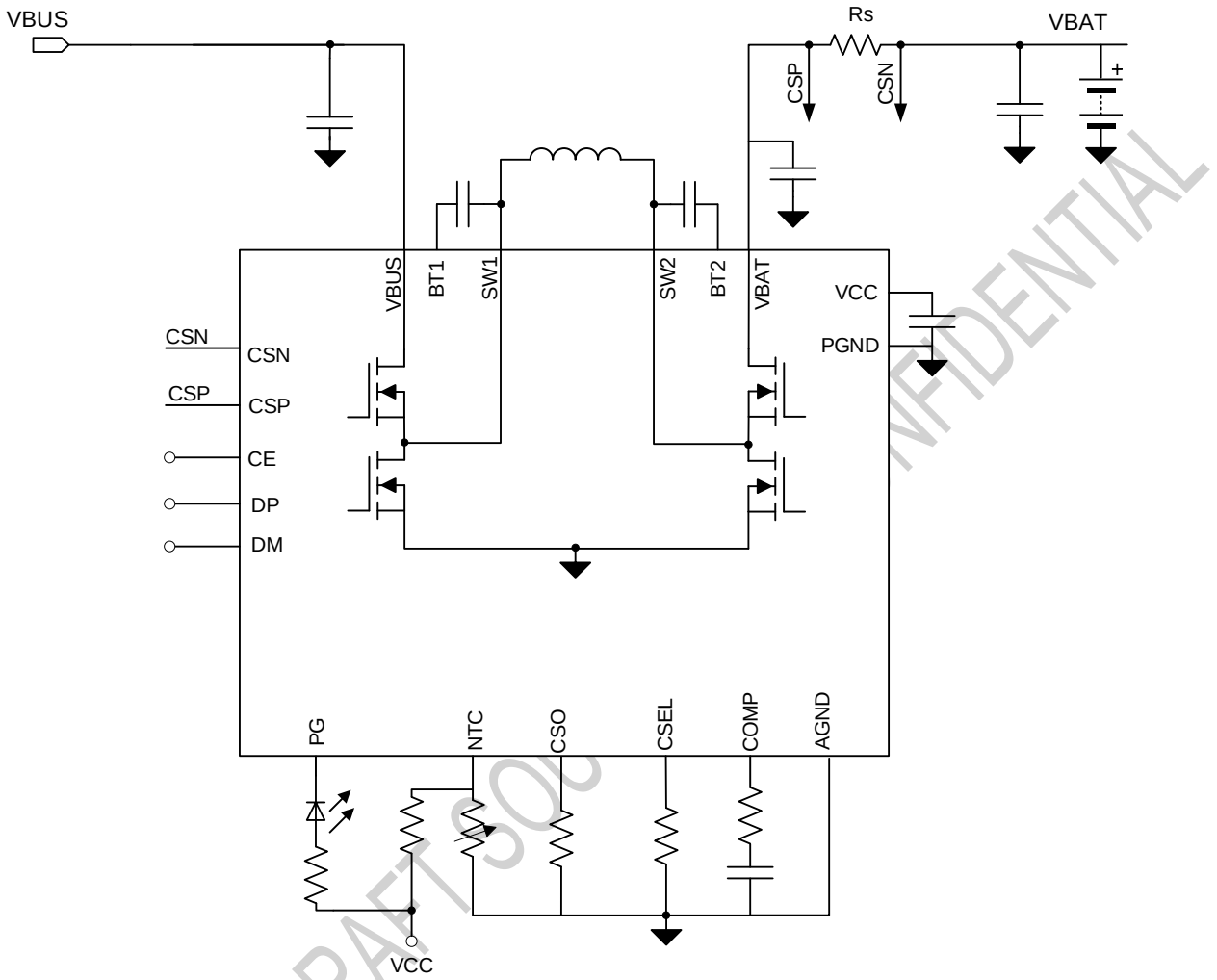
4 Device Information

Part Number	Package	Dimension
SC8906QFER	21 pin QFN	4.0mm x 4.0mm x 0.75mm

5 Typical Application Circuit



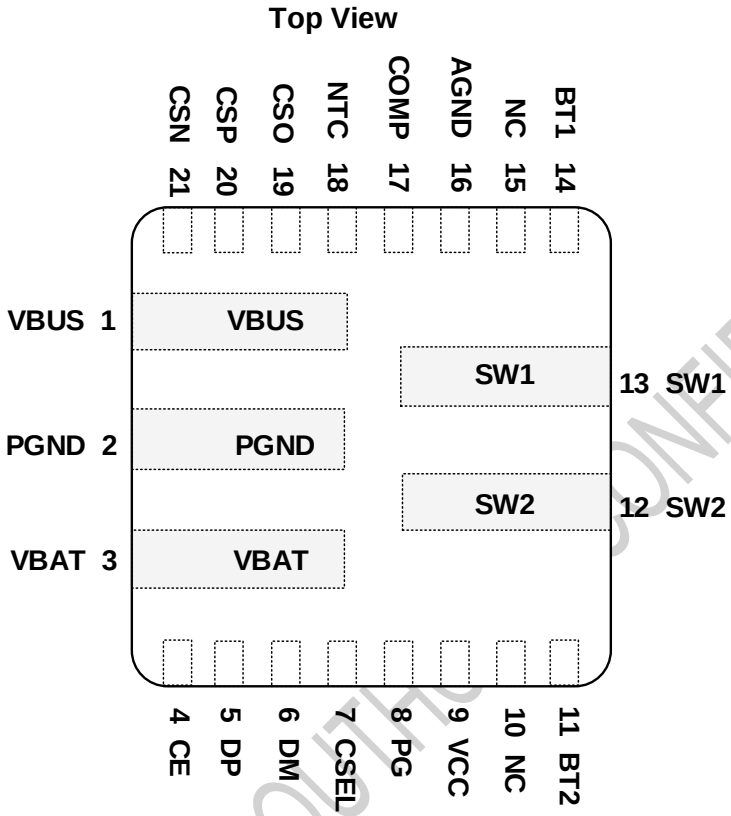
Typical application circuit 1. current sense at VBUS



Typical application circuit 2. current sense at VBAT

Note: User can place current sense resistor at VBUS or VBAT according to application requirement. SC8906 constantly regulates the sense resistor current at setting value, which is decided by CSO resistor. Please refer to **CC charge/Trickle charge** for current setting specification.

6 Terminal Configuration and Functions



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VBUS	I/O	The power input node of the converter in charging mode (DIR = 0), and the power output node of the converter in discharging mode (DIR = 1).
2	PGND	I/O	Power ground. User shall connect PGND and AGND together on PCB.
3	VBAT	I/O	The power output node of the converter in charging mode (DIR = 0), and the power input node of the converter in discharging mode (DIR = 1). Connect these pins to the positive node of battery cells.
4	CE	I	Chip enable pin, active high: pull this pin to logic low to disable the chip. This pin is internally pulled high.
5	DP	I/O	Handshaking for 9V fast charging
6	DM	I/O	Handshaking for 9V fast charging
7	CSEL	I	Use this pin to set the battery termination voltage for charging mode. 2s(4.2V,4.35V,4.4V),3s(4.2V,4.35V,4.4V), 4s (4.2V,4.35V).

8	PG	I	Charging status indication pin. Needs connect to a pull up resistor.
9	VCC	O	Output of an internal regulator. Connect a 2.2 µF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.
10	NC		Must be floating
11	BT2	I	Connect a 100nF ceramic capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
12	SW2	I/O	Switching Node 2. Connect to inductor.
13	SW1	I/O	Switching Node 1. Connect to inductor.
14	BT1	I	Connect a 100nF ceramic capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.
15	NC		Must be floating
16	AGND	I/O	Analog ground. User shall connect PGND and AGND together on PCB.
17	COMP	I	Connect a RC network to compensate the control loop.
18	NTC	I	Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. Short this pin to ground to disable this function
19	CSO	O	Use this pin to monitor the current sensed by CSP and CSN pin. The voltage of CSO is proportional to the sense current.
20	CSP	I	Positive input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between CSP and CSN to sense the current.
21	CSN	I	Negative input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between CSP and CSN to sense the current.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	CE, DP, DM, CSEL, PG, NTC, COMP, CSO	-0.3	5.5	V
	VCC	-0.3	6.5	V
	VBUS, VBAT, CSP, CSN	-0.3	25	V
	SW1, SW2	-0.3	25	V
	BT1, BT2	-0.3	32	V
	CSP to CSN	-10	10	V
	BT1 to SW1, BT2 to SW2	-0.3	6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information(TBD)

THERMAL RESISTANCE(1)		QFN-21 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	TBD	°C/W
θ_{JC}	Junction to case resistance	TBD	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{BUS}	VBUS voltage range	2.7	22	V
V_{BAT}	VBAT voltage range	2.7	22	V

C_{BUS}, C_{BAT}	VBUS Capacitance, VBAT capacitance	30		μF
L	Inductance	2.2	10	μH
R_S	Current Sense Resistor	5	10	mΩ
R_{CSO}	Current Limit setting resistor		64	KΩ

7.5 Electrical Characteristics (TBD)

T_J= 25°C and V_{BUS} = 12V, V_{BAT} = 8V, Rs=10mΩ, Rcso=64kΩ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	Rising edge		2.5		V
		Hysteresis		160		mV
I_Q	Quiescent current into VBUS	VBAT = 8V, VBUS = 5V CE = H, non-switching		1.5		mA
$I_{SHUTDOWN}$	Shutdown current from VBAT	VBAT = 8V, CE = L		5.5		μA
VCC, DIRVER AND POWER SWITCH						
V_{CC}	VCC regulation voltage	VBUS = 9V	4.4	5	5.5	V
		VBUS= 5V, ICC = 30mA	4			V
I_{VCC_LIM}	VCC current limit	VBUS = 9V, VCC = 4V		80		mA
R_{HS_PU}	high side MOS driver pull up resistor			8.9		Ω
R_{LS_PD}	high side MOS driver pull down resistor			1.1		Ω
R_{LS_PU}	low side MOS driver pull up resistor			11.1		Ω
R_{LS_PD}	low side MOS driver pull down resistor			1		Ω
R_{DSon_HS}	High side MOS on resistance			10		mΩ
R_{DSon_LS}	Low side MOS on resistance			20		mΩ
REFERENCE VOLTAGE FOR VBUS						
V_{BUS_OVP}	Absolute OVP threshold for VBUS			23		V
V_{BAT_TRGT}	Battery target voltage	CSEL = floating	17.3	17.4	17.5	V
		CSEL = 300K	16.7	16.8	16.9	V
		CSEL = 150K	13.13	13.2	13.27	V
		CSEL = 80K	12.98	13.05	13.12	V
		CSEL = 40K	12.53	12.6	12.67	V
		CSEL = 20K	8.75	8.8	8.85	V
		CSEL= 10K	8.65	8.7	8.75	V
		CSEL= short	8.35	8.4	8.45	V
V_{BAT_TERM}	Termination threshold over V_{BAT_TRGT}		97%	99.0%	99.5%	
V_{BAT_RECH}	Recharge threshold over V_{BAT_TRGT}			96.5%		
V_{TRK_CH}	Trickle charge threshold over V_{BAT_TRGT}	Rising edge	60%	65%	70%	
		Hysteresis		5%		
V_{BAT_OVP}	OVP threshold, over VBAT target			104%		

V_{BAT_SHORT}	VBAT short threshold, over VBUS voltage	Falling edge		18%		
		Hysteresis		2%		
V_{INREG}	VINREG reference voltage	No Fast-Charging port is recognized by DP/DM		4.5		V
		Fast-Charging port is recognized by DP/DM		8.0		V
CURRENT LIMIT						
I_{BUS_LIM}	IBUS current limit accuracy	I_{BUS} R_S ≥ 20mV, R_{CSO}=64KΩ		-5%	5%	
I_{BUS_TRK}	IBUS trickle charge current	CSEL=GND, VBAT=5V, RS=10mΩ, R_{CSO}=64KΩ		300		mA
I_{term}	Termination current accuracy	VBUS > 15V		50	200	350	mA
		VBUS < 15V	CSEL=2 cells	100	200	300	mA
			CSEL=3 cells	150	300	450	mA
			CSEL=4 cells	200	400	600	mA
I_{OCP}	Internal current limit				10		A
ERROR AMPLIFIER						
Gm_{EA}	Error amplifier gm				0.16		mS
R_{OUT}	Error amplifier output resistance				20		MΩ
I_{SINK_COMP}	COMP sink current				27		μA
I_{SRC_COMP}	COMP source current				16		μA
I_{BIAS_FB}	FB pin input bias current	FB in regulation				50	nA
INDICATION						
I_{SINK_PG}	PG pin sink current	V_{PG} = 0.4V			4		mA
LOGIC CONTROL						
R_{PH}	CE pin internal pull high resistor				2		MΩ
V_{IL}	CE pin input low voltage					0.4	V
V_{IH}	CE pin input high voltage			1.2			V
Frequency						
F_{sw}	Switching Frequency				500		KHZ
DPDM						
V_{DP_SRC}	D+ source voltage				0.6		V
V_{DM_SRC}	D- source voltage				0.6		V
I_{DP_sink}	D+ sink current				100		μA
I_{DM_sink}	D- sink current				100		μA
V_{DAT_REF}	Data detect voltage				0.325		V
NTC						
V_{COLD}	NTC cold temp threshold	Rising, as percentage of VCC			70%		
		Hysteresis (falling)			1%		

V_{HOT}	NTC hot temp threshold	Falling, as percentage of VCC	48%	
		Hysteresis (rising)	2%	
V_{DISNTC}	NTC function disable threshold		0.12	V
THERMAL SHUTDOWN				
T_{SD}	Thermal shutdown temperature (1)		160	°C
	Thermal shutdown hysteresis (1)		30	°C

8 Feature Description

8.1 Chip Enable

The IC is enabled or disabled by CE signal. When CE input is logic high, the IC is enabled; when CE input is logic low, the IC is disabled. The CE pin is pulled high by 2 MΩ resistor internally.

8.2 Charging Mode

When VBUS power up, the IC charges the battery cells according to below typical charging profile. When battery voltage is lower than trickle charge threshold, the IC charges the cells with small charging current; when cell voltage is higher than the threshold, the IC enters into Constant Current charging phase, and charges the cells with constant current set by CSP and CSN pins. When the cell voltage reaches the termination voltage target, the IC enters into Constant Voltage charge phase, and charges the cells with gradually decreased current until the current is lower than termination current threshold. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase. In this phase the IC can either terminate the charging or keep charging the cells.

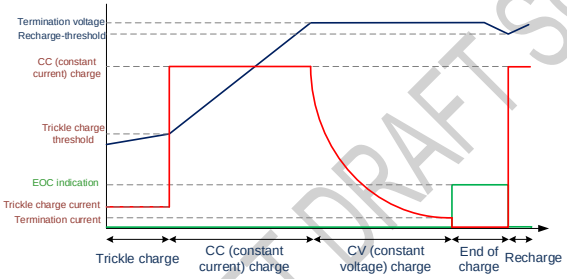


Figure 1 Typical Charging Profile

8.2.1 Trickle Charge

The trickle charge voltage threshold is 60% of battery target voltage. When SC8905 works in trickle charge phase, the IBUS charging current is decided by sense resistor and CSO resistor. The trickle charge current can be calculated as follow:

$$IBUS\_TRICKLE = \frac{96mV*2k\Omega}{Rs*Rcso}$$

where

R_{cso} = Resistor at CSO pin;

R_S = Current sense resistor value to sense IBUS current;

8.2.2 CC Charge (Constant Current Charge)

When cell voltage is higher than the trickle threshold, the IC charges the battery cells with constant current set by IBUS limit. The user can set the IBUS limit through CSO pins resistor respectively as below:

$$IBUS\_LIM = \frac{964mV * 2k\Omega}{Rs*Rcso}$$

In charging mode, the IC regulates the VBUS current which reaches its current limit value.

8.2.3 CV Charge (Constant Voltage Charge)

The battery target voltage can be set by CSEL pin

When the IC is enabled, the IC checks the resistor value at CSEL pin before startup. Below table shows the resistor value to set different charge termination voltages.

Table 1 CSEL pin resistor to set battery voltage

Battery voltage	CSEL resistor
17.4V	open
16.8V	300 kΩ
13.2V	150 kΩ
13.05V	80 kΩ
12.6V	40 kΩ
8.8V	20 kΩ
8.7V	10 kΩ
8.4V	GND

When the battery cell voltage reaches 99% of the cell target voltage, the IC enters into CV charge phase. In this phase, the VBAT voltage is regulated at target value, and the charging current reduces gradually.

8.2.4 EOC (End of Charge)

When all the below voltage condition and current condition for EOC detection are satisfied, the IC enters into EOC phase:

- the cell voltage is higher than 99% of set value
- the IBUS current is lower than termination current.
  When VBUS>15V, termination current is 200mA;
  When VBUS<15V, termination current is decided by CSEL resistor. Termination current is 200mA for 2 cells application, 300mA for 3 cells application and 400mA for 4 cells application respectively.;
- EOC voltage and current lasting for at least 500ms;

SC8906 integrates an open drain output PG pin to indicate status. In EOC phase, the PG pin is floating; In charging phase, the PG pin is internally pulled down.

8.2.5 Recharge

If the IC terminates the charging process after EOC is detected, the battery voltage may drop slowly due to leakage or operation current from battery cells. Once the VBAT voltage drops below 97% of the set voltage, EOC status is clear, and the IC enters into CC charge phase and recharges the battery.

8.2.6 Self-adaptive Charging Current

The IC features dynamic power management. The allowed minimum VBUS operation voltage is VINREG threshold. During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage is pulled low. Once the VBUS voltage drops at VINREG threshold, the IC reduces the charging current automatically and regulates the VBUS voltage at VINREG threshold. VINREG value is adjusted according the DP/DM detecting result.

Table 2 VINREG Threshold

VBUS	VINREG
5V Input	4.5V(Default)
9V Input	8V

8.3 NTC

The SC8906 monitors the battery cells' temperature through NTC pin once VIN is above ULVO threshold. It compares NTC pin voltage with VCC voltage to decide charging status. Once it detects the temperature is below cold or higher than hot threshold, the IC transitions to shutdown mode and temperature status can be read through status registers at the same time. Below shows the NTC operation summary. NTC function can be also disabled through shorting the pin to ground.

Table 3 NTC operation

V_{NTC}	Working Operation
$V_{NTC} > V_{COLD}$	Stop charging
$V_{HOT} < V_{NTC} < V_{COLD}$	Normal charging
$V_{DISNTC} < V_{NTC} < V_{HOT}$	Stop charging
$V_{NTC} < V_{DISNTC}$	NTC disabled

8.4 Safety Timer

When SC8906 starts charging (VBUS above VINREG threshold), a 12-hours safety timer is initiated. Once it detects EOC condition, the IC clears the timer, and it doesn't restart the timer unless recharge phase starts, or VBUS toggle happens.

If the charging cycle doesn't end when the timer expires, the SC8906 stops charging right away. In this case, the SC8906 only restart the timer after VBUS toggles.

8.9 DP/DM Handshaking

The IC supports automatic DP/DM handshaking. Once VBUS is detected in charging mode, the IC initiates the handshaking process at DP / DM lines and requests 9V charging voltage from the adapter.

8.5 VCC Driver Voltage

The IC integrates a VCC regulator so to generate the driver voltage for internal driver circuit. The VCC is supplied by the higher voltage of VBUS and VBAT and is clamped to 5V. Connect a 2.2μF ceramic capacitor from VCC to PGND pin close to the IC.

8.6 Loop Compensation

The internal control loop should be compensated by the resistor and capacitor connected at COMP pin. 10 kΩ resistor and 22 nF capacitor are suggested for most applications. If faster response is required, the user can increase the resistor value but should keep R*C value unchanged. After changing the compensation, check and make sure the loop is stable under target conditions.

8.7 Protections

8.7.1 Over Voltage Protection

The IC supports two mechanisms for over voltage protection.

The first is once the IC detects the VBUS or VBAT voltage is higher than typical 22V, the IC stops switching until the voltage drops below the threshold.

The third is once the IC detects the VBAT voltage is higher than the battery target voltage by 3%, the IC stops switching no matter in charging mode. The IC resumes switching when VBAT voltage recovers.

8.7.2 Over Current Protection

The IC implements internal current limit at 10A. Once the IC detects the inductor current is higher than 10A, it reduces the switching duty cycle, and keeps the inductor current from increasing.

8.7.3 VBAT Short Circuit Protection

The IC supports VBAT short circuit protection in charging mode. During power on, the IC monitors VBAT voltage. Once it detects the VBAT is lower than 18%, it still starts up and limits the VBUS current at fixed 50mA. This helps protect the VBAT short。

8.7.4 Over Temperature Protection

Once the IC detects the chip junction temperature exceeds the threshold (160°C typical), the IC goes into thermal shutdown and stops switching. When the junction temperature falls below typical 130°C, the IC resumes operation.

9 Application Information(TBD)

9.1 Input and Output Capacitor Selection

Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input and output capacitors. Typically, three 22 μF ceramic input capacitors and three 22 μF ceramic output capacitors work for most applications. The input / output capacitors should be places as close to CSP / VBAT pins as possible, and they should be also near the PGND pins or thermal pad.

Capacitors' derating effect under DC bias should be taken into account when selecting the capacitors. Ceramic capacitor normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select 16V or 25V capacitor.

Besides this, high value electrolytic capacitor or tantalum capacitor is recommended to place in parallel with the ceramic capacitors at output to improve the load transient response.

9.2 Inductor Selection

Because the selection of inductor affects the loop stability and the power efficiency, inductor is one of the most important components for the DCDC design.

The IC can work with inductors between 2.2 μH to 10 μH range for most applications. A higher value is suggested to keep the inductor current ripple ≤ 30% of the DC current.

Compared with high value inductor in the same package size, a lower value inductor normally has smaller DC resistance (DCR), so can reduce the conduction power loss, which can be calculated roughly as

$$PL\_DC = IL^2 \cdot DCR$$

IL is the average value of inductor current, and it equals to IBUS or IBAT.

However, besides DCR, the core loss or AC loss of an inductor also affects the power efficiency a lot. The low value inductor causes large inductor current ripple, thus high core loss or AC loss, so it is not always the low value inductor supports the higher efficiency.

Since the core loss is related to the inductor material type, and normally the inductor vendors don't provide the core loss data, it is very difficult to suggest what inductor value can result in higher efficiency. As a rule of thumb, high value inductor like 4.7 μH to 10 μH is recommended for applications where the difference between input voltage and output voltage is big, such as 5V to 20V; while for those applications where input voltage is close to output voltage, but large current is on power path, low value inductor like 2.2 μH is suggested.

For applications where efficiency or thermal dissipation is very important, it is highly suggested that the user chooses the inductor in larger package size for lower DCR, and also tests the efficiency with different inductor values, so to find the best combination to achieve the highest efficiency.

The saturation current is another important parameter when selecting the inductor. The inductance can decrease 20% to 35% when the current approaches saturation level, so the user should make sure the saturation current is higher than the inductor peak current during the operation.

The inductor peak current can be calculated by below formula.

$$IL\_peak = IBAT + \frac{VBAT \cdot (VBUS - VBAT \cdot \eta)}{2 \cdot fsw \cdot L \cdot VBUS} \quad (VBUS \geq VBAT)$$

$$IL\_peak = IBUS + \frac{VBUS \cdot (VBAT - VBUS)}{2 \cdot fsw \cdot L \cdot VBAT \cdot \eta} \quad (VBUS < VBAT)$$

where IBAT is the battery current at VBAT side, and can be calculated as

$$IBAT = \frac{VBUS \cdot IBUS}{\eta \cdot VBAT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

The peak inductor current in charging mode can be calculated as

$$I_{L\_peak} = I_{BAT} + \frac{V_{BAT}\cdot(V_{BUS}-V_{BAT})}{2\cdot f_{sw}\cdot L\cdot V_{BUS}\cdot\eta} \quad (V_{BUS}>V_{BAT})$$

$$I_{L\_peak} = I_{BUS} + \frac{V_{BUS}\cdot(V_{BAT}-V_{BUS}\cdot\eta)}{2\cdot f_{sw}\cdot L\cdot V_{BAT}} \quad (V_{BUS}\leq V_{BAT})$$

where IBAT is the battery charging current at VBAT side, and can be calculated as

$$I_{BAT} = \frac{V_{BUS}\cdot I_{BUS}\cdot\eta}{V_{BAT}}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

9.3 Current Sense Resistor

The R_S in the typical application circuit are current sense resistors for current limit functions.

A high resistor value can result in high current limit / monitor accuracy but causes high conductor loss. Typically, 10 mΩ is recommended. But for applications where efficiency is more important than accuracy, lower value is suggested.

When selecting the current sense resistor, its power rating and temperature coefficient should also be considered.

The power dissipation can be roughly calculated as $P=I^2R$, where I is the highest current flowing through it. The power rating should be higher than the calculated value.

The resistor value varies with temperature and the variation is decided by its temperature coefficient. If high accuracy of limit or monitor is required, select as lower temperature coefficient as possible.

9.4 Snubber Circuit

The RC snubber circuits at SWx nodes as shown below can be used to suppress the switching spike so to improve the EMC performance. A typical snubber circuit is composed by a 2.2Ω resistor and 1nF capacitor. The user can reduce the resistance and increase the capacitance further to improve the EMC. However, because it often causes higher switching loss and results in lower efficiency, it is suggested not to add snubber circuits unless necessary.

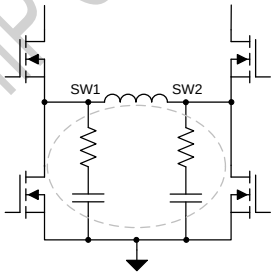


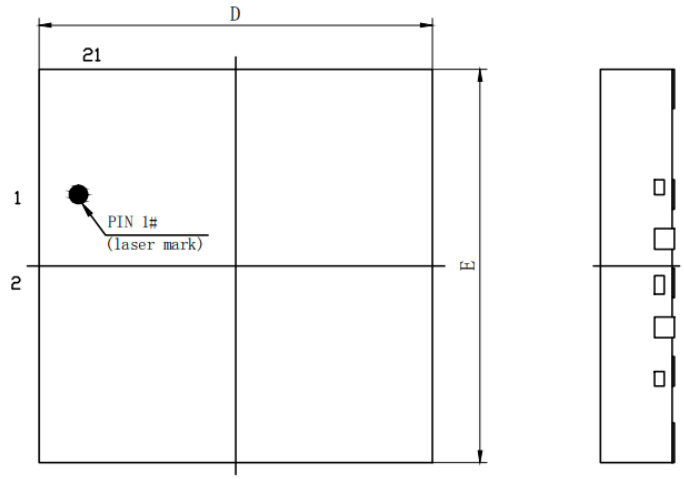
Figure 15 Snubber circuit at SWx nodes

The IC also allows user adding a driver resistor for the low side MOSFET at VBUS side to slow down the switching, thus to reduce the switching spike improve the EMC performance. However, because the driver resistor also causes higher switching loss and thus lower efficiency, it is suggested not to add the driver resistor unless necessary.

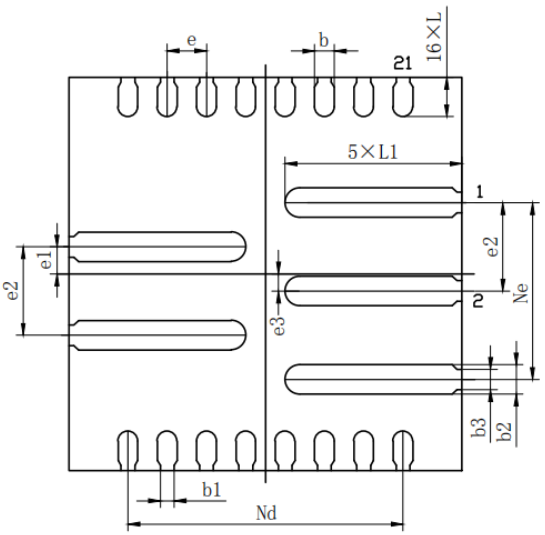
If the driver resistor is needed, a 0603 resistor should be used, and it should be placed near the IC

MECHANICAL DATA

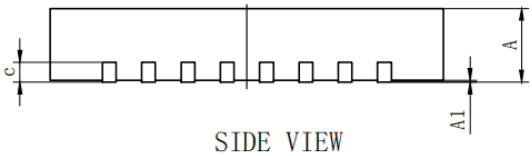
QFN-21 (4x4x0.75)



TOP VIEW



BOTTOW VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
b2	0.25	0.30	0.35
b3	0.21REF		
c	0.203REF		
D	3.90	4.00	4.10
e	0.40BSC		
e1	0.275BSC		
e2	0.90BSC		
e3	0.175BSC		
E	3.90	4.00	4.10
Nd	2.80BSC		
Ne	1.80BSC		
L	0.35	0.40	0.45
L1	1.75	1.80	1.85

RECOMMENDED FOOTPRINT

QFN-21 (4x4x0.75) (Unit: mm)