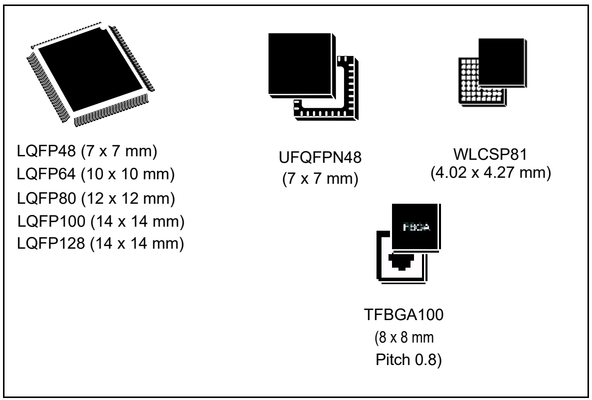
STM32G484xE

Arm® Cortex®-M4 32-bit MCU+FPU, 170 MHz / 213DMIPS, 128 KB SRAM, rich analog, math acc, 184 ps 12 chan Hi-res timer, AES

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator) allowing 0-wait-state execution from Flash memory, frequency up to 170 MHz with 213 DMIPS, MPU, DSP instructions
- Operating conditions:
  - V_{DD}, V_{DDA} voltage range: 1.71 V to 3.6 V
- Mathematical hardware accelerators
  - CORDIC for trigonometric functions acceleration
  - FMAC: filter mathematical accelerator
- Memories
  - 512 Kbytes of Flash memory with ECC support, two banks read-while-write, proprietary code readout protection (PCROP), securable memory area, 1 Kbyte OTP
  - 96 Kbytes of SRAM, with hardware parity check implemented on the first 32 Kbytes
  - Routine booster: 32 Kbytes of SRAM on instruction and data bus, with hardware parity check (CCM SRAM)
  - External memory interface for static memories FSMC supporting SRAM, PSRAM, NOR and NAND memories
  - Quad-SPI memory interface
- Reset and supply management
  - Power-on/power-down reset (POR/PDR/BOR)
  - Programmable voltage detector (PVD)
  - Low-power modes: sleep, stop, standby and shutdown
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz oscillator with calibration
  - Internal 16 MHz RC with PLL option (± 1%)
  - Internal 32 kHz RC oscillator (± 5%)
- Up to 107 fast I/Os
  - All mappable on external interrupt vectors
  - Several I/Os with 5 V tolerant capability
- Interconnect matrix
- 16-channel DMA controller
- 5 x 12-bit ADCs 0.25 µs, up to 42 channels. Resolution up to 16-bit with hardware oversampling, 0 to 3.6 V conversion range
- 7 x 12-bit DAC channels
  - 3 x buffered external channels 1 MSPS
  - 4 x unbuffered internal channels 15 MSPS
- 7 x ultra-fast rail-to-rail analog comparators
- 6 x operational amplifiers that can be used in PGA mode, all terminals accessible
- Internal voltage reference buffer (VREFBUF) supporting three output voltages (2.048 V, 2.5 V, 2.95 V)
- 17 timers:
  - HRTIM (Hi-Resolution and complex waveform builder): 6 x16-bit counters, 184 ps resolution, 12 PWM
  - 2 x 32-bit timer and 2 x 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 3 x 16-bit 8-channel advanced motor control timers, with up to 8 x PWM



This is information on a product in full production.

  - channels, dead time generation and emergency stop
  - 1 x 16-bit timer with 2 x IC/OCs, one OCN/PWM, dead time generation and emergency stop
  - 2 x 16-bit timers with IC/OC/OCN/PWM, dead time generation and emergency stop
  - 2 x watchdog timers (independent, window)
  - 1 x SysTick timer: 24-bit downcounter
  - 2 x 16-bit basic timers
  - 1 x low-power timer
- Calendar RTC with alarm, periodic wakeup from stop/standby
- Communication interfaces
  - 3 x FDCAN controller supporting flexible data rate
  - 4 x I^{2}C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from stop
  - 5 x USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - 1 x LPUART
  - 4 x SPIs, 4 to 16 programmable bit frames, 2 x with multiplexed half duplex I^{2}S interface
  - 1 x SAI (serial audio interface)
  - USB 2.0 full-speed interface with LPM and BCD support
  - IRTIM (infrared interface)
  - USB Type-C™ /USB power delivery controller (UCPD)
- True random number generator (RNG)
- CRC calculation unit, 96-bit unique ID
- AES: 128/256-bit key encryption hardware accelerator
- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell™

Table 1. Device summary

Reference	Part number
STM32G484xE	STM32G484CE, STM32G484ME, STM32G484RE, STM32G484QE, STM32G484VE

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32G484xE microcontrollers.

This document should be read in conjunction with the reference manual RM0440 “STM32G4 Series advanced Arm® 32-bit MCUs”. The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M4 core, refer to the Cortex®-M4 technical reference manual, available from the www.arm.com website.

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[a] Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32G484xE devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core. They operate at a frequency of up to 170 MHz.

The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm single-precision data-processing instructions and all the data types. It also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (512 Kbytes of Flash memory, and 128 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI Flash memory interface, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The devices also embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, securable memory area and proprietary code readout protection.

The devices embed peripherals allowing mathematical/arithmetic function acceleration (CORDIC for trigonometric functions and FMAC unit for filter functions).

They offer five fast 12-bit ADCs (5 Msps), seven comparators, six operational amplifiers, seven DAC channels (3 external and 4 internal), an internal voltage reference buffer, a low-power RTC, twothree general-purpose 32-bit timers, three 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and one 16-bit low-power timer, and high resolution timer with 184 ps resolution.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Four SPIs multiplexed with two half duplex I2Ss
- Three USARTs, two UARTs and one low-power UART.
- Three FDCANs
- One SAI
- USB device
- UCPD

The STM32G484xE devices embed an AES.

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported including an analog independent supply input for ADC, DAC, OPAMPs and comparators. A V_{BAT} input allows backup of the RTC and the registers.

The STM32G484xE family offers 8 packages from 48-pin to 128-pin.

Table 2. STM32G484xE features and peripheral counts

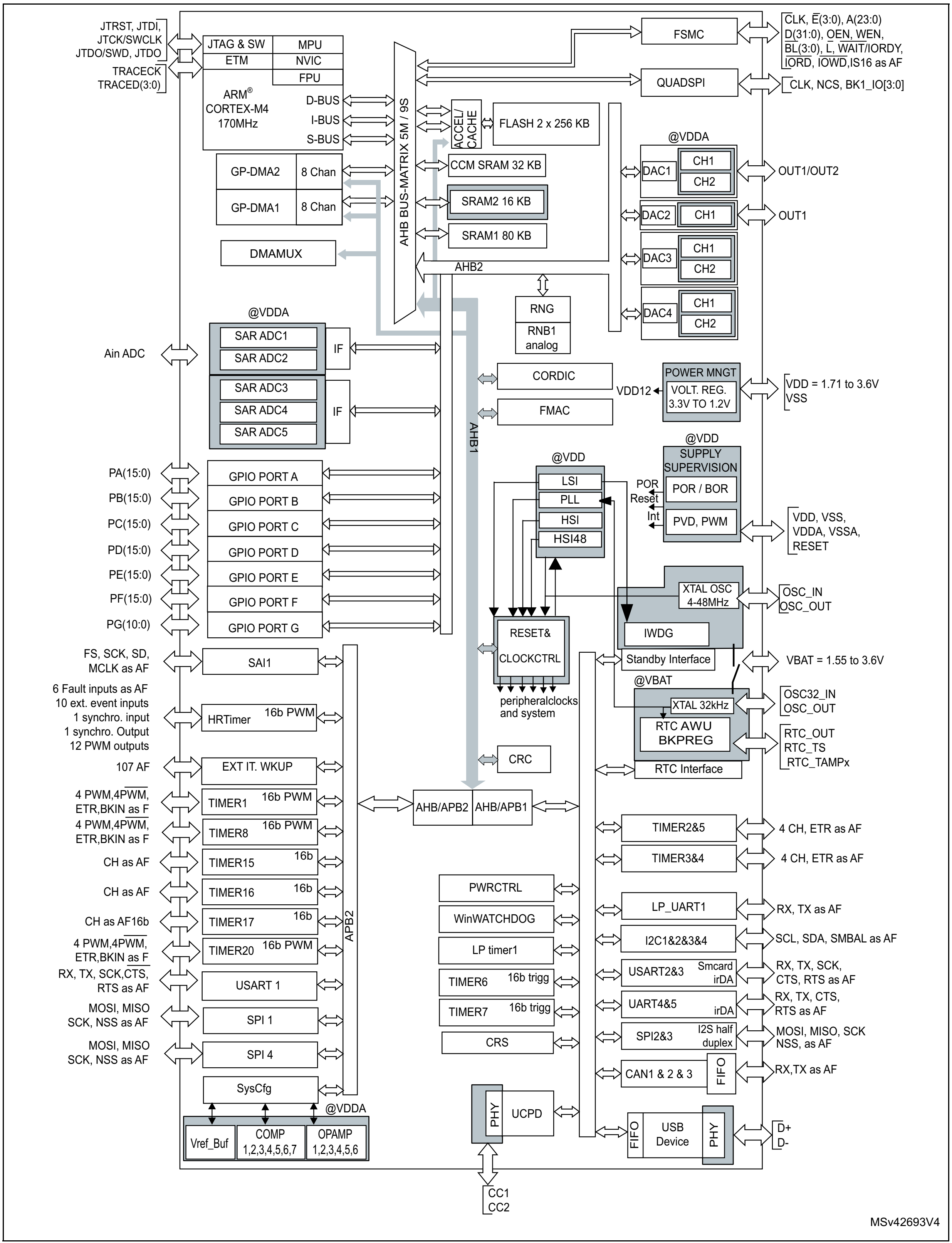
Peripheral		STM32G484 CE	STM32G484 RE	STM32G484 ME	STM32G484 VE	STM32G484 QE
Flash memory		512 KB				
SRAM		128 (80 + 16+ 32) KB				
External memory controller for static memories (FSMC)		No		Yes	Yes[1]	Yes
QUADSPI		1				
Timers	Advanced motor control	3 (16-bit)				
	HRTIM	1				
	General purpose	5 (16-bit) 2 (32-bit)				
	Basic	2 (16-bit)				
	Low power	1 (16-bit)				
	SysTick timer	1				
	Watchdog timers (independent, window)	2				
Comm. interfaces	SPI(I2S)[2]	3 (2)		4 (2)		
	I^2C	4				
	USART	3				
	UART	0	2			
	LPUART	1				
	FDCANs	3				
	USB device	Yes				
	UCPD	Yes				
	SAI	Yes				
RTC		Yes				
Tamper pins		2		3		
Random number generator		Yes				
AES		Yes				
CORDIC		Yes				
FMAC		Yes				
GPIOs		38 in LQFP48 42 in UFQFPN48	52	67 in WLCSP81 66 in LQFP80	86	107
Wakeup pins		3	4	4	5	5

Table 2. STM32G484xE features and peripheral counts (continued)

Peripheral	STM32G484 CE	STM32G484 RE	STM32G484 ME	STM32G484 VE	STM32G484 QE
12-bit ADCs Number of channels	5				
	20 in LQFP48 21 in UFQFPN48	26	42 in WLCSP81 41 in LQFP80	42	42
12-bit DAC Number of channels	4 7 (3 external + 4 internal)				
Internal voltage reference buffer	Yes				
Analog comparator	7				
Operational amplifiers	6				
Max. CPU frequency	170 MHz				
Operating voltage	1.71 V to 3.6 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 125 °C				
Packages	LQFP48/ UFQFPN48	LQFP64	WLCSP81 LQFP80	LQFP100/ TFBGA100	LQFP128

1. For the LQFP100 package, only FMC bank1 and NAND bank are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 chip select.
2. The SPI2/3 interfaces can work in an exclusive way in either the SPI mode or the I2S audio mode.

Figure 1. STM32G484xE block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M4 core with FPU

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of the MCU implementation, with a reduced pin count and with low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU 32-bit RISC processor features an exceptional code-efficiency, delivering the expected high-performance from an Arm core in a memory size usually associated with 8-bit and 16-bit devices.

The processor supports a set of DSP instructions which allows an efficient signal processing and a complex algorithm execution. Its single precision FPU speeds up the software development by using metalanguage development tools to avoid saturation.

With its embedded Arm core, the STM32G484xE family is compatible with all Arm tools and software.

Figure 1 shows the general block diagram of the STM32G484xE devices.

3.2 Adaptive real-time memory accelerator (ART accelerator)

The ART accelerator is a memory accelerator that is optimized for the STM32 industry-standard Arm® Cortex®-M4 processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 8 protected areas, which can be divided in up into 8 subareas each. The protection area sizes range between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The STM32G484xE devices feature 512 kbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported.

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels of protection are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected
  - Level 2: chip readout protection; the debug features (Cortex-M4 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only and it can only be reached by the STM32 CPU as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.
- Securable memory area: a part of Flash memory can be configured by option bytes to be securable. After reset this securable memory area is not secured and it behaves like the remainder of main Flash memory (execute, read, write access). When secured, any access to this securable memory area generates corresponding read/write error. Purpose of the Securable memory area is to protect sensitive code and data (secure keys storage) which can be executed only once at boot, and never again unless a new reset occurs.

The Flash memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register
- 1 Kbyte (128 double word) OTP (one-time programmable) bytes for user data. The OTP area is available in Bank 1 only. The OTP data cannot be erased and can be written only once.

3.5 Embedded SRAM

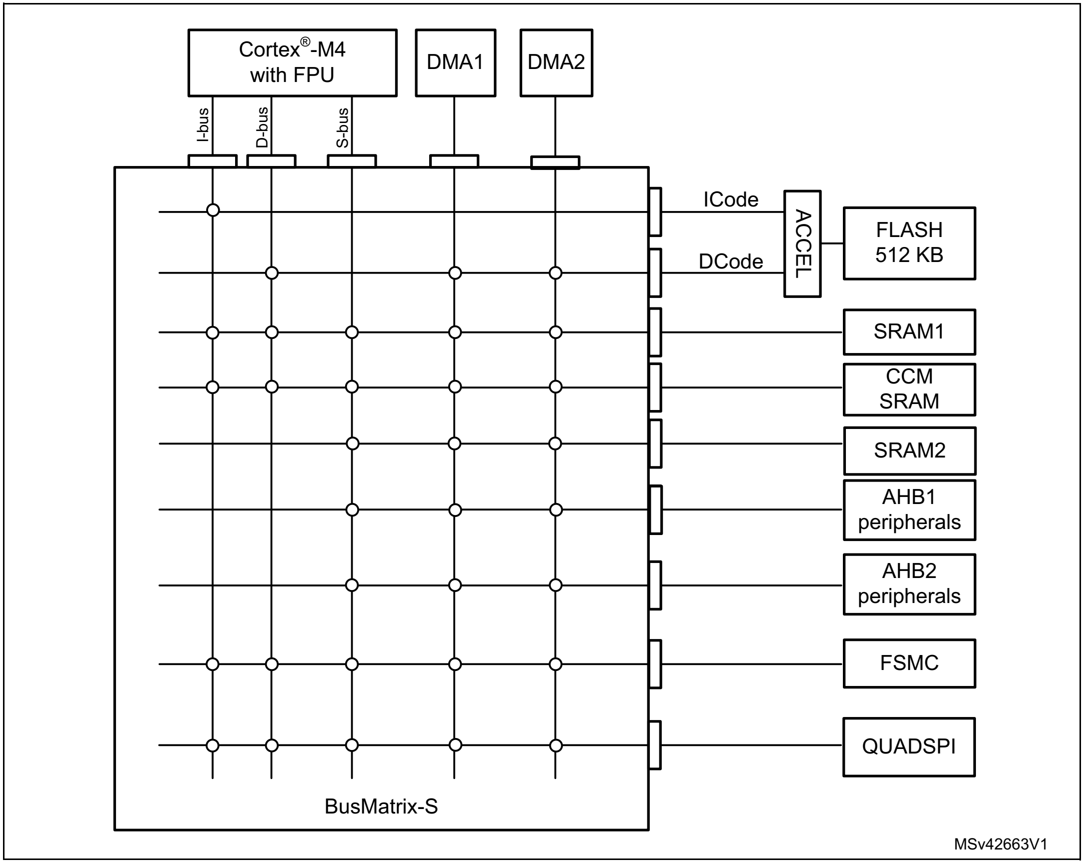
STM32G484xE devices feature 128 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 80 Kbytes mapped at address 0x2000 0000 (SRAM1). The CM4 can access the SRAM1 through the System Bus. The first 32 Kbyte of SRAM1 support hardware parity check.
- 16 Kbytes mapped at address 0x2001 4000 (SRAM2). The CM4 can access the SRAM2 through the System bus. SRAM2 can be retained in standby modes.
- 32 Kbytes mapped at address 0x1000 0000 (CCM SRAM). It is accessed by the CPU through I-Code/D-Code bus for maximum performance.
  It is also aliased at 0x2001 8000 address to be accessed by all masters (CPU, DMA1, DMA2) through SBUS contiguously to SRAM1 and SRAM2. The CCM SRAM supports hardware parity check and can be write-protected with 1 Kbyte granularity.
- The memory can be accessed in read/write at max CPU clock speed with 0 wait states.

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, FSMC, QUADSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Boot modes

At startup, a BOOT0 pin (or nBOOT0 option bit) and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PB8-BOOT0 pin or from an nBOOT0 option bit depending on the value of a user nBOOT_SEL option bit to free the GPIO pad if needed.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, and USB through the DFU (device firmware upgrade).

3.8 CORDIC

The CORDIC provides hardware acceleration of certain mathematical functions, notably trigonometric, commonly used in motor control, metering, signal processing and many other applications.

It speeds up the calculation of these functions compared to a software implementation, allowing a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

Cordic features

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: Sine, Cosine, Sinh, Cosh, Atan, Atan2, Atanh, Modulus, Square root, Natural logarithm
- Programmable precision up to 20-bit
- Fast convergence: 4 bits per clock cycle
- Supports 16-bit and 32-bit fixed point input and output formats
- Low latency AHB slave interface
- Results can be read as soon as ready without polling or interrupt
- DMA read and write channels

3.9 Filter mathematical accelerator (FMAC)

The filter mathematical accelerator unit performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic, which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

FMAC features

- 16 x 16-bit multiplier
- 24+2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two input, one output), defined by programmable base address pointers and associated size registers
- Input and output sample buffers can be circular
- Buffer “watermark” feature reduces overhead in interrupt mode
- Filter functions: FIR, IIR (direct form 1)
- AHB slave interface
- DMA read and write data channels

3.10 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.11 Power supply management

3.11.1 Power supply schemes

The STM32G484xE devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies, can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V to 3.6 V (see *Section 5: Electrical characteristics* for the minimum V_{DDA} voltage required for ADC, DAC, COMP, OPAMP, VREFBUF operation).
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- VREF-, VREF+

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  The internal voltage reference buffer supports three output voltages, which are configured with VRS bits in the VREFBUF_CSR register:
  - V_{REF+} = 2.048 V
  - V_{REF+} = 2.5 V
  - V_{REF+} = 2.95 V

  V_{REF-} is double bonded with V_{SSA}.

3.11.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the device after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.11.3 Voltage regulator

Two embedded linear voltage regulators, main regulator (MR) and low-power regulator (LPR), supply most of digital circuitry in the device. The MR is used in Run and Sleep modes. The LPR is used in Low-power run, Low-power sleep and Stop modes. In Standby and Shutdown modes, both regulators are powered down and their outputs set in high-impedance state, such as to bring their current consumption close to zero.

The device supports dynamic voltage scaling to optimize its power consumption in Run mode. the voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system’s maximum operating frequency.

The main regulator (MR) operates in the following ranges:

- Range 1 boost mode with the CPU running at up to 170 MHz.
- Range 1 normal mode with CPU running at up to 150 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz.

3.11.4 Low-power modes

By default, the microcontroller is in Run mode after system or power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode**: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Low-power run mode:** This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.
- **Low-power sleep mode:** This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low power run mode.
- **Stop mode:** In Stop mode, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the VCORE domain are stopped. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC). Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode, so as to get clock for processing the wakeup event.
- **Standby mode:** The Standby mode is used to achieve the lowest power consumption with brown-out reset, BOR. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are also powered down. The RTC can remain active (Standby mode with RTC, Standby mode without RTC). The BOR always remains active in Standby mode. For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode. Upon entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and standby circuitry. The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper), or when a failure is detected on LSE (CSS on LSE).
- **Shutdown mode:** The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the VCORE domain. The PLL, as well as the HSI16 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC). The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode. Therefore, switching to RTC domain is not supported. SRAM and register contents are lost except for registers in the RTC domain. The device exits Shutdown mode upon external reset event (NRST pin), IWDG reset event, wakeup event (WKUP pin, configurable rising or falling edge) or RTC event (alarm, periodic wakeup, timestamp, tamper).

3.11.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.11.6 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The V_{BAT} pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in V_{BAT} mode.

The V_{BAT} operation is automatically activated when V_{DD} is not present. An internal V_{BAT} battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: *When the microcontroller is supplied from* V_{BAT}*, neither external interrupts nor RTC alarm/events exit the microcontroller from the* V_{BAT} *operation.*

3.12 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 3. STM32G484xE peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-
	ADCx DACx	Conversion triggers	Y	Y	Y	Y	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-
TIM16/TIM17	IRTIM	Infrared interface output generation	Y	Y	Y	Y	-
COMPx	TIM1, 8, 20 TIM2, 3, 4, 5	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y
	HRTIM	COMPx Output is an input event or a fault input for HRTIM	Y	Y	Y	Y	-
ADCx	TIM1, 8, 20	Timer triggered by analog watchdog	Y	Y	Y	Y	-
	HRTIM	HRTIM external event source can be ADCx analog watchdog	Y	Y	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-
	LPTIMER1	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y
All clocks sources (internal and external)	TIM5, TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-
CSS RAM (parity error) Flash memory (ECC error) COMPx PVD	TIM1,8, 20 TIM15,16,17 HRTIM	Timer break HRTIM SYSFLT	Y	Y	Y	Y	-

Table 3. STM32G484xE peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
CPU (hard fault)	TIM1,8,20 TIM15/16/17 HRTIM	Timer break HRTIM SYSFLT	Y	Y	Y	Y	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-
	LPTIMER1	External trigger	Y	Y	Y	Y	Y
	HRTIM	External fault/event/Synchro inputs for HRTIM	Y	Y	Y	Y	-
	ADCx DACx	Conversion external trigger	Y	Y	Y	Y	-
HRTIM	DACx/ADCx	Conversion trigger	Y	Y	Y	Y	-
	GPIO	Synchro output for HRTIM	Y	Y	Y	Y	-

3.13 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4 - 48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 170 MHz. It can be fed with HSE or HSI16 clocks.
- **RC48 with clock recovery system (HSI48):** internal HSIRC48 MHz clock source can be used to drive the USB or the RNG peripherals.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (I2S, USART, I2C, LPTimer, ADC, SAI, RNG) have their own clock independent of the system clock.
- **Clock security system (CSS):** in the event of HSE clock failure, the system clock is automatically switched to HSI16 and, if enabled, a software interrupt is generated. LSE clock failure can also be detected and generate an interrupt.
- Clock-out capability:
  - **MCO:** microcontroller clock output: it outputs one of the internal clocks for external use by the application
  - **LSCO: low speed clock output:** it outputs LSI or LSE in all low-power modes.

Several prescalers allow to configure the AHB frequency, the High-speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 170 MHz.

3.14 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.15 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 4: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 16 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 16 independently configurable channels (requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are both software programmable (4 levels: very high, high, medium, low) or hardware programmable in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 4. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	8	8

3.16 DMA request router (DMAMux)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

For simplicity, the functional description is limited to DMA request lines. The other DMA control lines are not shown in figures or described in the text. The DMA request generator produces DMA requests following events on DMA request trigger inputs.

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The STM32G484xE devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 102 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 44 edge detector lines used to generate interrupt/event requests and to wake-up the system from the Stop mode. Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently.

A pending register maintains the status of the interrupt requests. The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 107 GPIOs can be connected to the 16 external interrupt lines.

3.18 Analog-to-digital converter (ADC)

The device embeds five successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 4 Msps maximum conversion rate with full resolution
  - Down to 25 ns sampling time
  - Increased conversion rate for lower resolution (up to 6.66 Msps for 6-bit resolution)
- One external reference pin is available on all packages, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching
  - Flexible sample time control
  - Hardware gain and offset compensation

3.18.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADCs input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.18.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADCx_IN18, x = 1,3,4,5 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+} = 3.0$ V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.18.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC1_IN17 channel. As the V_{BAT} voltage may be higher than the V_{DDA}, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.18.4 Operational amplifier internal output (OPAMPxINT):

The OPAMPx (x = 1...6) output OPAMPxINT can be sampled using an ADCx (x = 1...5) internal input channel. In this case, the I/O on which the OPAMPx output is mapped can be used as GPIO.

3.19 Digital to analog converter (DAC)

Seven 12 bit DAC channels (3 external buffered and 4 internal unbuffered) can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Saw tooth wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor
- Up to 1 Msps for external output and 15 Msps for internal output

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.20 Voltage reference buffer (V_{REFBUF})

The STM32G484xE devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

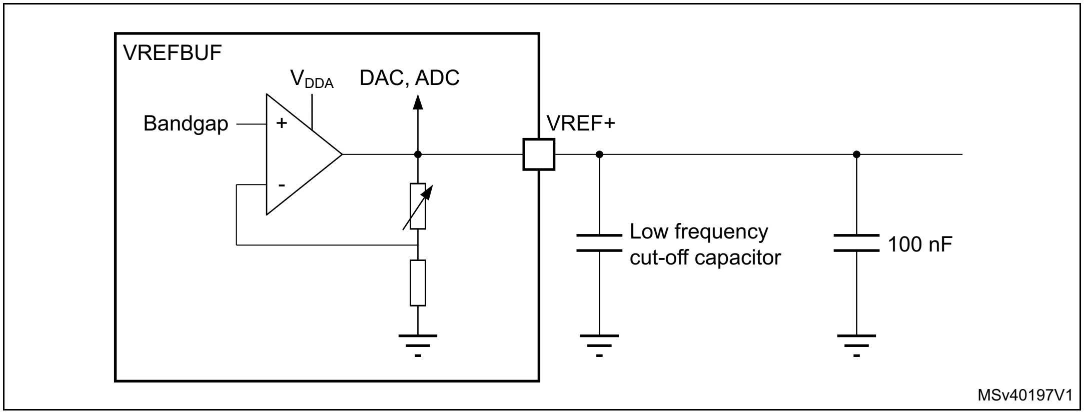
The internal voltage reference buffer supports three voltages:

- 2.048 V
- 2.5 V
- 2.9 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with V_{DDA} on some packages. In these packages the internal voltage reference buffer is not available.

Figure 3. Voltage reference buffer



3.21 Comparators (COMP)

The STM32G484xE devices embed seven rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers.

3.22 Operational amplifier (OPAMP)

The STM32G484xE devices embed six operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- 15 MHz bandwidth
- Rail-to-rail input/output
- PGA with a non-inverting gain ranging of 2, 4, 8, 16, 32 or 64 or inverting gain ranging of -1, -3, -7, -15, -31 or -63

3.23 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.24 Advanced encryption standard hardware accelerator (AES)

The STM32G484xE devices embed an AES hardware accelerator that can be used both to encipher and to decipher data using an AES algorithm.

The AES peripheral supports:

- Encryption/decryption using AES Rijndael block cipher algorithm
- NIST FIPS 197 compliant implementation of AES encryption/decryption algorithm
- 128-bit and 256-bit register for storing the encryption, decryption or derivation key (4x 32-bit registers)
- Electronic codebook (ECB), cipher block chaining (CBC), Counter mode (CTR), Galois Counter Mode (GCM), Galois Message Authentication Code mode (GMAC) and Cipher Message Authentication Code mode (CMAC) supported
- Key scheduler
- Key derivation for decryption
- 128-bit data block processing
- 128-bit, 256-bit key length
- 1x32-bit INPUT buffer and 1x32-bit OUTPUT buffer
- Register access supporting 32-bit data width only
- One 128-bit Register for the initialization vector when AES is configured in CBC mode or for the 32-bit counter initialization when CTR mode is selected, GCM mode or CMAC mode
- Automatic data flow control with support of direct memory access (DMA) using 2 channels, one for incoming data, and one for outcoming data
- Suspend a message if another message with a higher priority needs to be processed.

3.25 Timers and watchdogs

The STM32G484xE devices include One High Resolution time, two advanced motor control timers, up to nine general-purpose timers, two basic timers, one low-power timer, two watchdog timers and a SysTick timer. The table below compares the features of the advanced motor control, general purpose and basic timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
High resolution timer	HRTIM	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	12	Yes
Advanced motor control	TIM1, TIM8, TIM20	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No

Table 7. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.25.1 High-resolution timer (HRTIM)

The high-resolution timer (HRTIM) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 7 timers, 1 master and 6 slaves, totaling 12 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 6 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM timer is made of a digital kernel clocked at 170 MHz followed by delay lines. Delay lines with closed loop control guarantee a 184 ps resolution whatever the voltage, temperature or chip-to-chip manufacturing process deviation. The high-resolution is available on the 12 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

In debug mode, the HRTIM counters can be frozen and the PWM outputs enter safe state.

3.25.2 Advanced motor control timer (TIM1, TIM8, TIM20)

The advanced motor control timers can each be seen as a four-phase PWM multiplexed on 8 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced motor control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.25.3*) using the same architecture, so the advanced motor control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.25.3 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32G484xE devices (see *Table 7* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  - TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler
  - TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  - TIM15 has 2 channels and 1 complementary channel
  - TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.25.4 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.25.5 Low-power timer (LPTIM1)

The devices embed a low-power timer. This timer has an independent clock and are running in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the system from Stop mode.

LPTIM1 is active in Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode

3.25.6 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.25.7 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.25.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.26 Real-time clock (RTC) and backup registers

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.27 Tamper and backup registers (TAMP)

- 32 32-bit backup registers, retained in all low-power modes and also in V_{BAT} mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.
- Up to three tamper pins for external tamper detection events. The external tamper pins can be configured for edge detection, edge and level, level detection with filtering.
- Five internal tampers events.
- Any tamper detection can generate a RTC timestamp event.
- Any tamper detection erases the backup registers.
- Any tamper detection can generate an interrupt and wake-up the device from all low-power modes.

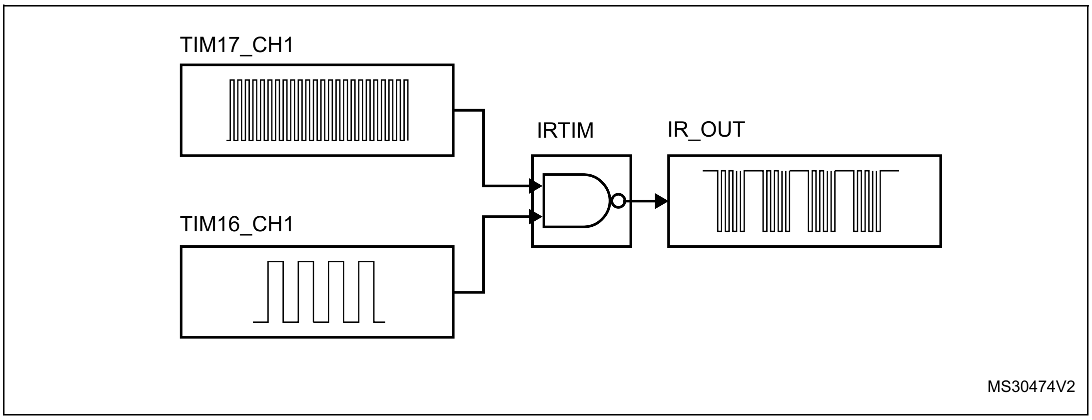
3.28 Infrared transmitter

The STM32G484xE devices provide an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 4. Infrared transmitter



3.29 Inter-integrated circuit interface (I^2C)

The device embeds four I2Cs. Refer to *Table 8: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop mode on address match	X	X	X	X

1. X: supported

3.30 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32G484xE devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, USART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

The USART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the U(S)ARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode. The wakeup from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

All USART interfaces can be served by the DMA controller.

Table 9. USART/UART/LPUART features

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop mode	X	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver Enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

Table 9. USART/UART/LPUART features (continued)

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5	LPUART1
Tx/Rx FIFO	X					
Tx/Rx FIFO size	8					

1. X = supported.

3.31 Low-power universal asynchronous receiver transmitter (LPUART)

The STM32G484xE devices embed one Low-Power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART comes with a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default. It has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wake up from Stop mode can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Some specific TXFIFO/RXFIFO status interrupts when FIFO mode is enabled

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.32 Serial peripheral interface (SPI)

Four SPI interfaces allow communication up to 75 Mbits/s in master and up to 41 Mbits/s in slave, half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

Two standard I^{2}S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

All SPI interfaces can be served by the DMA controller.

3.33 Serial audio interfaces (SAI)

The device embeds 1 SAI. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC’97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with 2 dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 10. SAI implementation for the features implementation

SAI features	Support[1]
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97	X
Mute mode	X
Stereo/Mono audio frame capability	X
16 slots	X

Table 10. SAI implementation for the features implementation (continued)

SAI features	Support[1]
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO size	X (8 word)
SPDIF	X

1. X: supported.

3.34 Controller area network (FDCAN1, FDCAN2, FDCAN3)

The controller area network (CAN) subsystem consists of three CAN modules and a shared message RAM memory.

The three CAN modules (FDCAN1, FDCAN2 and FDCAN3) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 3-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers. This message RAM is shared between the three FDCAN modules.

3.35 Universal serial bus (USB)

The STM32G484xE devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.36 USB Type-C™ / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.37 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.38 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.39 Quad SPI memory interface (QUADSPI)

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory.

Both throughput and capacity can be increased two-fold using dual-flash mode, where two quad SPI flash memories are accessed simultaneously.

The Quad SPI interface supports:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory
- Three functional modes: indirect, status-polling, and memory-mapped
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
  - Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

3.40 Development support

3.40.1 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.40.2 Embedded trace macrocell™

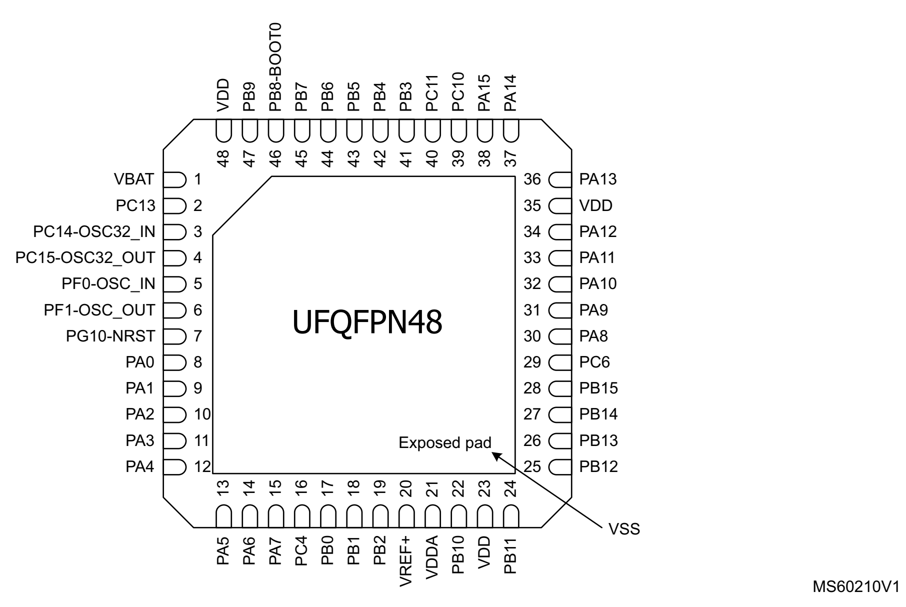
The Arm embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32G484xE devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded trace macrocell operates with third party debugger software tools.

4 Pinouts and pin description

4.1 UFQFPN48 pinout description

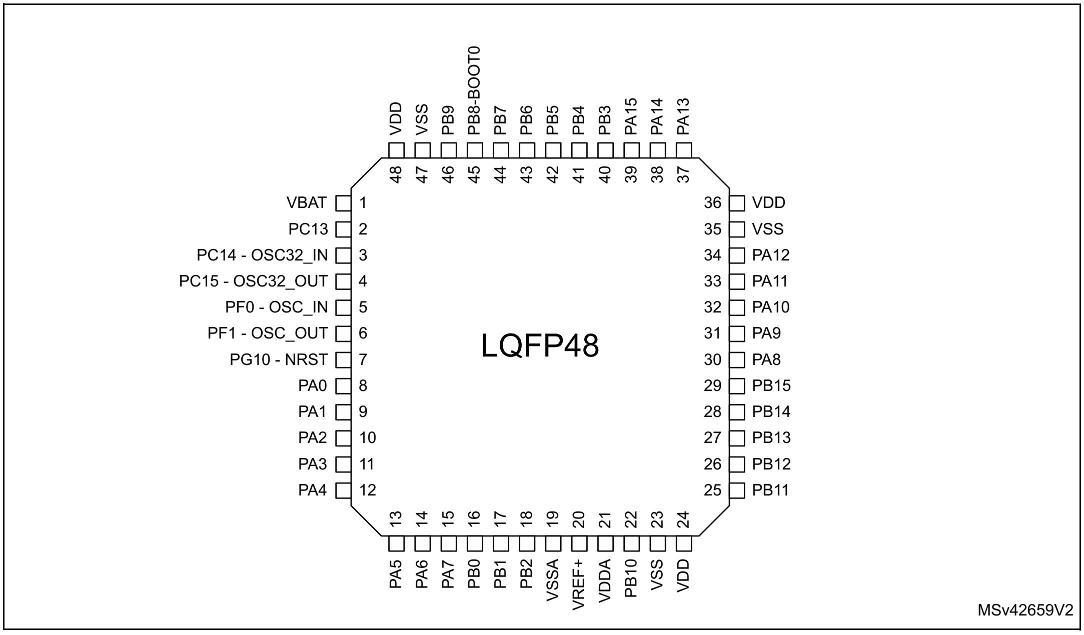
Figure 5. STM32G484xE UFQFPN48 pinout



1. The above figure shows the package top view.
2. VSS pads are connected to the exposed pad.

4.2 LQFP48 pinout description

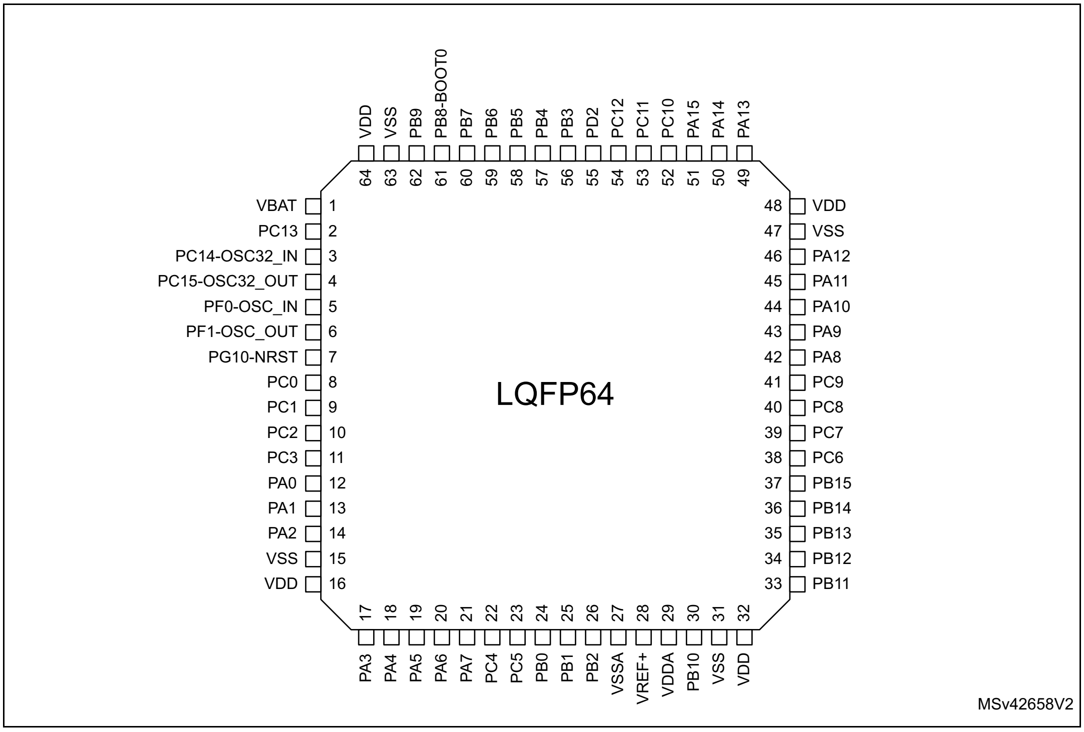
Figure 6. STM32G484xE LQFP48 pinout



1. The above figure shows the package top view.

4.3 LQFP64 pinout description

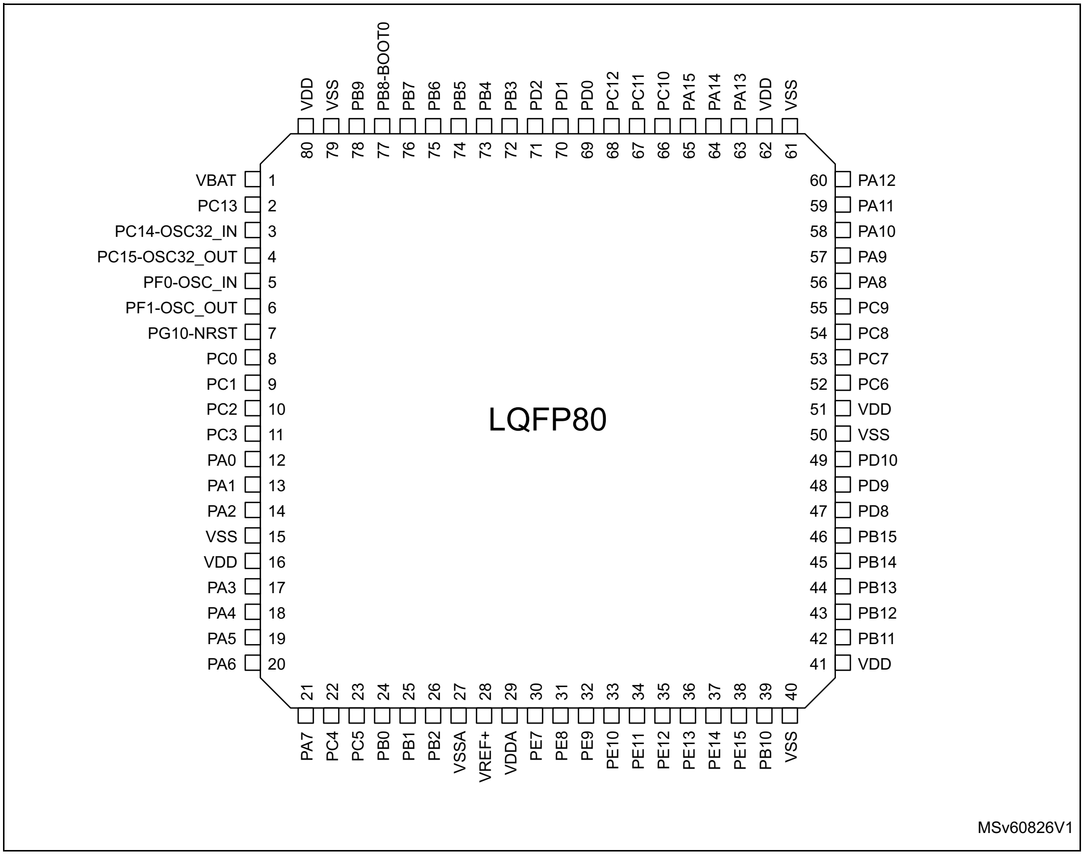
Figure 7. STM32G484xE LQFP64 pinout



1. The above figure shows the package top view.

4.4 LQFP80 pinout description

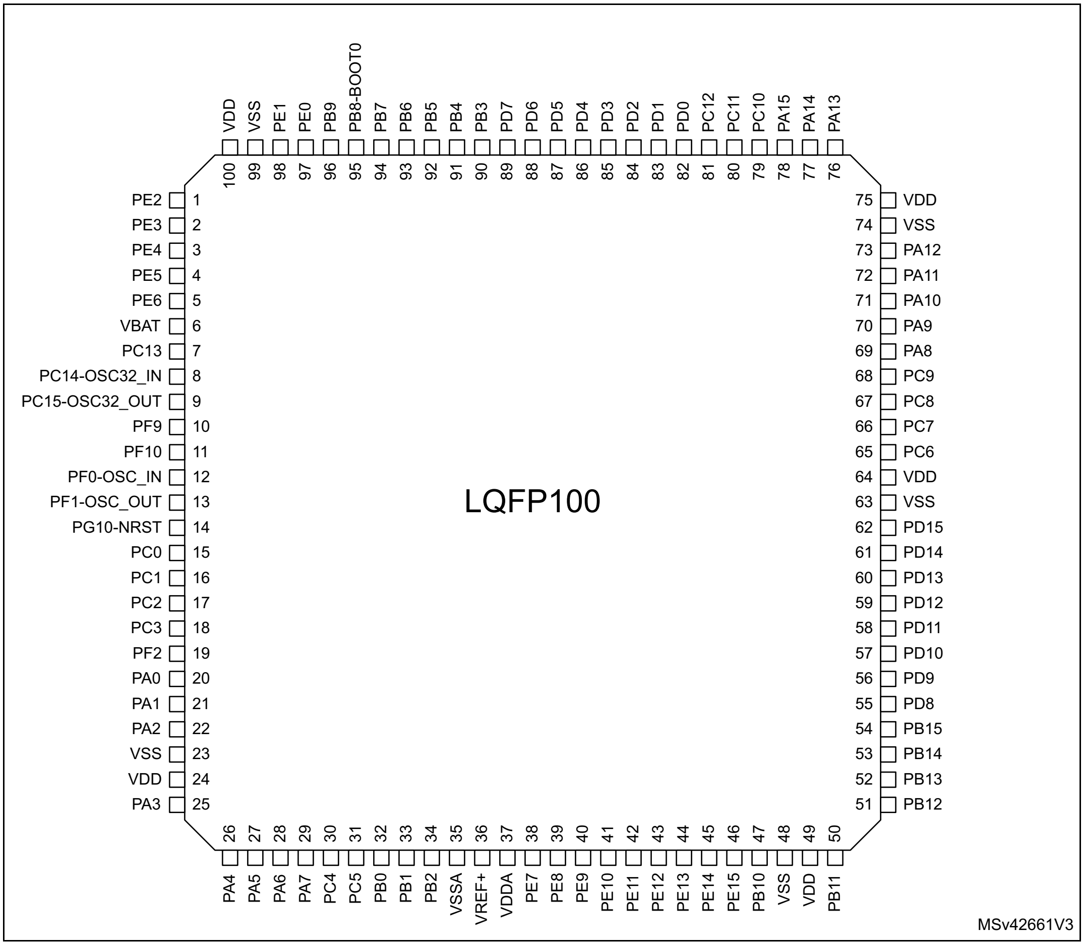
Figure 8. STM32G484xE LQFP80 pinout



1. The above figure shows the package top view.

4.5 LQFP100 pinout description

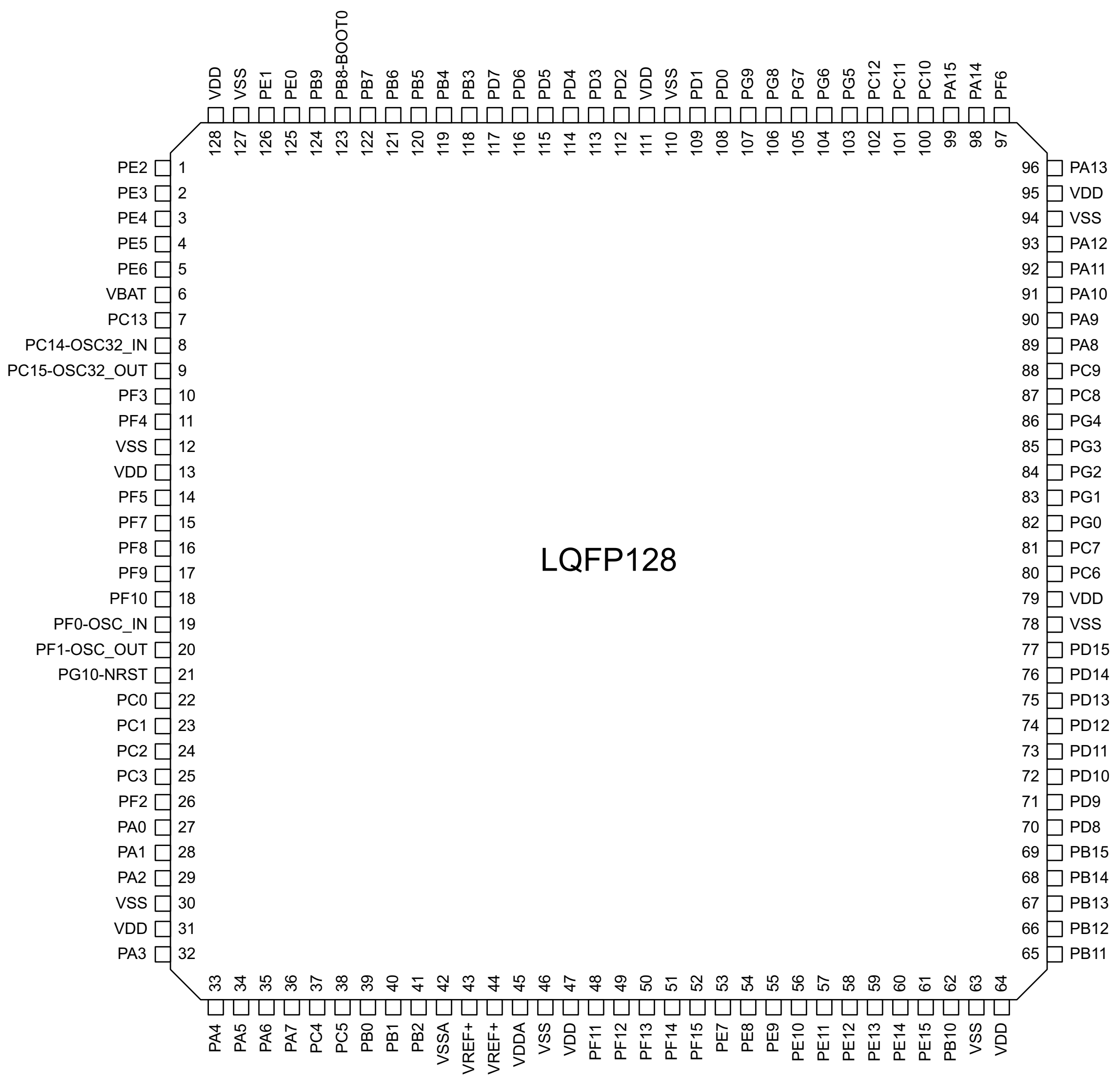
Figure 9. STM32G484xE LQFP100 pinout



1. The above figure shows the package top view.

4.6 LQFP128 pinout description

Figure 10. STM32G484xE LQFP128 pinout



1. The above figure shows the package top view.

4.7 WLCSP81 pinout description

Figure 11. STM32G484xE WLCSP81 pinout

	1	2	3	4	5	6	7	8	9
A	VDD	PA15	PC12	PD1	PB3	PB5	PB9	VSS	VDD
B	VSS	PA13	PC10	PD0	PD2	PB6	PB8-BOOT0	PC13	VBAT
C	PA12	PA11	PA14	PC11	PC8	PB4	PB7	PC1	PC14-OSC32_IN
D	PA8	PC9	PA10	PA9	PC7	PA4	PA0	PG10-NRST	PC15-OSC32_OUT
E	VDD	PD11	PC6	PB15	PE12	PC4	PA1	PC0	PF0-OSC_IN
F	VSS	PD10	PD9	PE15	PE9	PB0	PA5	PC2	PF1-OSC_OUT
G	PD8	PB14	PB12	PE13	PE8	PB1	PA6	PA2	PC3
H	PB13	PB11	PB10	PE11	PE7	VSSA	PC5	PA3	VSS
J	VDD	VSS	PE14	PE10	VDDA	VREF+	PB2	PA7	VDD

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1. The above figure shows the package top view.

4.8 TFBGA100 pinout description

Figure 12. STM32G484xE TFBGA100 pinout

	1	2	3	4	5	6	7	8	9	10
A	PE4	PB9	PB8-BOOT0	PB6	PB3	PD6	PD5	PD4	PD1	PC12
B	PE5	PE3	PE1	PB7	PB5	PD7	PD2	PD0	PA15	PA14
C	PC14-OSC32_IN	PE6	PE2	PE0	PB4	PD3	PC11	PC10	PA12	PA11
D	PC15-OSC32_OUT	VSS	VBAT	PC13	VDD	VSS	VDD	PA13	PA10	PA9
E	PF0-OSC_IN	PF1-OSC_OUT	PF9	PF10	VSS	VSS	VSS	PC8	PC9	PA8
F	PC2	PC0	PG10-NRST	PC1	VDD	VSS	VDD	PD14	PC6	PC7
G	PC3	PA1	PF2	PA0	PE7	PE12	PD10	PD9	PD13	PD15
H	PA2	PA4	PA3	PB0	PE8	PE9	PE15	PB11	PB14	PD11
J	PA5	PA6	PC5	PB2	VDDA	PE11	PE14	PB10	PB13	PD12
K	PA7	PC4	PB1	VSSA	VREF+	PE10	PE13	PB12	PB15	PD8

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1. The above figure shows the package top view.

4.9 Pin definition

Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TT	3.6 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
	Option for TT or FT I/Os	
	_a(1)	I/O, with Analog switch function supplied by V_{DDA}
	_c	I/O, USB Type-C PD capable
	_d	I/O, USB Type-C PD Dead Battery function
	_f(2)	I/O, Fm+ capable
	_u(3)	I/O, with USB function
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled through peripheral registers

1. The related I/O structures in *Table 12* are: FT_a, FT_fa, TT_a.
2. The related I/O structures in *Table 12* are: FT_f, FT_fa.
3. The related I/O structures in *Table 12* are FT_u.

Table 12. STM32G484xE pin definition

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	C3	1	1	PE2	I/O	FT	-	TRACECK, TIM3_CH1, SAI1_CK1, SPI4_SCK, TIM20_CH1, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	B2	2	2	PE3	I/O	FT	-	TRACED0, TIM3_CH2, SPI4_NSS, TIM20_CH2, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	A1	3	3	PE4	I/O	FT	-	TRACED1, TIM3_CH3, SAI1_D2, SPI4_NSS, TIM20_CH1N, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	B1	4	4	PE5	I/O	FT	-	TRACED2, TIM3_CH4, SAI1_CK2, SPI4_MISO, TIM20_CH2N, FMC_A21, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	C2	5	5	PE6	I/O	FT	-	TRACED3, SAI1_D1, SPI4_MOSI, TIM20_CH3N, FMC_A22, SAI1_SD_A, EVENTOUT	WKUP3, RTC_TAMP3
B9	1	1	1	1	D3	6	6	VBAT	S	-	-	-	-
B8	2	2	2	2	D4	7	7	PC13	I/O	FT	(2) (3)	TIM1_BKIN, TIM1_CH1N, TIM8_CH4N, EVENTOUT	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT1
C9	3	3	3	3	C1	8	8	PC14-OSC32_IN	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
D9	4	4	4	4	D1	9	9	PC15-OSC32_OUT	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	-	-	10	PF3	I/O	FT_f	-	TIM20_CH4, I2C3_SCL, FMC_A3, EVENTOUT	-
-	-	-	-	-	-	-	11	PF4	I/O	FT_f	-	COMP1_OUT, TIM20_CH1N, I2C3_SDA, FMC_A4, EVENTOUT	-
F1	-	-	-	-	D2	-	12	VSS	S	-	-	-	-
A9	-	-	-	-	D5	-	13	VDD	S	-	-	-	-
-	-	-	-	-	-	-	14	PF5	I/O	FT	-	TIM20_CH2N, FMC_A5, EVENTOUT	-
-	-	-	-	-	-	-	15	PF7	I/O	FT	-	TIM20_BKIN, TIM5_CH2, QUADSPI1_BK1_IO2, FMC_A1, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	16	PF8	I/O	FT	-	TIM20_BKIN2, TIM5_CH3, QUADSPI1_BK1_IO0, FMC_A24, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	-	E3	10	17	PF9	I/O	FT	-	TIM20_BKIN, TIM15_CH1, SPI2_SCK, TIM5_CH4, QUADSPI1_BK1_IO1, FMC_A25, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	E4	11	18	PF10	I/O	FT	-	TIM20_BKIN2, TIM15_CH2, SPI2_SCK, QUADSPI1_CLK, FMC_A0, SAI1_D3, EVENTOUT	-
E9	5	5	5	5	E1	12	19	PF0-OSC_IN	I/O	FT_fa	-	I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N, EVENTOUT	ADC1_IN10, OSC_IN
F9	6	6	6	6	E2	13	20	PF1-OSC_OUT	I/O	FT_a	-	SPI2_SCK/I2S2_CK, EVENTOUT	ADC2_IN10, COMP3_INM, OSC_OUT

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
D8	7	7	7	7	F3	14	21	PG10-NRST	I/O	FT	-	MCO, EVENTOUT	NRST
E8	-	-	8	8	F2	15	22	PC0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH1, LPUART1_RX, EVENTOUT	ADC12_IN6, COMP3_INM
C8	-	-	9	9	F4	16	23	PC1	I/O	TT_a	-	LPTIM1_OUT, TIM1_CH2, LPUART1_TX, QUADSPI1_BK2_IO0, SAI1_SD_A, EVENTOUT	ADC12_IN7, COMP3_INP
F8	-	-	10	10	F1	17	24	PC2	I/O	FT_a	-	LPTIM1_IN2, TIM1_CH3, COMP3_OUT, TIM20_CH2, QUADSPI1_BK2_IO1, EVENTOUT	ADC12_IN8
G9	-	-	11	11	G1	18	25	PC3	I/O	TT_a	-	LPTIM1_ETR, TIM1_CH4, SAI1_D1, TIM1_BKIN2, QUADSPI1_BK2_IO2, SAI1_SD_A, EVENTOUT	ADC12_IN9, OPAMP5_VINP
-	-	-	-	-	G3	19	26	PF2	I/O	FT	-	TIM20_CH3, I2C2_SMBA, FMC_A2, EVENTOUT	-
D7	8	8	12	12	G4	20	27	PA0	I/O	TT_a	-	TIM2_CH1, TIM5_CH1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, TIM2_ETR, EVENTOUT	ADC12_IN1, COMP1_INM, COMP3_INP, RTC_TAMP2,WKUP1
E7	9	9	13	13	G2	21	28	PA1	I/O	TT_a	-	RTC_REFIN, TIM2_CH2, TIM5_CH2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC12_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP, OPAMP6_VINM

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
G8	10	10	14	14	H1	22	29	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, USART2_TX, COMP2_OUT, TIM15_CH1, QUADSPI1_BK1_NCS, LPUART1_TX, UCPD1_FRSTX, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT, WKUP4/LSCO
H9	-	-	15	15	D6	23	30	VSS	S	-	-	-	-
J9	-	-	16	16	D7	24	31	VDD	S	-	-	-	-
H8	11	11	17	17	H3	25	32	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI1_CK1, USART2_RX, TIM15_CH2, QUADSPI1_CLK, LPUART1_RX, SAI1_MCLK_A, EVENTOUT	ADC1_IN4, COMP2_INP, OPAMP1_VINM/ OPAMP 1_VINP, OPAMP5_VINM
D6	12	12	18	18	H2	26	33	PA4	I/O	TT_a	-	TIM3_CH2, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, SAI1_FS_B, EVENTOUT	ADC2_IN17, DAC1_OUT1, COMP1_INM
F7	13	13	19	19	J1	27	34	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, UCPD1_FRSTX, EVENTOUT	ADC2_IN13, DAC1_OUT2, COMP2_INM, OPAMP2_VINM
G7	14	14	20	20	J2	28	35	PA6	I/O	TT_a	-	TIM16_CH1, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, QUADSPI1_BK1_IO3, LPUART1_CTS, EVENTOUT	ADC2_IN3, DAC2_OUT1, OPAMP2_VOUT
J8	15	15	21	21	K1	29	36	PA7	I/O	TT_a	-	TIM17_CH1, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, COMP2_OUT, QUADSPI1_BK1_IO2, UCPD1_FRSTX, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP1_VINP, OPAMP2_VINP

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
E6	16	-	22	22	K2	30	37	PC4	I/O	FT_fa	-	TIM1_ETR, I2C2_SCL, USART1_TX, QUADSPI1_BK2_IO3, EVENTOUT	ADC2_IN5
H7	-	-	23	23	J3	31	38	PC5	I/O	TT_a	-	TIM15_BKIN, SAI1_D3, TIM1_CH4N, USART1_RX, HRTIM1_EEV10, EVENTOUT	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM, WKUP5
F6	17	16	24	24	H4	32	39	PB0	I/O	TT_a	-	TIM3_CH3, TIM8_CH2N, TIM1_CH2N, QUADSPI1_BK1_IO1, HRTIM1_FLT5, UCPD1_FRSTX, EVENTOUT	ADC3_IN12/ADC1_IN15, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP
G6	18	17	25	25	K3	33	40	PB1	I/O	TT_a	-	TIM3_CH4, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, QUADSPI1_BK1_IO0, LPUART1_RTS_DE, HRTIM1_SCOUT, EVENTOUT	ADC3_IN1/ADC1_IN12, COMP1_INP, OPAMP3_VOUT, OPAMP6_VINM
J7	19	18	26	26	J4	34	41	PB2	I/O	TT_a	-	RTC_OUT2, LPTIM1_OUT, TIM5_CH1, TIM20_CH1, I2C3_SMBA, QUADSPI1_BK2_IO1, HRTIM1_SCIN, EVENTOUT	ADC2_IN12, COMP4_INM, OPAMP3_VINM
H6	-	19	27	27	K4	35	42	VSSA	S	-	-	-	-
J6	20	20	28	28	K5	36	43	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	-	-	44	VREF+	S	-	-	-	VREFBUF_OUT
J5	21	21	29	29	J5	37	45	VDDA	S	-	-	-	-
H9	-	-	-	-	E5	-	46	VSS	S	-	-	-	-
J1	-	-	-	-	F5	-	47	VDD	S	-	-	-	-
-	-	-	-	-	-	-	48	PF11	I/O	FT	-	TIM20_ETR, FMC_NE4, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	-	-	49	PF12	I/O	FT	-	TIM20_CH1, FMC_A6, EVENTOUT	-
-	-	-	-	-	-	-	50	PF13	I/O	FT	-	TIM20_CH2, I2C4_SMBA, FMC_A7, EVENTOUT	-
-	-	-	-	-	-	-	51	PF14	I/O	FT_f	-	TIM20_CH3, I2C4_SCL, FMC_A8, EVENTOUT	-
-	-	-	-	-	-	-	52	PF15	I/O	FT_f	-	TIM20_CH4, I2C4_SDA, FMC_A9, EVENTOUT	-
H5	-	-	-	30	G5	38	53	PE7	I/O	TT_a	-	TIM1_ETR, FMC_D4, SAI1_SD_B, EVENTOUT	ADC3_IN4, COMP4_INP
G5	-	-	-	31	H5	39	54	PE8	I/O	FT_a	-	TIM5_CH3, TIM1_CH1N, FMC_D5, SAI1_SCK_B, EVENTOUT	ADC345_IN6, COMP4_INM
F5	-	-	-	32	H6	40	55	PE9	I/O	FT_a	-	TIM5_CH4, TIM1_CH1, FMC_D6, SAI1_FS_B, EVENTOUT	ADC3_IN2
J4	-	-	-	33	K6	41	56	PE10	I/O	FT_a	-	TIM1_CH2N, QUADSPI1_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	ADC345_IN14
H4	-	-	-	34	J6	42	57	PE11	I/O	FT_a	-	TIM1_CH2, SPI4_NSS, QUADSPI1_BK1_NCS, FMC_D8, EVENTOUT	ADC345_IN15
E5	-	-	-	35	G6	43	58	PE12	I/O	FT_a	-	TIM1_CH3N, SPI4_SCK, QUADSPI1_BK1_IO0, FMC_D9, EVENTOUT	ADC345_IN16
G4	-	-	-	36	K7	44	59	PE13	I/O	FT_a	-	TIM1_CH3, SPI4_MISO, QUADSPI1_BK1_IO1, FMC_D10, EVENTOUT	ADC3_IN3

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
J3	-	-	-	37	J7	45	60	PE14	I/O	FT_a	-	TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, QUADSPI1_BK1_IO2, FMC_D11, EVENTOUT	ADC4_IN1
F4	-	-	-	38	H7	46	61	PE15	I/O	FT_a	-	TIM1_BKIN, TIM1_CH4N, USART3_RX, QUADSPI1_BK1_IO3, FMC_D12, EVENTOUT	ADC4_IN2
H3	22	22	30	39	J8	47	62	PB10	I/O	TT_a	-	TIM2_CH3, USART3_TX, LPUART1_RX, QUADSPI1_CLK, TIM1_BKIN, HRTIM1_FLT3, SAI1_SCK_A, EVENTOUT	COMP5_INM, OPAMP3_VINM, OPAMP4_VINM
J2	-	23	31	40	E6	48	63	VSS	S	-	-	-	-
J1	23	24	32	41	F7	49	64	VDD	S	-	-	-	-
H2	24	25	33	42	H8	50	65	PB11	I/O	TT_a	-	TIM2_CH4, USART3_RX, LPUART1_TX, QUADSPI1_BK1_NCS, HRTIM1_FLT4, EVENTOUT	ADC12_IN14, COMP6_INP, OPAMP4_VINP, OPAMP6_VOUT
G3	25	26	34	43	K8	51	66	PB12	I/O	TT_a	-	TIM5_ETR, I2C2_SMBA, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, LPUART1_RTS_DE, FDCAN2_RX, HRTIM1_CHC1, EVENTOUT	ADC4_IN3/ADC1_IN11, COMP7_INM, OPAMP4_VOUT, OPAMP6_VINP
H1	26	27	35	44	J9	52	67	PB13	I/O	TT_a	-	SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, LPUART1_CTS, FDCAN2_TX, HRTIM1_CHC2, EVENTOUT	ADC3_IN5, COMP5_INP, OPAMP3_VINP, OPAMP4_VINP, OPAMP6_VINP

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
G2	27	28	36	45	H9	53	68	PB14	I/O	TT_a	-	TIM15_CH1, SPI2_MISO, TIM1_CH2N, USART3_RTS_DE, COMP4_OUT, HRTIM1_CHD1, EVENTOUT	ADC4_IN4/ADC1_IN5, COMP7_INP, OPAMP2_VINP, OPAMP5_VINP
E4	28	29	37	46	K9	54	69	PB15	I/O	TT_a	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, COMP3_OUT, TIM1_CH3N, SPI2_MOSI/I2S2_SD, HRTIM1_CHD2, EVENTOUT	ADC4_IN5/ADC2_IN15, COMP6_INM, OPAMP5_VINM
G1	-	-	-	47	K10	55	70	PD8	I/O	TT_a	-	USART3_TX, FMC_D13, EVENTOUT	ADC4_IN12/ADC5_IN12, OPAMP4_VINM
F3	-	-	-	48	G8	56	71	PD9	I/O	TT_a	-	USART3_RX, FMC_D14, EVENTOUT	ADC4_IN13/ADC5_IN13, OPAMP6_VINP
F2	-	-	-	49	G7	57	72	PD10	I/O	FT_a	-	USART3_CK, FMC_D15, EVENTOUT	ADC345_IN7, COMP6_INM
E2	-	-	-	-	H10	58	73	PD11	I/O	TT_a	-	TIM5_ETR, I2C4_SMBA, USART3_CTS, FMC_A16, EVENTOUT	ADC345_IN8, COMP6_INP, OPAMP4_VINP
-	-	-	-	-	J10	59	74	PD12	I/O	TT_a	-	TIM4_CH1, USART3_RTS_DE, FMC_A17, EVENTOUT	ADC345_IN9, COMP5_INP, OPAMP5_VINP
-	-	-	-	-	G9	60	75	PD13	I/O	FT_a	-	TIM4_CH2, FMC_A18, EVENTOUT	ADC345_IN10, COMP5_INM
-	-	-	-	-	F8	61	76	PD14	I/O	TT_a	-	TIM4_CH3, FMC_D0, EVENTOUT	ADC345_IN11, COMP7_INP, OPAMP2_VINP
-	-	-	-	-	G10	62	77	PD15	I/O	FT_a	-	TIM4_CH4, SPI2_NSS, FMC_D1, EVENTOUT	COMP7_INM
B1	-	-	-	50	E7	63	78	VSS	S	-	-	-	-
E1	-	-	-	51	-	64	79	VDD	S	-	-	-	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
E3	29	-	38	52	F9	65	80	PC6	I/O	FT_f	-	TIM3_CH1, HRTIM1_EEV10, TIM8_CH1, I2S2_MCK, COMP6_OUT, I2C4_SCL, HRTIM1_CHF1, EVENTOUT	-
D5	-	-	39	53	F10	66	81	PC7	I/O	FT_f	-	TIM3_CH2, HRTIM1_FLT5, TIM8_CH2, I2S3_MCK, COMP5_OUT, I2C4_SDA, HRTIM1_CHF2, EVENTOUT	-
-	-	-	-	-	-	-	82	PG0	I/O	FT	-	TIM20_CH1N, FMC_A10, EVENTOUT	-
-	-	-	-	-	-	-	83	PG1	I/O	FT	-	TIM20_CH2N, FMC_A11, EVENTOUT	-
-	-	-	-	-	-	-	84	PG2	I/O	FT	-	TIM20_CH3N, SPI1_SCK, FMC_A12, EVENTOUT	-
-	-	-	-	-	-	-	85	PG3	I/O	FT_f	-	TIM20_BKIN, I2C4_SCL, SPI1_MISO, TIM20_CH4N, FMC_A13, EVENTOUT	-
-	-	-	-	-	-	-	86	PG4	I/O	FT_f	-	TIM20_BKIN2, I2C4_SDA, SPI1_MOSI, FMC_A14, EVENTOUT	-
C5	-	-	40	54	E8	67	87	PC8	I/O	FT_f	-	TIM3_CH3, HRTIM1_CHE1, TIM8_CH3, TIM20_CH3, COMP7_OUT, I2C3_SCL, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
D2	-	-	41	55	E9	68	88	PC9	I/O	FT_f	-	TIM3_CH4, RTIM1_CHE2, TIM8_CH4, I2SCKIN, TIM8_BKIN2, I2C3_SDA, EVENTOUT	-
D1	30	30	42	56	E10	69	89	PA8	I/O	FT_a	-	MCO, I2C3_SCL, I2C2_SDA, I2S2_MCK, TIM1_CH1, USART1_CK, COMP7_OUT, TIM4_ETR, FDCAN3_RX, SAI1_CK2, HRTIM1_CHA1, SAI1_SCK_A, EVENTOUT	ADC5_IN1, OPAMP5_VOUT
D4	31	31	43	57	D10	70	90	PA9	I/O	FT_fda	-	I2C3_SMBA, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, OMP5_OUT, TIM15_BKIN, TIM2_CH3, HRTIM1_CHA2, SAI1_FS_A, EVENTOUT	ADC5_IN2, UCPD1_DBCC1
D3	32	32	44	58	D9	71	91	PA10	I/O	FT_fda	-	TIM17_BKIN, USB_CRS_SYNC, I2C2_SMBA, SPI2_MISO, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, TIM8_BKIN, SAI1_D1, HRTIM1_CHB1, SAI1_SD_A, EVENTOUT	UCPD1_DBCC2

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
C2	33	33	45	59	C10	72	92	PA11	I/O	FT_u	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, FDCAN1_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, HRTIM1_CHB2, EVENTOUT	USB_DM
C1	34	34	46	60	C9	73	93	PA12	I/O	FT_u	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, FDCAN1_TX, TIM4_CH2, TIM1_ETR, HRTIM1_FLT1, EVENTOUT	USB_DP
A8	-	35	47	61	F6	74	94	VSS	S	-	-	-	-
A1	35	36	48	62	-	75	95	VDD	S	-	-	-	-
B2	36	37	49	63	D8	76	96	PA13	I/O	FT_f	(4)	SWDIO-JTMS, TIM16_CH1N, I2C4_SCL, I2C1_SCL, IR_OUT, USART3_CTS, TIM4_CH3, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	97	PF6	I/O	FT_f	-	TIM5_ETR, TIM4_CH4, SAI1_SD_B, I2C2_SCL, TIM5_CH1, USART3_RTS, QUADSPI1_BK1_IO3, EVENTOUT	-
C3	37	38	50	64	B10	77	98	PA14	I/O	FT_f	(4)	SWCLK-JTCK, LPTIM1_OUT, I2C4_SMBA, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, SAI1_FS_B, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
A2	38	39	51	65	B9	78	99	PA15	I/O	FT_f	(4)	JTDI, TIM2_CH1, TIM8_CH1, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, UART4_RTS_DE, TIM1_BKIN, FDCAN3_TX, HRTIM1_FLT2, TIM2_ETR, EVENTOUT	-
B3	39	-	52	66	C8	79	100	PC10	I/O	FT	-	TIM8_CH1N, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX, HRTIM1_FLT6, EVENTOUT	-
C4	40	-	53	67	C7	80	101	PC11	I/O	FT_f	-	HRTIM1_EEV2, TIM8_CH2N, UART4_RX, SPI3_MISO, USART3_RX, I2C3_SDA, EVENTOUT	-
A3	-	-	54	68	A10	81	102	PC12	I/O	FT	-	TIM5_CH2, HRTIM1_EEV1, TIM8_CH3N, UART5_TX, SPI3_MOSI/I2S3_SD , USART3_CK, UCPD1_FRSTX, EVENTOUT	-
-	-	-	-	-	-	-	103	PG5	I/O	FT	-	TIM20_ETR, SPI1_NSS, LPUART1_CTS, FMC_A15, EVENTOUT	-
-	-	-	-	-	-	-	104	PG6	I/O	FT	-	TIM20_BKIN, I2C3_SMBA, LPUART1_RTS_DE, FMC_INT, EVENTOUT	-
-	-	-	-	-	-	-	105	PG7	I/O	FT_f	-	SAI1_CK1, I2C3_SCL, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	-	-	106	PG8	I/O	FT_f	-	I2C3_SDA, LPUART1_RX, FMC_NE3, EVENTOUT	-
-	-	-	-	-	-	-	107	PG9	I/O	FT	-	SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, TIM15_CH1N, EVENTOUT	-
B4	-	-	-	69	B8	82	108	PD0	I/O	FT	-	TIM8_CH4N, FDCAN1_RX, FMC_D2, EVENTOUT	-
A4	-	-	-	70	A9	83	109	PD1	I/O	FT	-	TIM8_CH4, TIM8_BKIN2, FDCAN1_TX, FMC_D3, EVENTOUT	-
-	-	-	-	-	-	-	110	VSS	S	-	-	-	-
A1	-	-	-	-	-	-	111	VDD	S	-	-	-	-
B5	-	-	55	71	B7	84	112	PD2	I/O	FT	-	TIM3_ETR, TIM8_BKIN, UART5_RX, EVENTOUT	-
-	-	-	-	-	C6	85	113	PD3	I/O	FT	-	TIM2_CH1/ TIM2_ETR, USART2_CTS, QUADSPI1_BK2_NCS, FMC_CLK, EVENTOUT	-
-	-	-	-	-	A8	86	114	PD4	I/O	FT	-	TIM2_CH2, USART2_RTS_DE, QUADSPI1_BK2_IO0, FMC_NOE, EVENTOUT	-
-	-	-	-	-	A7	87	115	PD5	I/O	FT	-	USART2_TX, QUADSPI1_BK2_IO1, FMC_NWE, EVENTOUT	-
-	-	-	-	-	A6	88	116	PD6	I/O	FT	-	TIM2_CH4, SAI1_D1, USART2_RX, QUADSPI1_BK2_IO2, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	B6	89	117	PD7	I/O	FT	-	TIM2_CH3, USART2_CK, QUADSPI1_BK2_IO3 , FMC_NCE/FMC_NE1, EVENTOUT	-
A5	41	40	56	72	A5	90	118	PB3	I/O	FT	(4)	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, UCPD1_CRS_SYNC, TIM8_CH1N, SPI1_SCK, SPI3_SCK/I2S3_CK, USART2_TX, TIM3_ETR, FDCAN3_RX, HRTIM1_SCOUT, HRTIM1_EEV9, SAI1_SCK_B, EVENTOUT	-
C6	42	41	57	73	C5	91	119	PB4	I/O	FT_c	(4)	JTRST, TIM16_CH1, TIM3_CH1, TIM8_CH2N, SPI1_MISO, SPI3_MISO, USART2_RX, UART5_RTS_DE, TIM17_BKIN, FDCAN3_TX, HRTIM1_EEV7, SAI1_MCLK_B, EVENTOUT	UCPD1_CC2
A6	43	42	58	74	B5	92	120	PB5	I/O	FT_f	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD , USART2_CK, I2C3_SDA, FDCAN2_RX, TIM17_CH1, LPTIM1_IN1, SAI1_SD_B, HRTIM1_EEV6, UART5_CTS, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)(1)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
B6	44	43	59	75	A4	93	121	PB6	I/O	FT_c	-	TIM16_CH1N, TIM4_CH1, TIM8_CH1, TIM8_ETR, USART1_TX, COMP4_OUT, FDCAN2_TX, TIM8_BKIN2, LPTIM1_ETR, HRTIM1_SCIN, HRTIM1_EEV4, SAI1_FS_B, EVENTOUT	UCPD1_CC1
C7	45	44	60	76	B4	94	122	PB7	I/O	FT_f	-	TIM17_CH1N, TIM4_CH2, I2C4_SDA, I2C1_SDA, TIM8_BKIN, USART1_RX, COMP3_OUT, TIM3_CH4, LPTIM1_IN2, FMC_NL, HRTIM1_EEV3, UART4_CTS, EVENTOUT	PVD_IN
B7	46	45	61	77	A3	95	123	PB8-BOOT0	I/O	FT_f	(5)	TIM16_CH1, TIM4_CH3, SAI1_CK1, I2C1_SCL, USART3_RX, COMP1_OUT, FDCAN1_RX, TIM8_CH2, TIM1_BKIN, HRTIM1_EEV8, SAI1_MCLK_A, EVENTOUT	-
A7	47	46	62	78	A2	96	124	PB9	I/O	FT_f	-	TIM17_CH1, TIM4_CH4, SAI1_D2, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, FDCAN1_TX, TIM8_CH3, TIM1_CH3N, HRTIM1_EEV5, SAI1_FS_A, EVENTOUT	-

Table 12. STM32G484xE pin definition (continued)

Pin Number								Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP81	UFQFPN48	LQFP48	LQFP64	LQFP80	TFBGA100	LPQF100	LPQF128						
-	-	-	-	-	C4	97	125	PE0	I/O	FT	-	TIM4_ETR, TIM20_CH4N, TIM16_CH1, TIM20_ETR, USART1_TX, FMC_NBL0, EVENTOUT	-
-	-	-	-	-	B3	98	126	PE1	I/O	FT	-	TIM17_CH1, TIM20_CH4, USART1_RX, FMC_NBL1, EVENTOUT	-
-	-	47	63	79	-	99	127	VSS	S	-	-	-	-
A9	48	48	64	80	-	100	128	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
3. After a backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs".
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.
5. It is recommended to set PB8 in another mode than analog mode after startup to limit consumption if the pin is left unconnected.

4.10 Alternate functions

Table 13. Alternate function

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/SYS_AF	LPTIM1/TIM2/5/15/16/17	I2C1/3/TIM1/2/3/4/5/8/20/15/COMP1	QUADSPI1/I2C3/4/SAI1/USB/HRTIM1/TIM8/20/15/COMP3	I2C1/2/3/4/TIM1/8/16/17	QUADSPI1/SPI1/2/3/4/I2S2/3/I2C4/UART4/5/TIM8/Infrared	QUADSPI1/SPI2/3/I2S2/3/TIM1/5/8/20/Infrared	USART1/2/3/FDCAN/COMP7/5/6	I2C3/4/UART4/5/LPUART1/COMP1/2/7/4/5/6/3	FDCAN/TIM1/8/15/FDCAN1/2	QUADSPI1/TIM2/3/4/8/17	LPTIM1/TIM1/8/FDCAN1/3	FMC/LPUART1/SAI1/HRTIM1/TIM1	SAI1SAI1/HRTIM1/OPAMP2	UART4/5/SAI1/TIM2/15/UCPD1	EVENT
Port A	PA0	-	TIM2_CH1	TIM5_CH1	-	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	TIM2_ETR	EVENTOUT
	PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS_DE	-	TIM15_CH1N	-	-	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	QUADSPI1_BK1_NCS	-	LPUART1_TX	-	UCPD1_FRSTX	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_RX	-	TIM15_CH2	QUADSPI1_CLK	-	LPUART1_RX	SAI1_MCLK_A	-	EVENTOUT
	PA4	-	-	TIM3_CH2	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PA5	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	UCPD1_FRSTX	EVENTOUT
	PA6	-	TIM16_CH1	TIM3_CH1	-	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	QUADSPI1_BK1_IO3	-	LPUART1_CTS	-	-	EVENTOUT
	PA7	-	TIM17_CH1	TIM3_CH2	-	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	COMP2_OUT	-	QUADSPI1_BK1_IO2	-	-	-	UCPD1_FRSTX	EVENTOUT
	PA8	MCO	-	I2C3_SCL	-	I2C2_SDA	I2S2_MCK	TIM1_CH1	USART1_CK	COMP7_OUT	-	TIM4_ETR	FDCAN3_RX	SAI1_CK2	HRTIM1_CHA1	SAI1_SCK_A	EVENTOUT
	PA9	-	-	I2C3_SMBA	-	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	-	-	HRTIM1_CHA2	SAI1_FS_A	EVENTOUT
	PA10	-	TIM17_BKIN	-	USB_CRS_SYNC	I2C2_SMBA	SPI2_MISO	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	TIM8_BKIN	SAI1_D1	HRTIM1_CHB1	SAI1_SD_A	EVENTOUT
	PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	COMP1_OUT	FDCAN1_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	HRTIM1_CHB2	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_RTS_DE	COMP2_OUT	FDCAN1_TX	TIM4_CH2	TIM1_ETR	-	HRTIM1_FLT1	-	EVENTOUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	I2C4_SCL	I2C1_SCL	IR_OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	SWCLK-JTCK	LPTIM1_OUT	-	I2C4_SMBA	I2C1_SDA	TIM8_CH2	TIM1_BKIN	USART2_TX	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	JTDI	TIM2_CH1	TIM8_CH1	-	I2C1_SCL	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_RX	UART4_RTS_DE	TIM1_BKIN	-	FDCAN3_TX	-	HRTIM1_FLT2	TIM2_ETR	EVENTOUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/SYS_AF	LPTIM1/TIM2/5/15/16/17	I2C1/3/TIM1/2/3/4/5/8/20/15/COMP1	QUADSPI1/I2C3/4/SAI1/USB/HRTIM1/TIM8/20/15/COMP3	I2C1/2/3/4/TIM1/8/16/17	QUADSPI1/SPI1/2/3/4/I2S2/3/I2C4/UART4/5/TIM8/Infrared	QUADSPI1/SPI2/3/I2S2/3/TIM1/5/8/20/Infrared	USART1/2/3/FDCAN/COMP7/5/6	I2C3/4/UART4/5/LPUART1/COMP1/2/7/4/5/6/3	FDCAN/TIM1/8/15/FDCAN1/2	QUADSPI1/TIM2/3/4/8/17	LPTIM1/TIM1/8/FDCAN1/3	FMC/LPUART1/SAI1/HRTIM1/TIM1	SAI1SAI1/HRTIM1/OPAMP2	UART4/5/SAI1/TIM2/15/UCPD1	EVENT
Port B	PB0	-	-	TIM3_CH3	-	TIM8_CH2N	-	TIM1_CH2N	-	-	-	QUADSPI1_BK1_IO1	-	-	HRTIM1_FLT5	UCPD1_FRSTX	EVENTOUT
	PB1	-	-	TIM3_CH4	-	TIM8_CH3N	-	TIM1_CH3N	-	COMP4_OUT	-	QUADSPI1_BK1_IO0	-	LPUART1_RTS_DE	HRTIM1_SCOUT	-	EVENTOUT
	PB2	RTC_OUT2	LPTIM1_OUT	TIM5_CH1	TIM20_CH1	I2C3_SMBA	-	-	-	-	-	QUADSPI1_BK2_IO1	-	-	HRTIM1_SCIN	-	EVENTOUT
	PB3	JTDO-TRACESWO	TIM2_CH2	TIM4_ETR	USB_CRS_SYNC	TIM8_CH1N	SPI1_SCK	SPI3_SCK/I2S3_CK	USART2_TX	-	-	TIM3_ETR	FDCAN3_RX	HRTIM1_SCOUT	HRTIM1_EEV9	SAI1_SCK_B	EVENTOUT
	PB4	JTRST	TIM16_CH1	TIM3_CH1	-	TIM8_CH2N	SPI1_MISO	SPI3_MISO	USART2_RX	UART5_RTS_DE	-	TIM17_BKIN	FDCAN3_TX	-	HRTIM1_EEV7	SAI1_MCLK_B	EVENTOUT
	PB5	-	TIM16_BKIN	TIM3_CH2	TIM8_CH3N	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI/I2S3_SD	USART2_CK	I2C3_SDA	FDCAN2_RX	TIM17_CH1	LPTIM1_IN1	SAI1_SD_B	HRTIM1_EEV6	UART5_CTS	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	-	-	TIM8_CH1	TIM8_ETR	USART1_TX	COMP4_OUT	FDCAN2_TX	TIM8_BKIN2	LPTIM1_ETR	HRTIM1_SCIN	HRTIM1_EEV4	SAI1_FS_B	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	I2C4_SDA	I2C1_SDA	TIM8_BKIN	-	USART1_RX	COMP3_OUT	-	TIM3_CH4	LPTIM1_IN2	FMC_NL	HRTIM1_EEV3	UART4_CTS	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	SAI1_CK1	I2C1_SCL	-	-	USART3_RX	COMP1_OUT	FDCAN1_RX	TIM8_CH2	-	TIM1_BKIN	HRTIM1_EEV8	SAI1_MCLK_A	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	SAI1_D2	I2C1_SDA	-	IR_OUT	USART3_TX	COMP2_OUT	FDCAN1_TX	TIM8_CH3	-	TIM1_CH3N	HRTIM1_EEV5	SAI1_FS_A	EVENTOUT
	PB10	-	TIM2_CH3	-	-	-	-	-	USART3_TX	LPUART1_RX	-	QUADSPI1_CLK	-	TIM1_BKIN	HRTIM1_FLT3	SAI1_SCK_A	EVENTOUT
	PB11	-	TIM2_CH4	-	-	-	-	-	USART3_RX	LPUART1_TX	-	QUADSPI1_BK1_NCS	-	-	HRTIM1_FLT4	-	EVENTOUT
	PB12	-	-	TIM5_ETR	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	LPUART1_RTS_DE	FDCAN2_RX	-	-	-	HRTIM1_CHC1	-	EVENTOUT
	PB13	-	-	-	-	-	SPI2_SCK/I2S2_CK	TIM1_CH1N	USART3_CTS	LPUART1_CTS	FDCAN2_TX	-	-	-	HRTIM1_CHC2	-	EVENTOUT
	PB14	-	TIM15_CH1	-	-	-	SPI2_MISO	TIM1_CH2N	USART3_RTS_DE	COMP4_OUT	-	-	-	-	HRTIM1_CHD1	-	EVENTOUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	COMP3_OUT	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	HRTIM1_CHD2	-	EVENTOUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/ SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C1/3/ TIM1/2/3/4/5/8/ 20/15/ COMP1	QUADSPI1/ I2C3/4/SAI1/US B/HRTIM1/ TIM8/20/15/ COMP3	I2C1/2/3/ 4/TIM1/8/ 16/17	QUADSPI1 /SPI1/2/3/4/ I2S2/3/I2C4/ UART4/5/ TIM8/ Infrared	QUADSPI1/ SPI2/3/I2S2 /3/TIM1/5/8/ 20/Infrared	USART1/2/3 /FDCAN/CO MP7/5/6	I2C3/4/UAR T4/5/LPUA RT1/COMP 1/2/7/4/5/6/ 3	FDCAN/T IM1/8/15/ FDCAN1/ 2	QUADSPI1/ TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/F DCAN1/3	FMC/LPUART1 /SAI1/HRTIM1/ TIM1	SAI1SAI1/HR TIM1/OPAMP 2	UART4/5/ SAI1/TIM 2/15/ UCPD1	EVENT
Port C	PC0	-	LPTIM1_IN1	TIM1_CH1	-	-	-	-	-	LPUART1_ RX	-	-	-	-	-	-	EVENT OUT
	PC1	-	LPTIM1_OUT	TIM1_CH2	-	-	-	-	-	LPUART1_ TX	-	QUADSPI1_ BK2_IO0	-	-	SAI1_SD_A	-	EVENT OUT
	PC2	-	LPTIM1_IN2	TIM1_CH3	COMP3_OUT	-	-	TIM20_CH2	-	-	-	QUADSPI1_ BK2_IO1	-	-	-	-	EVENT OUT
	PC3	-	LPTIM1_ETR	TIM1_CH4	SAI1_D1	-	-	TIM1_ BKIN2	-	-	-	QUADSPI1_ BK2_IO2	-	-	SAI1_SD_A	-	EVENT OUT
	PC4	-	-	TIM1_ETR	-	I2C2_ SCL	-	-	USART1_ TX	-	-	QUADSPI1_ BK2_IO3	-	-	-	-	EVENT OUT
	PC5	-	-	TIM15_BKIN	SAI1_D3	-	-	TIM1_ CH4N	USART1_ RX	-	-	-	-	-	HRTIM1_ EEV10	-	EVENT OUT
	PC6	-	-	TIM3_CH1	HRTIM1_EEV10	TIM8_ CH1	-	I2S2_MCK	COMP6_ OUT	I2C4_SCL	-	-	-	-	HRTIM1_ CHF1	-	EVENT OUT
	PC7	-	-	TIM3_CH2	HRTIM1_FLT5	TIM8_ CH2	-	I2S3_MCK	COMP5_ OUT	I2C4_SDA	-	-	-	-	HRTIM1_ CHF2	-	EVENT OUT
	PC8	-	-	TIM3_CH3	HRTIM1_CHE1	TIM8_ CH3	-	TIM20_CH3	COMP7_ OUT	I2C3_SCL	-	-	-	-	-	-	EVENT OUT
	PC9	-	-	TIM3_CH4	HRTIM1_CHE2	TIM8_ CH4	I2SCKIN	TIM8_ BKIN2	-	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC10	-	-	-	-	TIM8_ CH1N	UART4_TX	SPI3_SCK/ I2S3_CK	USART3_ TX	-	-	-	-	-	HRTIM1_ FLT6	-	EVENT OUT
	PC11	-	-	-	HRTIM1_EEV2	TIM8_ CH2N	UART4_RX	SPI3_MISO	USART3_ RX	I2C3_SDA	-	-	-	-	-	-	EVENT OUT
	PC12	-	TIM5_CH2	-	HRTIM1_EEV1	TIM8_ CH3N	UART5_TX	SPI3_MOSI /I2S3_SD	USART3_ CK	-	-	-	-	-	-	UCPD1_ FRSTX	EVENT OUT
	PC13	-	-	TIM1_BKIN	-	TIM1_ CH1N	-	TIM8_ CH4N	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/ SYS_AF	LPTIM1/ TIM2/5/ 15/16/17	I2C1/3/ TIM1/2/3/4/5/8/ 20/15/ COMP1	QUADSPI1/ I2C3/4/SAI1/US B/HRTIM1/ TIM8/20/15/ COMP3	I2C1/2/3/ 4/TIM1/8/ 16/17	QUADSPI1 /SPI1/2/3/4/ I2S2/3/I2C4/ UART4/5/ TIM8/ Infrared	QUADSPI1/ SPI2/3/I2S2 /3/TIM1/5/8/ 20/Infrared	USART1/2/3 /FDCAN/CO MP7/5/6	I2C3/4/UAR T4/5/LPUA RT1/COMP 1/2/7/4/5/6/ 3	FDCAN/T IM1/8/15/ FDCAN1/ 2	QUADSPI1/ TIM2/3/4/8/1 7	LPTIM1/ TIM1/8/F DCAN1/3	FMC/LPUART1 /SAI1/HRTIM1/ TIM1	SAI1SAI1/HR TIM1/OPAMP 2	UART4/5/ SAI1/TIM 2/15/ UCPD1	EVENT
Port D	PD0	-	-	-	-	-	-	TIM8_ CH4N	-	-	FDCAN1 _RX	-	-	FMC_D2	-	-	EVENT OUT
	PD1	-	-	-	-	TIM8_ CH4	-	TIM8_ BKIN2	-	-	FDCAN1 _TX	-	-	FMC_D3	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	-	TIM8_ BKIN	UART5_RX	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD3	-	-	TIM2_CH1/ TIM2_ETR	-	-	-	-	USART2_ CTS	-	-	QUADSPI1 _BK2_NCS	-	FMC_CLK	-	-	EVENT OUT
	PD4	-	-	TIM2_CH2	-	-	-	-	USART2_ RTS_DE	-	-	QUADSPI1_ BK2_IO0	-	FMC_NOE	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	-	USART2_ TX	-	-	QUADSPI1_ BK2_IO1	-	FMC_NWE	-	-	EVENT OUT
	PD6	-	-	TIM2_CH4	SAI1_D1	-	-	-	USART2_ RX	-	-	QUADSPI1_ BK2_IO2	-	FMC_NWAIT	SAI1_SD_A	-	EVENT OUT
	PD7	-	-	TIM2_CH3	-	-	-	-	USART2_ CK	-	-	QUADSPI1_ BK2_IO3	-	FMC_NCE/ FMC_NE1	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	USART3_ TX	-	-	-	-	FMC_D13	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	USART3_ RX	-	-	-	-	FMC_D14	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	USART3_ CK	-	-	-	-	FMC_D15	-	-	EVENT OUT
	PD11	-	TIM5_ETR	-	-	I2C4_ SMBA	-	-	USART3_ CTS	-	-	-	-	FMC_A16	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_ RTS_DE	-	-	-	-	FMC_A17	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	FMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	SPI2_NSS	-	-	-	-	-	FMC_D1	-	-	EVENT OUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/SYS_AF	LPTIM1/TIM2/5/15/16/17	I2C1/3/TIM1/2/3/4/5/8/20/15/COMP1	QUADSPI1/I2C3/4/SAI1/USB/HRTIM1/TIM8/20/15/COMP3	I2C1/2/3/4/TIM1/8/16/17	QUADSPI1/SPI1/2/3/4/I2S2/3/I2C4/UART4/5/TIM8/Infrared	QUADSPI1/SPI2/3/I2S2/3/TIM1/5/8/20/Infrared	USART1/2/3/FDCAN/COMP7/5/6	I2C3/4/UART4/5/LPUART1/COMP1/2/7/4/5/6/3	FDCAN/TIM1/8/15/FDCAN1/2	QUADSPI1/TIM2/3/4/8/17	LPTIM1/TIM1/8/FDCAN1/3	FMC/LPUART1/SAI1/HRTIM1/TIM1	SAI1SAI1/HRTIM1/OPAMP2	UART4/5/SAI1/TIM2/15/UCPD1	EVENT
Port E	PE0	-	-	TIM4_ETR	TIM20_CH4N	TIM16_CH1	-	TIM20_ETR	USART1_TX	-	FDCAN1_RXFD	-	-	FMC_NBL0	-	-	EVENTOUT
	PE1	-	-	-	-	TIM17_CH1	-	TIM20_CH4	USART1_RX	-	-	-	-	FMC_NBL1	-	-	EVENTOUT
	PE2	TRACECK	-	TIM3_CH1	SAI1_CK1	-	SPI4_SCK	TIM20_CH1	-	-	-	-	-	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	TRACED0	-	TIM3_CH2	-	-	SPI4_NSS	TIM20_CH2	-	-	-	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	TRACED1	-	TIM3_CH3	SAI1_D2	-	SPI4_NSS	TIM20_CH1N	-	-	-	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	TRACED2	-	TIM3_CH4	SAI1_CK2	-	SPI4_MISO	TIM20_CH2N	-	-	-	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	TRACED3	-	-	SAI1_D1	-	SPI4_MOSI	TIM20_CH3N	-	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	TIM5_CH3	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	TIM5_CH4	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	-	TIM1_CH2N	-	-	-	-	-	-	-	QUADSPI1_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	-	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	QUADSPI1_BK1_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	-	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	QUADSPI1_BK1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	-	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	QUADSPI1_BK1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	QUADSPI1_BK1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	TIM1_BKIN	-	-	-	TIM1_CH4N	USART3_RX	-	-	QUADSPI1_BK1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/ SYS_AF	**LPTIM1/ TIM2/5/ 15/16/17**	**I2C1/3/ TIM1/2/3/4/5/8/ 20/15/ COMP1**	**QUADSPI1/ I2C3/4/SAI1/USB/HRTIM1/ TIM8/20/15/ COMP3**	**I2C1/2/3/ 4/TIM1/8/ 16/17**	**QUADSPI1 /SPI1/2/3/4/ I2S2/3/I2C4/ UART4/5/ TIM8/ Infrared**	**QUADSPI1/ SPI2/3/I2S2 /3/TIM1/5/8/ 20/Infrared**	**USART1/2/3 /FDCAN/COMP7/5/6**	**I2C3/4/UART4/5/LPUART1/COMP1/2/7/4/5/6/3**	**FDCAN/TIM1/8/15/ FDCAN1/2**	**QUADSPI1/ TIM2/3/4/8/17**	**LPTIM1/ TIM1/8/FDCAN1/3**	**FMC/LPUART1 /SAI1/HRTIM1/ TIM1**	**SAI1SAI1/HRTIM1/OPAMP2**	**UART4/5/ SAI1/TIM2/15/ UCPD1**	**EVENT**
Port F	PF0	-	-	-	-	I2C2_ SDA	SPI2_NSS/ I2S2_WS	TIM1_ CH3N	-	-	-	-	-	-	-	-	EVENT OUT
	PF1	-	-	-	-	-	SPI2_SCK/ I2S2_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF2	-	-	TIM20_CH3	-	I2C2_ SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	TIM20_CH4	-	I2C3_ SCL	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	COMP1_OUT	TIM20_CH1N	I2C3_ SDA	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	TIM5_ETR	TIM4_CH4	SAI1_SD_B	I2C2_ SCL	-	TIM5_CH1	USART3_ RTS	-	-	QUADSPI1_ BK1_IO3	-	-	-	-	EVENT OUT
	PF7	-	-	TIM20_BKIN	-	-	-	TIM5_CH2	-	-	-	QUADSPI1_ BK1_IO2	-	FMC_A1	SAI1_MCLK_ B	-	EVENT OUT
	PF8	-	-	TIM20_BKIN2	-	-	-	TIM5_CH3	-	-	-	QUADSPI1_ BK1_IO0	-	FMC_A24	SAI1_SCK_B	-	EVENT OUT
	PF9	-	-	TIM20_BKIN	TIM15_CH1	-	SPI2_SCK	TIM5_CH4	-	-	-	QUADSPI1_ BK1_IO1	-	FMC_A25	SAI1_FS_B	-	EVENT OUT
	PF10	-	-	TIM20_BKIN2	TIM15_CH2	-	SPI2_SCK	-	-	-	-	QUADSPI1_ CLK	-	FMC_A0	SAI1_D3	-	EVENT OUT
	PF11	-	-	TIM20_ETR	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	EVENT OUT
	PF12	-	-	TIM20_CH1	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	TIM20_CH2	-	I2C4_ SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	TIM20_CH3	-	I2C4_ SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
	PF15	-	-	TIM20_CH4	-	I2C4_ SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT

Table 13. Alternate function (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		I2C4/SYS_AF	LPTIM1/TIM2/5/15/16/17	I2C1/3/TIM1/2/3/4/5/8/20/15/COMP1	QUADSPI1/I2C3/4/SAI1/USB/HRTIM1/TIM8/20/15/COMP3	I2C1/2/3/4/TIM1/8/16/17	QUADSPI1/SPI1/2/3/4/I2S2/3/I2C4/UART4/5/TIM8/Infrared	QUADSPI1/SPI2/3/I2S2/3/TIM1/5/8/20/Infrared	USART1/2/3/FDCAN/COMP7/5/6	I2C3/4/UART4/5/LPUART1/COMP1/2/7/4/5/6/3	FDCAN/TIM1/8/15/FDCAN1/2	QUADSPI1/TIM2/3/4/8/17	LPTIM1/TIM1/8/FDCAN1/3	FMC/LPUART1/SAI1/HRTIM1/TIM1	SAI1SAI1/HRTIM1/OPAMP2	UART4/5/SAI1/TIM2/15/UCPD1	EVENT
Port G	PG0	-	-	TIM20_CH1N	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	-	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	TIM20_CH3N	-	-	SPI1_SCK	-	-	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PG3	-	-	TIM20_BKIN	-	I2C4_SCL	SPI1_MISO	TIM20_CH4N	-	-	-	-	-	FMC_A13	-	-	EVENTOUT
	PG4	-	-	TIM20_BKIN2	-	I2C4_SDA	SPI1_MOSI	-	-	-	-	-	-	FMC_A14	-	-	EVENTOUT
	PG5	-	-	TIM20_ETR	-	-	SPI1_NSS	-	-	LPUART1_CTS	-	-	-	FMC_A15	-	-	EVENTOUT
	PG6	-	-	TIM20_BKIN	-	I2C3_SMBA	-	-	-	LPUART1_RTS_DE	-	-	-	FMC_INT	-	-	EVENTOUT
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	-	-	-	LPUART1_TX	-	-	-	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	-	-	-	-	I2C3_SDA	-	-	-	LPUART1_RX	-	-	-	FMC_NE3	-	-	EVENTOUT
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX	-	-	-	-	FMC_NCE/FMC_NE2	-	TIM15_CH1N	EVENTOUT
	PG10	MCO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, $V_{DD} = V_{DDA}$ = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 13*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 14*.

Figure 13. Pin loading conditions

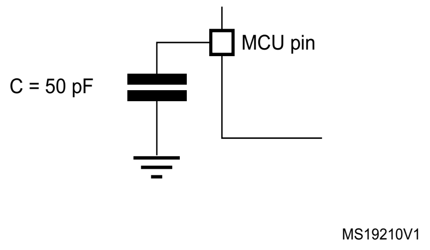
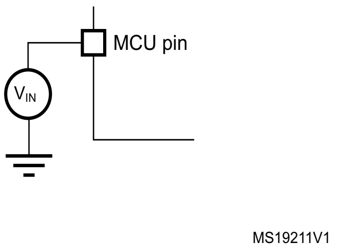
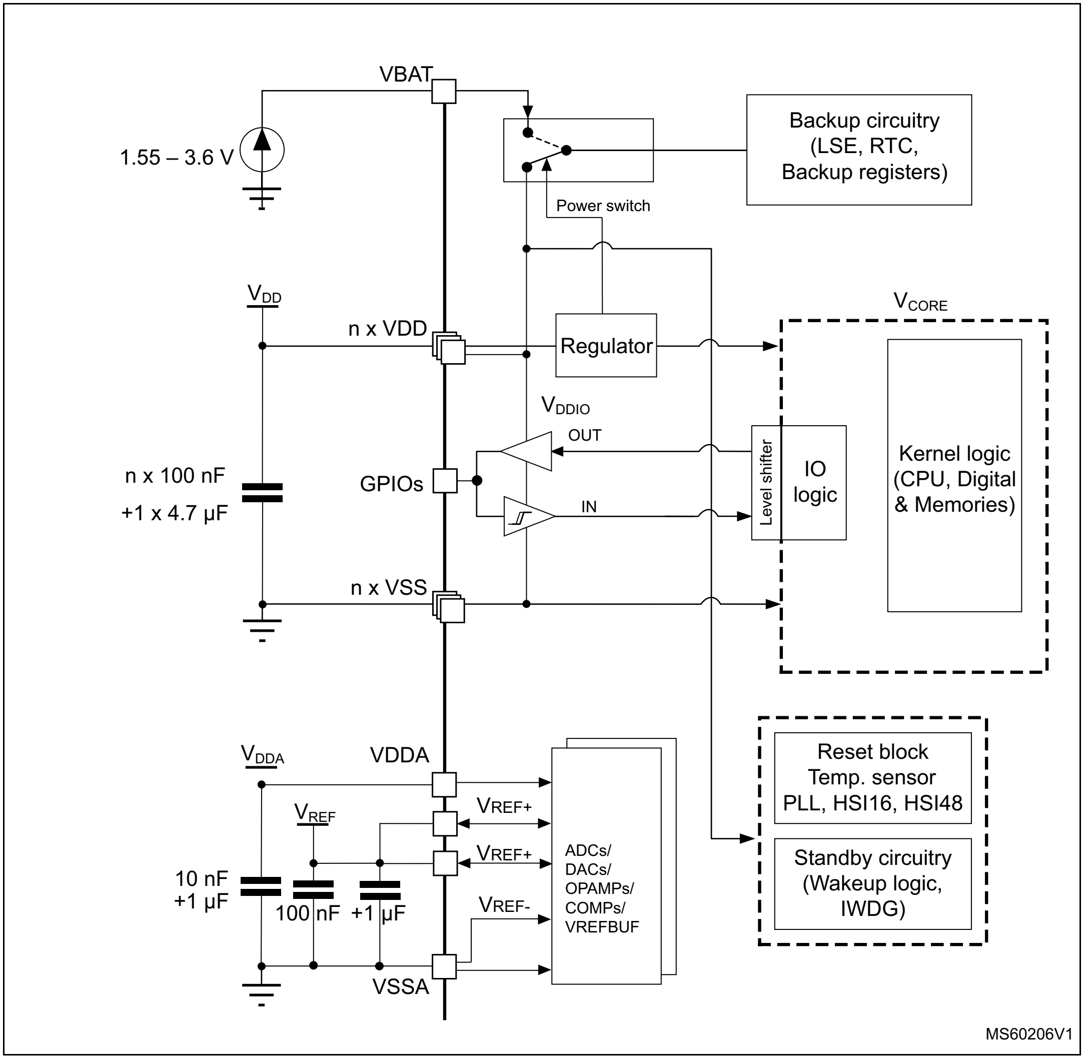


Figure 14. Pin input voltage



5.1.6 Power supply scheme

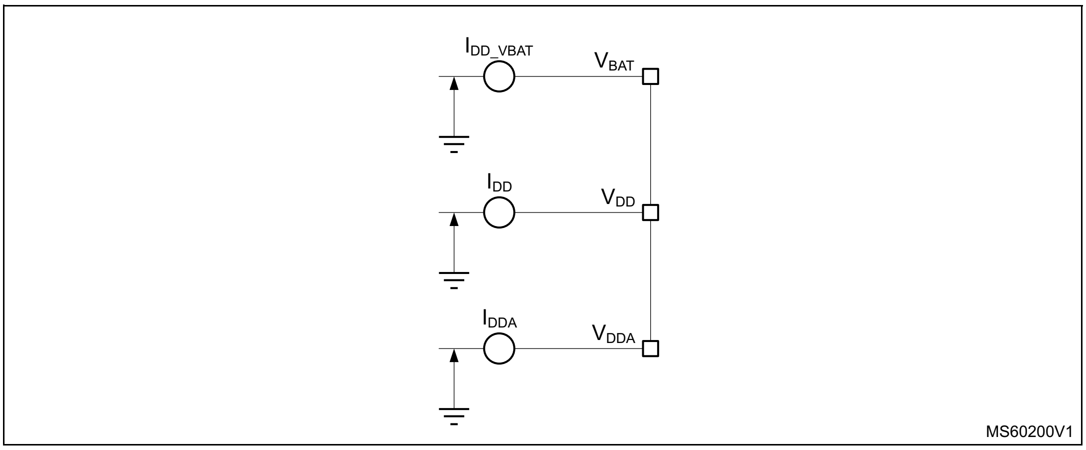
Figure 15. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

Figure 16. Current consumption measurement



The I_{DD_ALL} parameters given in *Table 21* to *Table 28* represent the total MCU consumption including the current supplying V_{DD}, V_{DDA} and V_{BAT}.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics* and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA} and V_{BAT})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_xxx pins except FT_c pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}) + 4.0(3)(4)	
	Input voltage on FT_c pins	V_{SS}-0.3	5.5	
	Input voltage on TT_xx pins	V_{SS}-0.3	4.0	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)	-	50	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 15: Current characteristics* for the maximum allowed injected current values.

3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 15. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	150	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100	
	Total output current sourced by sum of all I/Os and control pins(2)	100	
$I_{INJ(PIN)}$(3)	Injected current on FT_xxx, TT_xx, NRST pins	-5/0(4)	
$\sum \lvert I_{INJ(PIN)} \rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by VIN < VSS. IINJ(PIN) must never be exceeded. Refer also to *Table 14: Voltage characteristics* for the minimum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum \lvert I_{INJ(PIN)} \rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	170	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	170	
f_{PCLK2}	Internal APB2 clock frequency	-	0	170	
V_{DD}	Standard operating voltage	-	1.71(1)	3.6	V
V_{DDA}	Analog supply voltage	ADC	1.62	3.6	V
		DAC 1 MSPS or DAC 15 MSPS or OPAMP	1.8		
		COMP used	1.8	3.6	
		VREFBUF used	2.4	3.6	
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	V
V_{IN}	I/O input voltage	TT_xx	-0.3	V_{DD}+0.3	V
		FT_c	-0.3	5	
		All I/O except TT_xx and FT_c	-0.3	MIN(MIN(V_{DD}, V_{DDA})+3.6 V, 5.5 V)(2)(3)	
P_D	Power dissipation	See *Section 6.9: Thermal characteristics* for application appropriate thermal resistance and package. Power dissipation is then calculated according ambient temperature (T_A) and maximum junction temperature (T_J) and selected thermal resistance.			mW
P_D	Power dissipation	See *Section 6.9: Thermal characteristics* for application appropriate thermal resistance and package. Power dissipation is then calculated according to ambient temperature (T_A), maximum junction temperature (T_J) and selected thermal resistance.			mW
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	°C
		Low-power dissipation(4)	-40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	-40	125	
		Low-power dissipation(4)	-40	130	
T_J	Junction temperature range	Suffix 6 version	-40	105	°C
		Suffix 3 version	-40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.

2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA})+3.6 V and 5.5V.

3. For operation with voltage higher than Min (V_{DD}, V_{DDA}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 6.9: Thermal characteristics*).

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 18* are derived from tests performed under the ambient temperature condition summarized in *Table 17*.

Table 18. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 19* are derived from tests performed under the ambient temperature conditions summarized in *Table 17: General operating conditions*.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)(2)	BOR(3) (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM1}	V_{DDA} peripheral voltage monitoring (COMP/ADC)	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM2}	V_{DDA} peripheral voltage monitoring (OPAMP/DAC)	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM1}	PVM1 hysteresis	-	-	10	-	mV
V_{hyst_PVM2}	PVM2 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

5.3.4 Embedded voltage reference

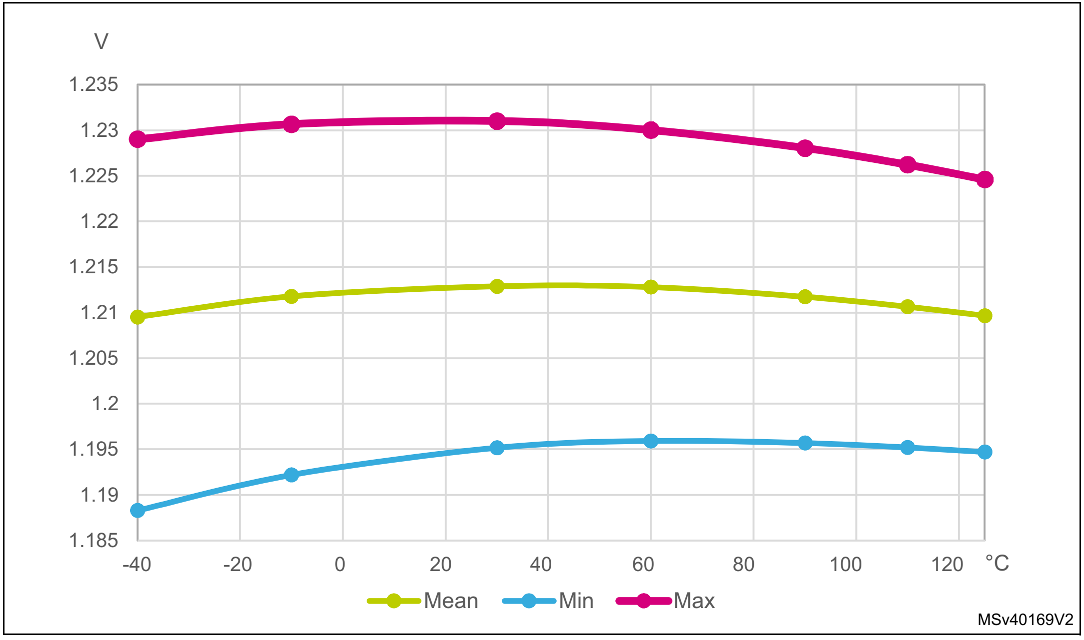
The parameters given in *Table 20* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 20. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Average temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	300	1000(2)	ppm
$V_{DDCoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time is determined in the application by multiple iterations.
2. Guaranteed by design.

Figure 17. V_{REFINT} versus temperature



5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code

The current consumption is measured as described in *Figure 16: Current consumption measurement*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “number of wait states according to CPU clock (HCLK) frequency” available in the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs").
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- The voltage scaling Range 1 is adjusted to f_{HCLK} frequency as follows:
  - Voltage Range 1 Boost mode for 150 MHz < $f_{HCLK} \leq$ 170 MHz
  - Voltage Range 1 Normal mode for 26 MHz < $f_{HCLK} \leq$ 150 MHz

The parameters given in *Table 21* to *Table 28* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 21. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.65	3.85	4.45	5.1	6.45	4.00	4.50	6.50	8.40	13.00	mA
				16 MHz	2.30	2.55	3.1	3.8	5.15	2.60	3.20	5.20	7.10	11.00	
				8 MHz	1.25	1.5	2.05	2.8	4.1	1.60	2.10	4.10	6.00	9.80	
				4 MHz	0.75	0.955	1.5	2.3	3.6	0.94	1.50	3.50	5.40	9.30	
				2 MHz	0.47	0.69	1.25	2	3.35	0.65	1.30	3.20	5.10	9.00	
				1 MHz	0.34	0.55	1.1	1.9	3.2	0.51	1.10	3.00	5.00	8.90	
				100 KHz	0.22	0.43	0.98	1.75	3.1	0.38	0.94	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	29.50	29.5	31	32	34.5	30.00	30.00	34.00	36.00	42.00	
			Range 1	150 MHz	24.50	26	27	28	30	25.00	27.00	29.00	32.00	37.00	
				120 MHz	19.50	20	20.5	21.5	23.5	20.00	21.00	23.00	25.00	31.00	
				80 MHz	13.00	13.5	14	15.5	17	14.00	14.00	16.00	19.00	24.00	
				72 MHz	12.00	12	13	14	15.5	13.00	13.00	16.00	18.00	23.00	
				64 MHz	10.50	11	11.5	12.5	14.5	11.00	12.00	14.00	16.00	22.00	
				48 MHz	7.90	8.2	9	9.7	11.5	8.40	9.00	12.00	14.00	20.00	
				32 MHz	5.40	5.65	6.4	7.2	8.85	5.80	6.50	9.00	12.00	17.00	
				24 MHz	4.10	4.35	5.1	5.95	7.6	4.50	5.20	7.80	11.00	16.00	
				16 MHz	2.80	3.1	3.8	4.7	6.3	3.20	3.90	6.50	8.90	14.00	

Table 21. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single Bank, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	455	725	1350	2250	3800	720	1500	3700	6000	11000	µA
				1 MHz	280	545	1200	2100	3600	570	1300	3500	5800	11000	
				250 KHz	160	435	1100	2000	3500	410	1100	3400	5700	10000	
				62.5 KHz	130	405	1050	1950	3500	390	1000	3400	5600	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	920	1200	1850	2750	4250	1300	2000	4200	6600	11000	
				1 MHz	780	1100	1700	2650	4150	1200	1900	4100	6500	11000	
				250 KHz	725	980	1600	2500	4050	1100	1800	4100	6400	11000	
				62.5 KHz	720	955	1600	2500	4000	1100	1700	4000	6300	11000	

Table 22. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.70	3.9	4.45	5.15	6.45	4.10	4.60	6.50	8.50	13.00	mA
				16 MHz	2.35	2.55	3.1	3.85	5.15	2.70	3.20	5.20	7.10	11.00	
				8 MHz	1.25	1.5	2.05	2.8	4.15	1.60	2.10	4.10	6.00	9.90	
				4 MHz	0.75	0.97	1.5	2.3	3.6	0.94	1.60	3.50	5.40	9.30	
				2 MHz	0.47	0.7	1.25	2.05	3.35	0.65	1.30	3.20	5.10	9.00	
				1 MHz	0.34	0.56	1.1	1.9	3.2	0.51	1.10	3.00	5.00	8.90	
				100 KHz	0.22	0.44	0.975	1.8	3.1	0.38	0.95	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	29.50	30	31	32	34.5	30.00	31.00	34.00	36.00	42.00	
			Range 1	150 MHz	24.50	24.5	25.5	26.5	28.5	25.00	26.00	28.00	30.00	35.00	
				120 MHz	19.50	20	20.5	22	23.5	20.00	21.00	23.00	26.00	31.00	
				80 MHz	13.00	13.5	14.5	15.5	17	14.00	14.00	17.00	19.00	24.00	
				72 MHz	12.00	12.5	13	14	15.5	13.00	13.00	16.00	18.00	23.00	
				64 MHz	10.50	11	11.5	13	14.5	11.00	12.00	14.00	17.00	22.00	
				48 MHz	7.95	8.3	9	10	11.5	8.50	9.10	12.00	15.00	20.00	
				32 MHz	5.40	5.7	6.45	7.25	8.9	5.80	6.50	9.10	12.00	17.00	
				24 MHz	4.10	4.4	5.1	6	7.65	4.50	5.30	7.80	11.00	16.00	
				16 MHz	2.85	3.15	3.8	4.75	6.35	3.20	4.00	6.50	8.90	14.00	

Table 22. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	450	725	1350	2250	3800	725	1500	3700	6000	11000	µA
				1 MHz	270	575	1200	2150	3650	575	1300	3500	5800	11000	
				250 KHz	185	460	1050	2000	3550	460	1100	3400	5700	11000	
				62.5 KHz	130	430	1050	2000	3500	430	1100	3400	5600	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	970	1200	1850	2750	4300	1200	2000	4200	6600	12000	
				1 MHz	800	1100	1700	2650	4150	1100	1900	4100	6500	11000	
				250 KHz	680	990	1600	2550	4050	990	1800	4100	6400	11000	
				62.5 KHz	695	965	1600	2500	4050	965	1700	4000	6400	11000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 23. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.65	3.85	4.4	5.25	6.8	4.00	4.60	6.50	8.40	13.00	mA
				16 MHz	2.75	2.95	3.5	4.35	5.9	3.10	3.70	5.50	7.50	12.00	
				8 MHz	1.50	1.65	2.2	3.05	4.55	1.70	2.40	4.20	6.10	10.00	
				4 MHz	0.84	1	1.55	2.35	3.9	1.10	1.70	3.60	5.50	9.30	
				2 MHz	0.51	0.68	1.2	2.05	3.55	0.70	1.40	3.20	5.10	9.00	
				1 MHz	0.34	0.51	1.05	1.85	3.35	0.53	1.20	3.10	4.90	8.80	
				100 KHz	0.20	0.36	0.895	1.7	3.2	0.38	0.99	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	20.00	20.5	21.5	22.5	24.5	21.00	22.00	25.00	27.00	47.00	
			Range 1	150 MHz	18.00	18.5	19	20	22	19.00	16.00	19.00	21.00	26.00	
				120 MHz	16.50	16.5	17.5	18.5	20.5	18.00	18.00	21.00	23.00	28.00	
				80 MHz	13.00	13	14	15	17	14.00	15.00	17.00	19.00	24.00	
				72 MHz	11.50	12	12.5	13.5	15.5	13.00	13.00	16.00	18.00	23.00	
				64 MHz	10.50	10.5	11.5	12.5	14.5	11.00	12.00	14.00	17.00	22.00	
				48 MHz	7.95	8.25	9	10	12	8.30	8.90	12.00	14.00	19.00	
				32 MHz	6.50	6.75	7.5	8.55	10.5	8.10	8.70	11.00	13.00	19.00	
				24 MHz	4.95	5.2	5.9	6.95	8.8	5.10	6.00	8.50	11.00	16.00	
				16 MHz	3.40	3.65	4.3	5.35	7.15	3.70	4.50	7.00	9.40	15.00	

Table 23. Current consumption in Run and Low-power run modes, code with data processing running from Flash in single bank, ART disable (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	505	700	1300	2250	3950	780	1500	3800	6000	11000	µA
				1 MHz	295	500	1100	2050	3750	540	1300	3600	5900	11000	
				250 KHz	145	350	970	1900	3600	410	1100	3400	5700	11000	
				62.5 KHz	110	310	935	1850	3550	380	1100	3400	5700	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	940	1150	1800	2700	4400	1300	2100	4400	6600	11000	
				1 MHz	830	1000	1600	2550	4250	1200	1900	4300	6500	11000	
				250 KHz	700	890	1500	2400	4100	1000	1800	4100	6400	11000	
				62.5 KHz	645	855	1450	2400	4100	1100	1800	4100	6400	11000	

Table 24. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.5	4.1	4.95	6.45	3.70	4.20	6.20	8.10	12.00	mA
				16 MHz	2.65	2.8	3.4	4.2	5.75	3.00	3.50	5.40	7.40	12.00	
				8 MHz	1.40	1.6	2.15	2.95	4.45	1.70	2.30	4.20	6.10	10.00	
				4 MHz	0.81	0.975	1.5	2.35	3.85	1.10	1.60	3.60	5.50	9.30	
				2 MHz	0.49	0.655	1.2	2	3.5	0.69	1.30	3.20	5.10	9.00	
				1 MHz	0.34	0.495	1.05	1.85	3.35	0.53	1.10	3.10	5.00	8.80	
				100 KHz	0.19	0.355	0.895	1.7	3.2	0.38	0.95	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	18.00	18	19	20	22	19.00	20.00	22.00	25.00	45.00	
			Range 1	150 MHz	16.00	16.5	17	18	20	17.00	18.00	20.00	22.00	27.00	
				120 MHz	14.50	15	15.5	16.5	18.5	16.00	16.00	18.00	21.00	26.00	
				80 MHz	12.00	12	13	14	15.5	13.00	13.00	16.00	18.00	23.00	
				72 MHz	10.50	11	11.5	12.5	14.5	12.00	12.00	15.00	17.00	22.00	
				64 MHz	9.45	9.7	10.5	11.5	13.5	9.90	11.00	13.00	16.00	21.00	
				48 MHz	7.25	7.55	8.25	9.3	11	7.50	8.20	11.00	14.00	18.00	
				32 MHz	6.15	6.4	7.1	8.15	10	6.60	7.30	9.80	13.00	18.00	
				24 MHz	4.70	4.95	5.65	6.65	8.5	5.10	5.80	8.30	11.00	16.00	
				16 MHz	3.20	3.45	4.15	5.15	6.95	3.60	4.40	6.80	9.30	15.00	

Table 24. Current consumption in Run and Low-power run modes, code with data processing running from Flash in dual bank, ART disable (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	480	665	1300	2200	3900	710	1400	3800	6000	11000	µA
				1 MHz	270	485	1100	2050	3750	540	1200	3600	5900	11000	
				250 KHz	145	340	965	1900	3600	410	1100	3400	5700	11000	
				62.5 KHz	120	310	930	1850	3550	380	1100	3400	5700	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	990	1150	1750	2700	4350	1300	2000	4400	6600	11000	
				1 MHz	830	995	1600	2550	4200	1200	1900	4300	6500	11000	
				250 KHz	720	880	1500	2400	4100	1100	1700	4100	6400	11000	
				62.5 KHz	660	845	1450	2400	4050	1100	1700	4100	6400	11000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	3.35	3.55	4.1	4.95	6.45	3.70	4.30	6.20	8.10	12.00	mA
				16 MHz	2.15	2.35	2.9	3.7	5.25	2.50	3.00	4.90	6.90	11.00	
				8 MHz	1.15	1.35	1.9	2.7	4.2	1.40	2.00	3.90	5.90	9.70	
				4 MHz	0.69	0.855	1.4	2.2	3.7	0.89	1.50	3.40	5.30	9.20	
				2 MHz	0.43	0.595	1.15	1.95	3.45	0.63	1.20	3.10	5.10	8.90	
				1 MHz	0.30	0.47	1	1.8	3.3	0.50	1.10	3.00	4.90	8.80	
				100 KHz	0.19	0.355	0.89	1.7	3.2	0.38	0.94	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	26.00	26.5	27.5	28.5	30.5	28.00	28.00	30.00	33.00	38.00 [2]	
			Range 1	150 MHz	21.50	22	22.5	23.5	25.5	23.00	23.00	25.00	28.00	33.00 [2]	
				120 MHz	17.50	17.5	18.5	19.5	21.5	19.00	19.00	21.00	24.00	28.00	
				80 MHz	11.50	12	12.5	13.5	15.5	13.00	13.00	16.00	18.00	23.00	
				72 MHz	10.50	11	11.5	12.5	14.5	12.00	12.00	14.00	17.00	22.00	
				64 MHz	9.45	9.7	10.5	11.5	13.5	9.90	11.00	13.00	16.00	21.00	
				48 MHz	7.25	7.5	8.2	9.25	11	7.60	8.20	11.00	14.00	18.00	
				32 MHz	4.90	5.15	5.85	6.9	8.7	5.40	6.10	8.60	11.00	16.00	
				24 MHz	3.75	4	4.7	5.7	7.5	4.20	4.90	7.40	9.80	15.00	
				16 MHz	2.60	2.85	3.5	4.5	6.3	3.00	3.70	6.20	8.60	14.00	

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1 (continued)

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX[1]					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	365	570	1200	2150	3850	640	1400	3700	6000	11000	µA
				1 MHz	240	425	1050	2000	3650	500	1200	3500	5800	11000	
				250 KHz	135	315	945	1850	3550	390	1100	3400	5700	11000	
				62.5 KHz	105	285	915	1850	3550	350	990	3300	5600	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	835	1050	1650	2600	4300	1300	1900	4300	6600	11000	
				1 MHz	775	940	1550	2500	4150	1200	1800	4200	6400	11000	
				250 KHz	640	860	1450	2400	4100	1100	1700	4100	6400	11000	
				62.5 KHz	640	830	1450	2350	4050	1100	1700	4100	6300	11000	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 26. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
IDD (Run)	Supply current in Run mode	$f_{HCLK}=f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26MHz	Reduced code(1)	3.65	3.7	mA	140	142	µA/MHz
				Coremark	3.65	3.7		140	142	
				Dhrystone2.1	3.65	3.7		140	142	
				Fibonacci	4.55	4.2		175	162	
				While(1)	2.90	3		112	115	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	24.5	24.5	mA	163	163	µA/MHz
				Coremark	24	24		160	160	
				Dhrystone2.1	24.5	24.5		163	163	
				Fibonacci	22.5	28		150	187	
				While(1)	19.5	20		130	133	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	29.5	29.5	mA	174	174	µA/MHz
				Coremark	29	29		171	171	
				Dhrystone2.1	29.5	29.5		174	174	
				Fibonacci	38	35		224	206	
				While(1)	23.5	24		138	141	

Table 26. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 f_{HCLK} = 2 MHz all peripherals disable		Reduced code(1)	920	970	µA	460	485	µA/MHz
				Coremark	905	985		453	493	
				Dhrystone2.1	915	915		458	458	
				Fibonacci	1,050	950		525	475	
				While(1)	930	875		465	438	

1. Reduced code used for characterization results provided in *Table 21*, *Table 23*, *Table 25*.

Table 27. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK}= 26 MHz	Reduced code(1)	3.55	3.25	mA	137	125	µA/MHz
				Coremark	3.45	3.2		133	123	
				Dhrystone2.1	3.55	3.25		137	125	
				Fibonacci	3.40	3		131	115	
				While(1)	2.90	2.95		112	113	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	18.50	16.00	mA	123	107	µA/MHz
				Coremark	17.50	15.50		117	103	
				Dhrystone2.1	18.50	16.00		123	107	
				Fibonacci	16.50	14.50		110	97	
				While(1)	19.50	19.50		130	130	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	20.50	18.00	mA	121	106	µA/MHz
				Coremark	20.00	17.50		118	103	
				Dhrystone2.1	20.50	18.00		121	106	
				Fibonacci	18.50	16.50		109	97	
				While(1)	23.50	24.00		138	141	

Table 27. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD} (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 f_{HCLK} = 2 MHz all peripherals disable		Reduced code[1]	970	1,000	µA	485	500	µA/MHz
				Coremark	985	1,000		493	500	
				Dhrystone2.1	985	955		493	478	
				Fibonacci	1,050	990		525	495	
				While(1)	920	875		460	438	

1. Reduced code used for characterization results provided in the first tables.

Table 28. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions		Code	TYP	Unit	TYP	Unit
		-	Voltage scaling		25°C		25°C	
IDD (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 M Hz	Reduced code(1)	3.25	mA	125	µA/MHz
				Coremark	3.35		129	
				Dhrystone2.1	3.30		127	
				Fibonacci	3.30		127	
				While(1)	3.40		131	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	21.50	mA	143	µA/MHz
				Coremark	22.50		150	
				Dhrystone2.1	21.50		143	
				Fibonacci	22.50		150	
				While(1)	20.00		133	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	26.00	mA	153	µA/MHz
				Coremark	27.00		159	
				Dhrystone2.1	26.00		153	
				Fibonacci	27.50		162	
				While(1)	24.50		144	
IDD (LPRun)	Supply current in Low-power run	f_{HCLK} = f_{HSE} = 2 MHz all peripherals disable		Reduced code(1)	955	µA	478	µA/MHz
				Coremark	890		445	
				Dhrystone2.1	915		458	
				Fibonacci	880		440	
				While(1)	905		453	

1. Reduced code used for characterization results provided in *Table 21*, *Table 23*, *Table 25*.

Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM2

Symbol	Parameter	Conditions		f_{HCLK}	TYP	Unit	TYP	Unit
		-	Voltage scaling		Single bank mode		Single bank mode	
IDD (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 M Hz	Reduced code[(1)]	2.65	mA	102	µA/MHz
				Coremark	2.80		108	
				Dhrystone2.1	2.65		102	
				Fibonacci	2.60		100	
				While(1)	2.45		94	
			Range 1 f_{HCLK}= 150 MHz	Reduced code[(1)]	17.50	mA	117	µA/MHz
				Coremark	18.00		120	
				Dhrystone2.1	17.50		117	
				Fibonacci	17.00		113	
				While(1)	16		107	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code[(1)]	21.00	mA	124	µA/MHz
				Coremark	22.00		129	
				Dhrystone2.1	21.00		124	
				Fibonacci	20.50		121	
				While(1)	19.50		115	
IDD (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 F_{HCLK} = 2MHz all peripherals disable		Reduced code[(1)]	890	µA	445	µA/MHz
				Coremark	830		415	
				Dhrystone2.1	825		413	
				Fibonacci	830		415	
				While(1)	815		408	

1. Reduced code used for characterization results provided in *Table 21*, *Table 23*, *Table 25*.

Table 30. Typical current consumption in Run and Low-power run modes, with different codes running from CCMSRAM

Symbol	Parameter	Conditions		f_{HCLK}	TYP	Unit	TYP	Unit
		-	Voltage scaling		Single bank mode		Single bank mode	
IDD (Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	Range2 f_{HCLK}=26 M Hz	Reduced code(1)	2.75	mA	106	µA/MHz
				Coremark	2.85		110	
				Dhrystone2.1	2.75		106	
				Fibonacci	2.95		113	
				While(1)	2.60		100	
			Range 1 f_{HCLK}= 150 MHz	Reduced code(1)	18.00	mA	120	µA/MHz
				Coremark	18.50		123	
				Dhrystone2.1	18.00		120	
				Fibonacci	19.00		127	
				While(1)	17.00		113	
			Range 1 Boost mode f_{HCLK}= 170 MHz	Reduced code(1)	22.00	mA	129	µA/MHz
				Coremark	22.50		132	
				Dhrystone2.1	22.00		129	
				Fibonacci	23.50		138	
				While(1)	20.50		121	
IDD (LPRun)	Supply current in Low-power run	SYSCLK source is HSI16 F_{HCLK} = 2MHz all peripherals disable		Reduced code(1)	900	µA	450	µA/MHz
				Coremark	850		425	
				Dhrystone2.1	870		435	
				Fibonacci	850		425	
				While(1)	810		405	

1. Reduced code used for characterization results provided in *Table 21*, *Table 23*, *Table 25*.

Table 31. Current consumption in Sleep and Low-power sleep mode Flash ON

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.98	1.1	1.75	2.4	3.75	1.40	2.00	4.00	5.90	9.80	mA
				16 MHz	0.67	0.835	1.45	2.15	3.5	1.10	1.60	3.60	5.50	9.40	
				8 MHz	0.44	0.605	1.25	2	3.35	0.71	1.30	3.30	5.20	9.00	
				4 MHz	0.33	0.5	1.1	1.9	3.25	0.55	1.20	3.10	5.00	8.90	
				2 MHz	0.27	0.445	1.05	1.85	3.2	0.46	1.10	3.00	4.90	8.80	
				1 MHz	0.24	0.415	1.05	1.8	3.15	0.41	0.97	2.90	4.80	8.70	
				100 KHz	0.21	0.385	0.995	1.8	3.1	0.37	0.93	2.90	4.80	8.70	
			Range 1 Boost mode	170 MHz	6.60	6.95	7.8	8.9	10.5	8.60	8.80	11.00	14.00	19.00	
			Range 1	150 MHz	5.50	5.8	6.55	7.55	9.25	6.80	7.30	9.00	12.00	17.00	
				120 MHz	4.50	4.75	5.5	6.55	8.2	5.80	6.20	8.00	11.00	16.00	
				80 MHz	3.15	3.45	4.2	5.15	6.8	4.50	4.20	6.70	9.10	14.00	
				72 MHz	2.85	3.15	3.9	4.9	6.55	3.90	3.90	6.40	8.80	14.00	
				64 MHz	2.60	2.9	3.65	4.6	6.3	3.60	3.60	6.10	8.60	14.00	
				48 MHz	1.90	2.2	3	3.65	5.3	3.00	3.10	5.60	8.00	13.00	
				32 MHz	1.40	1.65	2.4	3.2	4.85	1.90	2.70	5.20	7.60	13.00	
				24 MHz	1.10	1.35	2.1	3	4.65	1.60	2.40	4.90	7.30	13.00	
				16 MHz	0.83	1.1	1.85	2.75	4.35	1.30	2.10	4.60	7.00	12.00	

Table 31. Current consumption in Sleep and Low-power sleep mode Flash ON (continued)

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPRun)	Supply current in Low-power run mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	205	430	1150	2050	3600	1700	2700	3500	5700	11000	µA
				1 MHz	165	400	1100	2000	3550	940	2200	3400	5700	11000	
				250 KHz	145	370	1100	2000	3550	370	1100	3400	5700	11000	
				62.5 KHz	140	365	1050	2000	3550	360	1100	3400	5600	11000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	700	925	1650	2550	4100	1100	1900	4300	6300	11000	µA
				1 MHz	710	925	1600	2550	4100	1100	1800	4300	6300	11000	
				250 KHz	670	910	1600	2500	4050	1100	1800	4200	6300	11000	
				62.5 KHz	685	910	1600	2500	4050	1100	1800	4000	6300	11000	

Table 32. Current consumption in low-power sleep modes, Flash in power-down

Symbol	Parameter	Condition		f_{HCLK}	Typ					Max					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (LPSleep)	Supply current in low-power sleep mode	SYSCLK source is HSE in bypass mode all peripherals disable		2 MHz	210	385	1150	2050	3550	460	1200	3500	5700	11000	µA
				1 MHz	150	360	1100	2000	3550	410	1100	3400	5600	11000	
				250 KHz	120	330	1050	2000	3500	370	1100	3400	5600	11000	
				62.5 KHz	110	330	1050	1950	3500	360	1100	3300	5600	10000	
		SYSCLK source is HSI16 all peripherals disable		2 MHz	675	900	1600	2500	4050	1100	1800	4200	6400	11000	
				1 MHz	695	890	1600	2500	4050	1100	1800	4100	6300	11000	
				250 KHz	640	885	1600	2500	4050	1100	1800	4100	6300	11000	
				62.5 KHz	690	880	1600	2500	4050	990	1600	3500	5400	9300	

Table 33. Current consumption in Stop 1 mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	VDD	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD (Stop 1)	Supply current in Stop 1 mode, RTC disabled	RTC disabled	1.8 V	80	250	830	1550	2850	230	770	2400	4600	6000	µA
			2.4 V	80	250	835	1600	2850	230	780	2400	4600	8400	
			3.0 V	80.5	255	840	1600	2900	230	780	2400	4600	8400	
			3.6 V	81.5	255	845	1600	2900	240	780	2400	4600	8400	
IDD (Stop 1 with RTC)	Supply current in Stop 1 mode, RTC enabled	RTC clocked by LSI	1.8 V	80.5	255	830	1550	2850	230	770	2400	4600	11000	
			2.4 V	81	255	835	1600	2850	230	770	2400	4600	11000	
			3.0 V	81.5	255	835	1600	2850	230	780	2400	4600	11000	
			3.6 V	82	255	845	1600	2900	240	780	2400	4600	11000 (2)	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	80	255	830	1550	2850	-	-	-	-	-	
			2.4 V	80.5	255	830	1600	2850	-	-	-	-	-	
			3.0 V	81.5	255	835	1600	2900	-	-	-	-	-	
			3.6 V	83	260	845	1600	2900	-	-	-	-	-	
		RTC clocked by LSE quartz in low drive mode at 32768 Hz	1.8 V	83.5	220	655	1300	-	-	-	-	-	-	
			2.4 V	84	220	660	1300	-	-	-	-	-	-	
			3.0 V	84.5	220	660	1300	-	-	-	-	-	-	
			3.6 V	87	220	660	1300	-	-	-	-	-	-	
IDD (wakeup from Stop 1	Supply current during wakeup from Stop 1 mode	Wakeup clock is HSI6, voltage Range 1	3.0 V	1.73	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is HSI6 = 4 MHz, (HPRE = 4), voltage Range 2	3.0 V	1.29	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production

Table 34. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Stop 0)	Supply current in Stop 0 mode, RTC disabled	-	1.8 V	190	380	980	1750	3100	350	920	2700	5000	12000	µA
			2.4 V	190	380	985	1750	3100	350	930	2700	5100	12000	
			3 V	190	380	985	1750	3100	350	940	2700	5100	12000	
			3.6 V	190	380	985	1750	3100	360	940	2700	5200	12000 (2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

Table 35. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	No independent watchdog	1.8 V	100	275	1350	3450	8450	270	1800	4700	8800	24000	nA
			2.4 V	110	325	1600	4100	10000	290	2100	5200	11000	28000	
			3 V	130	385	1900	4850	12000	350	2300	6200	12000	32000	
			3.6 V	180	530	2400	6050	14500	670	2400	7200	14000	38000 (2)	
		With independent watchdog	1.8 V	300	-	-	-	-	-	-	-	-	-	
			2.4 V	365	-	-	-	-	-	-	-	-	-	
			3 V	435	-	-	-	-	-	-	-	-	-	
			3.6 V	545	-	-	-	-	-	-	-	-	-	

Table 35. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	540	725	1800	3850	8850	770	1900	4900	9300	25000	nA
			2.4 V	700	920	2150	4650	10500	960	3900	5800	11000	29000	
			3 V	885	1150	2650	5550	12500	1300	4500	7000	13000	33000	
			3.6 V	1100	1450	3350	7000	15500	1600	5100	8200	15000	39000	
		RTC clocked by LSI, with independent watchdog	1.8 V	580	-	-	-	-	-	-	-	-	-	
			2.4 V	760	-	-	-	-	-	-	-	-	-	
			3 V	960	-	-	-	-	-	-	-	-	-	
			3.6 V	1200	-	-	-	-	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768 Hz	1.8 V	410	580	1600	3650	8600	-	-	-	-	-	nA
			2.4 V	545	750	1950	4450	10500	-	-	-	-	-	
			3 V	830	1150	2750	5800	13000	-	-	-	-	-	
			3.6 V	2200	3050	5550	9550	18000	-	-	-	-	-	
		RTC clocked by LSE quartz(3) in low drive mode	1.8 V	370	570	1350	3150	7100	-	-	-	-	-	
			2.4 V	495	715	1650	3800	8350	-	-	-	-	-	
			3 V	655	915	2100	4550	9850	-	-	-	-	-	
			3.6 V	875	1350	2800	5750	12000	-	-	-	-	-	
I_{DD} (SRAM2)(4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	300	825	2950	6300	12550	-	-	-	-	-	nA
			2.4 V	305	875	2900	6400	12500	-	-	-	-	-	
			3 V	305	865	2950	6150	12500	-	-	-	-	-	
			3.6 V	310	870	3000	6450	13000	-	-	-	-	-	

Table 35. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is HSI16 = 16 MHz[5]	3 V	2.46	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: II_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 39: Low-power mode wakeup timings*.

Table 36. Current consumption in Shutdown mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown)	Supply current in Shutdown mode (backup registers retained) RTC disabled	-	1.8 V	19	140	885	2500	6600	160	390	2100	6700	21000	nA
			2.4 V	28	180	1050	2950	7800	190	510	2400	7900	24000	
			3 V	43	230	1300	3600	9300	220	580	2900	9100	27000	
			3.6 V	87	360	1750	4700	12000	300	750	3500	11000	32000	

Table 36. Current consumption in Shutdown mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[(1)]					Unit
		-	V_{DD}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Shutdown with RTC)	Supply current in Shutdown mode (backup registers retained) RTC enabled	RTC clocked by LSE bypassed at 32768 Hz	1.8 V	330	445	1150	2700	6800	-	-	-	-	-	nA
			2.4 V	460	605	1450	3350	8150	-	-	-	-	-	
			3 V	745	1000	2200	4550	10500	-	-	-	-	-	
			3.6 V	2100	2850	4900	8150	15500	-	-	-	-	-	
		RTC clocked by LSE quartz[(2)] in low drive mode	1.8 V	285	450	1050	2500	-	-	-	-	-	-	
			2.4 V	410	585	1300	3050	-	-	-	-	-	-	
			3 V	565	770	1750	3750	-	-	-	-	-	-	
			3.6 V	780	1200	2400	4850	-	-	-	-	-	-	
IDD(wakeup from Shutdown)	Supply current during wakeup from Shutdown mode	Wakeup clock is HSI16 = 16 MHz[(3)]	3 V	1.6	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
3. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 39: Low-power mode wakeup timings*.

Table 37. Current consumption in V_{BAT} mode

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(V_{BAT})	Backup domain supply current	RTC disabled	1.8 V	4	17	92	245	600	-	-	-	-	-	nA
			2.4 V	5	20	105	280	690	-	-	-	-	-	
			3 V	6	24	125	330	805	-	-	-	-	-	
			3.6 V	16	54	260	675	1650	-	-	-	-	-	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	310	315	350	470	-	-	-	-	-	-	
			2.4 V	435	440	500	665	-	-	-	-	-	-	
			3 V	720	815	1050	1350	-	-	-	-	-	-	
			3.6 V	2150	2600	3400	4050	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz[2]	1.8 V	270	345	455	715	835	-	-	-	-	-	
			2.4 V	385	455	650	910	910	-	-	-	-	-	
			3 V	525	600	910	1150	1000	-	-	-	-	-	
			3.6 V	710	995	1250	1700	1900	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

IO system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 57: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC, OPAMP, COMP input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This is done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 39: Low-power mode wakeup timings*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
V_{DD} is the I/O supply voltage
f_{SW} is the I/O switching frequency
C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 38*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 14: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 38*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 38. Peripheral current consumption

Bus	Peripheral	Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
-	Bus Matrix	6.12	5.69	4.70	6.11	µA/MHz
	AHB1 to APB1 bridge	0.26	0.25	0.22	0.03	
	AHB1 to APB2 bridge	0.39	0.37	0.32	0.03	
	FSMC	10.21	9.52	7.87	10.28	
	QUADSPI	3.51	3.27	2.69	3.51	
AHB1	CORDIC	1.28	1.19	0.98	0.78	µA/MHz
	CRC	0.74	0.68	0.57	0.63	
	DMA 1	2.83	2.64	2.17	2.75	
	DMA 2	3.11	2.90	2.39	2.43	
	DMAMUX	6.71	6.26	5.17	6.68	
	SRAM1	0.58	0.54	0.44	0.54	
	FLASH	6.46	6.01	4.95	6.15	
	FMAC	4.59	4.29	3.57	3.83	

Table 38. Peripheral current consumption (continued)

Bus	Peripheral	Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
AHB2	ADC1/ADC2	6.24	5.80	4.77	5.88	µA/MHz
	ADC3/ADC4/ADC5	8.21	7.64	6.29	8.14	
	DAC1	4.70	4.38	3.63	4.40	
	DAC2	2.51	2.34	1.93	2.14	
	DAC3	4.62	4.31	3.57	4.15	
	DAC4	4.31	4.01	3.32	3.90	
	GPIOA	0.09	0.08	0.07	0.14	
	GPIOB	0.10	0.09	0.07	0.03	
	GPIOC	0.10	0.09	0.08	0.03	
	GPIOD	0.06	0.06	0.03	0.05	
	GPIOE	0.23	0.22	0.18	0.10	
	GPIOF	0.07	0.07	0.05	0.02	
	GPIOG	0.25	0.24	0.20	0.24	
	SRAM2	0.39	0.37	0.29	0.28	
	CCM SRAM	0.29	0.27	0.23	0.22	
	RNG	2.09	1.95	NA	NA	

Table 38. Peripheral current consumption (continued)

Bus	Peripheral	Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
AHB2	ADC1/ADC2	6.24	5.80	4.77	5.88	µA/MHz
	ADC3/ADC4/ADC5	8.21	7.64	6.29	8.14	
	DAC1	4.70	4.38	3.63	4.40	
	DAC2	2.51	2.34	1.93	2.14	
	DAC3	4.62	4.31	3.57	4.15	
	DAC4	4.31	4.01	3.32	3.90	
	GPIOA	0.09	0.08	0.07	0.14	
	GPIOB	0.10	0.09	0.07	0.03	
	GPIOC	0.10	0.09	0.08	0.03	
	GPIOD	0.06	0.06	0.03	0.05	
	GPIOE	0.23	0.22	0.18	0.10	
	GPIOF	0.07	0.07	0.05	0.02	
	GPIOG	0.25	0.24	0.20	0.24	
	SRAM2	0.39	0.37	0.29	0.28	
	CCM SRAM	0.29	0.27	0.23	0.22	
	RNG	2.09	1.95	NA	NA	
	AES	2.84	2.64	2.19	2.43	

Table 38. Peripheral current consumption (continued)

Bus	Peripheral	Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
APB1	CRS	0.74	0.68	0.57	0.51	µA/MHz
	FDCAN1/FDCAN2/FDCAN3	22.20	20.68	17.10	21.15	
	I2C1	1.29	1.20	0.99	1.28	
	I2C2	1.29	1.20	0.99	1.28	
	I2C3	1.25	1.17	0.96	1.56	
	I2C4	1.25	1.16	0.96	1.97	
	LPTIM1	1.11	1.03	0.85	1.42	
	LPUART1	1.91	1.78	1.47	2.03	
	PWR	0.71	0.65	0.53	0.53	
	RTC	2.64	2.46	2.07	3.26	
	SPI2/I2S2	4.05	3.77	3.11	4.16	
	SPI3/I2S3	4.08	3.81	3.13	4.49	
	TIM2	7.97	7.42	6.16	8.29	
	TIM3	6.37	5.93	4.92	6.81	
	TIM4	6.43	5.98	4.97	6.50	
	TIM5	8.28	7.71	6.38	8.11	
	TIM6	1.22	1.13	0.94	1.45	
	TIM7	1.28	1.18	0.98	1.56	
	UART4	2.51	2.33	1.92	3.14	
	UART5	2.79	2.60	2.14	3.34	
	USART2	2.75	2.56	2.12	3.11	
	USART3	2.71	2.52	2.08	2.47	
	USB	0.46	0.43	NA	NA	
	UCPD	2.46	2.28	1.89	NA	
	WWDG	0.42	0.39	0.31	0.42	

Table 38. Peripheral current consumption (continued)

Bus	Peripheral	Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
APB2	HRTIM	69.98	65.11	53.68	60.95	µA/MHz
	SAI1	2.67	2.48	2.05	2.64	
	SPI1	1.99	1.86	1.54	2.02	
	SPI4	1.99	1.86	1.54	2.02	
	TIM1	10.85	10.13	8.40	9.93	
	TIM8	10.67	9.96	8.25	9.82	
	TIM15	4.81	4.48	3.71	4.57	
	TIM16	3.71	3.45	2.88	3.45	
	TIM17	3.66	3.41	2.83	3.81	
	TIM20	10.71	9.99	8.29	10.00	
	USART1	2.49	2.31	1.91	2.49	
	SYSCFG/COMP/OPAMP/VREFBUF	1.63	1.52	1.25	0.91	

Table 38. Peripheral current consumption (continued)

Bus	Peripheral		Range 1 Boost mode	Range 1 Normal mode	Range 2	Low-power run and sleep	Unit
Independent clock domain	ADC1/ ADC2	independent clock domain	0.72	0.67	0.53	0.63	µA/MHz
	ADC3/ ADC4/ ADC5	independent clock domain	0.67	0.62	0.50	0.22	
	FDCAN1/ FDCAN2/ FDCAN3	independent clock domain	11.62	10.84	8.95	10.24	
	I2C1	independent clock domain	4.03	3.76	3.12	4.15	
	I2C2	independent clock domain	3.78	3.52	2.93	3.23	
	I2C3	independent clock domain	2.72	2.55	2.11	2.65	
	I2C4	independent clock domain	3.95	3.67	3.04	2.81	
	I2S2	independent clock domain	1.49	1.40	1.15	1.63	
	I2S3	independent clock domain	1.52	1.43	1.16	2.15	
	LPTIM1	independent clock domain	4.00	3.71	3.08	3.57	
	LPUART1	independent clock domain	4.43	4.13	3.45	4.02	
	QUADSPI	independent clock domain	0.54	0.51	0.44	0.75	
	RNG	independent clock domain	0.83	0.87	NA	NA	
	USB	independent clock domain	1.10	1.17	NA	NA	
	SAI1	independent clock domain	3.36	3.14	2.58	3.25	
	UART4	independent clock domain	6.60	6.17	5.14	6.02	
	UART5	independent clock domain	6.60	6.16	5.12	6.12	
	USART1	independent clock domain	7.62	7.12	5.89	6.90	
	USART2	independent clock domain	7.37	6.86	5.70	6.72	
	USART3	independent clock domain	7.98	7.44	6.17	8.21	
All	-		369.00	316.04	266.18	325.00	µA/MHz

5.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 39* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Table 39. Low-power mode wakeup timings[1]

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep mode to Run mode	-		11	12	Nb of CPU cycles
$t_{WULPSLEEP}$	Wakeup time from Low-power sleep mode to Low-power run mode	-		10	11	
$t_{WUSTOP0}$	Wake up time from Stop 0 mode to Run mode in Flash	Range 1	Wakeup clock HSI16 = 16 MHz	5.8	6	µs
		Range 2	Wakeup clock HSI16 = 16 MHz	18.4	19.1	
	Wake up time from Stop 0 mode to Run mode in SRAM1	Range 1	Wakeup clock HSI16 = 16 MHz	2.8	3	
		Range 2	Wakeup clock HSI16 = 16 MHz	2.9	3	
$t_{WUSTOP1}$	Wake up time from Stop 1 mode to Run in Flash	Range 1	Wakeup clock HSI16 = 16 MHz	9.5	9.8	
		Range 2	Wakeup clock HSI16 = 16 MHz	21.9	22.7	
	Wake up time from Stop 1 mode to Run mode in SRAM1	Range 1	Wakeup clock HSI16 = 16 MHz	6.6	6.9	
		Range 2	Wakeup clock HSI16 = 16 MHz	6.4	6.6	
	Wake up time from Stop 1 mode to Low-power run mode in Flash	Regulator in low-power mode (LPR=1 in PWR_CR1)	Wakeup clock HSI16 = 16 MHz, with HPRE = 8	26.1	27.1	
	Wake up time from Stop 1 mode to Low-power run mode in SRAM1			14.4	15	
t_{WUSTBY}	Wakeup time from Standby mode to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	29.7	33.8	
$t_{WUSTBY\ SRAM2}$	Wakeup time from Standby with SRAM2 to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	29.7	33.5	
t_{WUSHDN}	Wakeup time from Shutdown mode to Run mode	Range 1	Wakeup clock HSI16 = 16 MHz	267.9	274.6	
$t_{WULPRUN}$	Wakeup time from Low-power run mode to Run mode[2]	Wakeup clock HSI16 = 16 MHz with HPRE = 8		5	7	

1. Guaranteed by characterization results.
2. Time until REGLPF flag is cleared in PWR_SR2.

Table 40. Regulator modes transition times[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{VOST}	Regulator transition time from Range 2 to Range 1 or Range 1 to Range 2[2]	Wakeup clock HSI16 = 16 MHz with HPRE = 8	20	40	µs

1. Guaranteed by characterization results.
2. Time until VOSF flag is cleared in PWR_SR2.

Table 41. Wakeup time using USART/LPUART[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wakeup up from stop mode when USART/LPUART clock source is HSI16	Stop 0 mode	-	1.7	µs
		Stop 1 mode	-	8.5	

1. Guaranteed by design.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

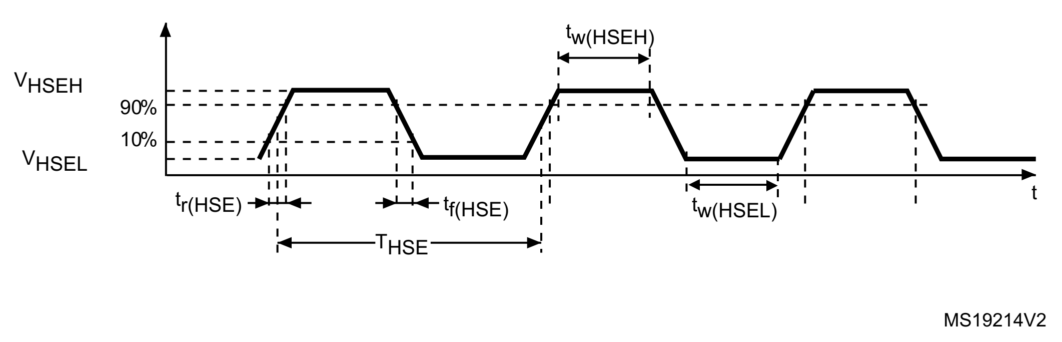
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. However, the recommended clock input waveform is shown in *Figure 18: High-speed external clock source AC timing diagram*.

Table 42. High-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 18. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

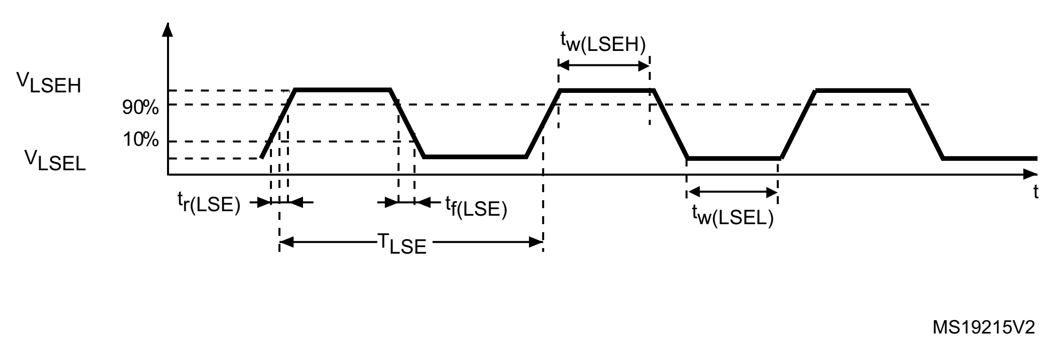
The external clock signal has to respect the I/O characteristics in *Section 5.3.14*. However, the recommended clock input waveform is shown in *Figure 19*.

Table 43. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. HSE oscillator characteristics(1)

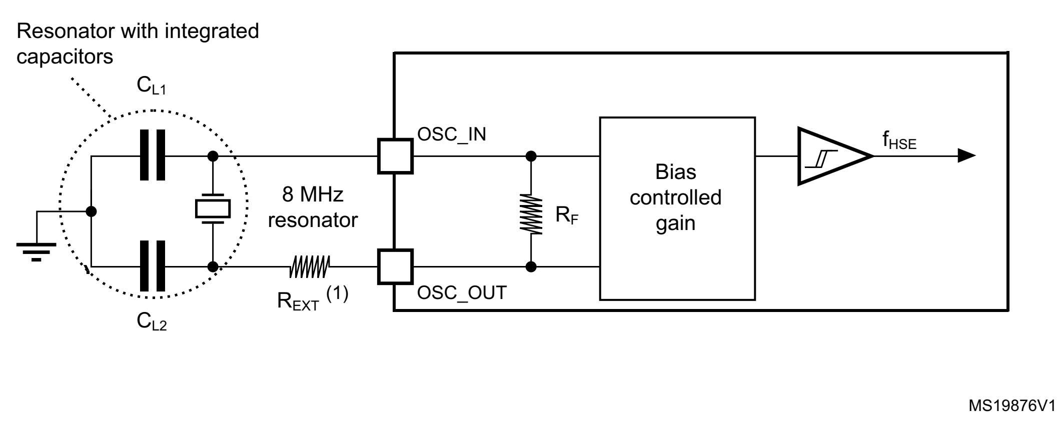
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 20*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

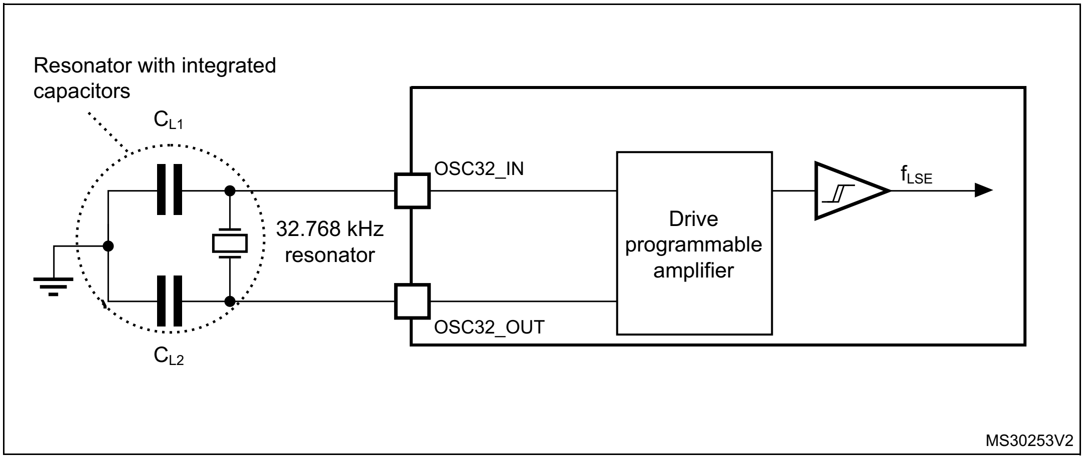
Table 45. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 46* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*. The provided curves are characterization results, not tested in production.

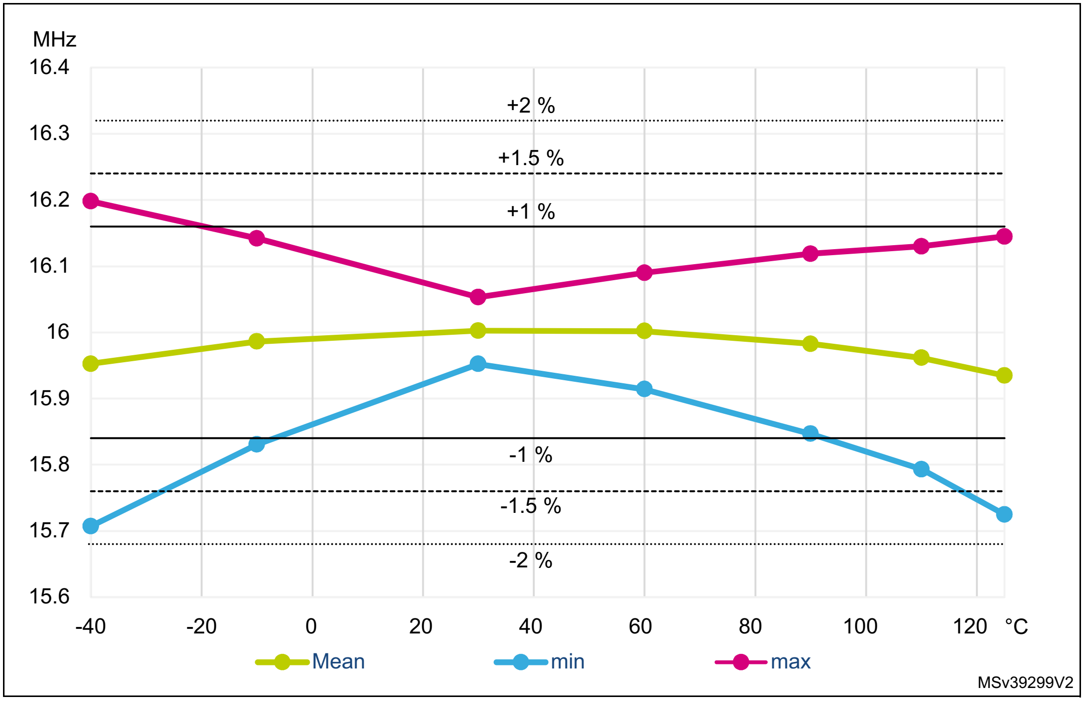
High-speed internal (HSI16) RC oscillator

Table 46. HSI16 oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)[2]	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)[2]	HSI16 oscillator start-up time	-	-	0.8	1.2	μs
t_{stab}(HSI16)[2]	HSI16 oscillator stabilization time	-	-	3	5	μs
I_{DD}(HSI16)[2]	HSI16 oscillator power consumption	-	-	155	190	μA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 22. HSI16 frequency versus temperature



High-speed internal 48 MHz (HSI48) RC oscillator

Table 47. HSI48 oscillator characteristics[(1)]

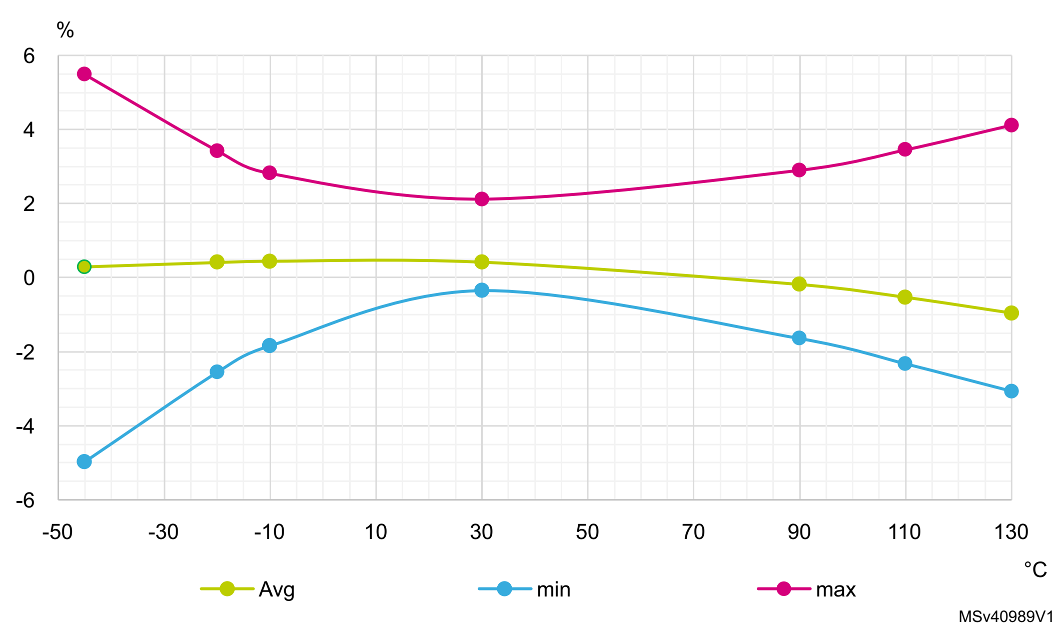
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

Table 47. HSI48 oscillator characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles[4]	-	-	+/-0.15[2]	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles[4]	-	-	+/-0.25[2]	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 23. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 48. LSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, T_A = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$[2]	LSI oscillator start-up time	-	-	80	130	µs

Table 48. LSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{STAB}(LSI)(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
I_{DD}(LSI)(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

5.3.9 PLL characteristics

The parameters given in *Table 49* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 49. PLL characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	-	2.66	-	16	MHz
	PLL input clock duty cycle	-	45	-	55	%
$f_{PLL\_P\_OUT}$	PLL multiplier output clock P	Voltage scaling Range 1 Boost mode	2.0645	-	170	MHz
		Voltage scaling Range 1	2.0645	-	150	
		Voltage scaling Range 2	2.0645	-	26	
$f_{PLL\_Q\_OUT}$	PLL multiplier output clock Q	Voltage scaling Range 1 Boost mode	8	-	170	
		Voltage scaling Range 1	8	-	150	
		Voltage scaling Range 2	8	-	26	
$f_{PLL\_R\_OUT}$	PLL multiplier output clock R	Voltage scaling Range 1 Boost mode	8	-	170	
		Voltage scaling Range 1	8	-	150	
		Voltage scaling Range 2	8	-	26	
f_{VCO_OUT}	PLL VCO output	Voltage scaling Range 1	96	-	344	
		Voltage scaling Range 2	96	-	128	
t_{LOCK}	PLL lock time	-	-	15	40	µs
Jitter	RMS cycle-to-cycle jitter	System clock 150 MHz	-	28.6	-	±ps
	RMS period jitter		-	21.4	-	
I_{DD}(PLL)	PLL power consumption on V_{DD}(1)	VCO freq = 96 MHz	-	200	260	µA
		VCO freq = 192 MHz	-	300	380	
		VCO freq = 344 MHz	-	520	650	

1. Guaranteed by design.
2. Take care of using the appropriate division factor M to obtain the specified PLL input clock values.

5.3.10 Flash memory characteristics

Table 50. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.7	83.35	µs
t_{prog_row}	One row (32 double word) programming time	Normal programming	2.61	2.7	ms
		Fast programming	1.91	1.95	
t_{prog_page}	One page (2 Kbytes) programming time	Normal programming	20.91	21.34	
		Fast programming	15.29	15.6	
t_{ERASE}	Page (2 Kbytes) erase time	-	22.02	24.47	
t_{prog_bank}	One bank (256 Kbyte) programming time	Normal programming	2.68	2.73	s
		Fast programming	1.96	2	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.6	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.5	-	mA
		Erase mode	3.5	-	
	Maximum current (peak)	Write mode	7 (for 6 µs)	-	
		Erase mode	7 (for 67 µs)	-	

1. Guaranteed by design.

Table 51. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

5.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 52*. They are based on the EMS levels and classes defined in application note AN1709.

Table 52. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 170 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 170 MHz, conforming to IEC 61000-4-4	5A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 53. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8 MHz / 170 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP128 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	4	dBµV
			30 MHz to 130 MHz	0	
			130 MHz to 1 GHz	16	
			1 GHz to 2 GHz	11	
			EMI Level	3.5	-

5.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 54. ESD absolute maximum ratings

Symbol	Ratings	Conditions		Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	LQFP100 and LQFP128	C1	250	V
			LQFP80	TBD	TBD	
			Other packages	C2a	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on three parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78E IC latch-up standard.

Table 55. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	TA = +125 °C conforming to JESD78E	Class II level A

5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 56*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 56. I/O current injection susceptibility

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(1)	Injected current on pin	All except TT_a, PF10, PB8-BOOT0, PC10	-5	NA	mA
		PF10, PB8-BOOT0, PC10	-0	NA	
		TT_a pins	-5	0	

1. Guaranteed by characterization.

5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the conditions summarized in *Table 17: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 57. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)(2)	I/O input low level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	--	--	0.3xV_{DD}	V
						0.39xV_{DD}-0.06(3)	
		FT_c	2 V<V_{DD}<2.7 V	-	-	0.3xV_{DD}	
			1.62 V<V_{DD}<2.7 V	-	-	0.2.5xV_{DD}	
V_{IH}(1)(2)	I/O input high level voltage	All except FT_c	1.62 V<V_{DD}<3.6 V	0.7xV_{DD}	-	-	V
				0.49xV_{DD} +0.26(3)	-	-	
		FT_c	1.62 V<V_{DD}<3.6 V	0.7xV_{DD}	-	-	
V_{HYS}(3)	Input hysteresis	TT_xx, FT_xxx, NRST	1.62 V<V_{DD}<3.6 V	-	200	-	mV
I_{leak}	Input leakage current(3)	FT_xx except FT_c	$0 < V_{IN} \leq V_{DD}$	-	-	±100	nA
			$V_{DD} \leq V_{IN} \leq V_{DD}$+1 V	-	-	650(4)	
			V_{DD}+1 V < $V_{IN} \leq$ 5.5 V	-	-	200(4)	
		FT_c	$0 \leq V_{IN} \leq V_{DDMAX}$	-	-	2000	
			$V_{DD} \leq V_{IN}$ <0.5 V	-	-	3000	
		FT_u, PC3	$0 \leq V_{IN} \leq V_{DD}$	-	-	±150	
			$V_{DD} \leq V_{IN} \leq V_{DD}$+ 1 V	-	-	±2500	
			$V_{DD} \leq V_{IN} \leq$ 5.5 V	-	-	±250	
		FT_d	$0 \leq V_{IN} \leq V_{DD}$	-	-	±4500	
			V_{DD} + 1V $\leq V_{IN} \leq$ 5.5 V	-	-	±9000	
		TT_xx	$0 \leq V_{IN} \leq V_{DD}$	-	-	±150	
			$V_{DD} \leq V_{IN} \leq$ 3.6 V	-	-	2000	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$		25	40	55	
C_{IO}	I/O pin capacitance	I/O pin capacitance	-	-	5	-	pF

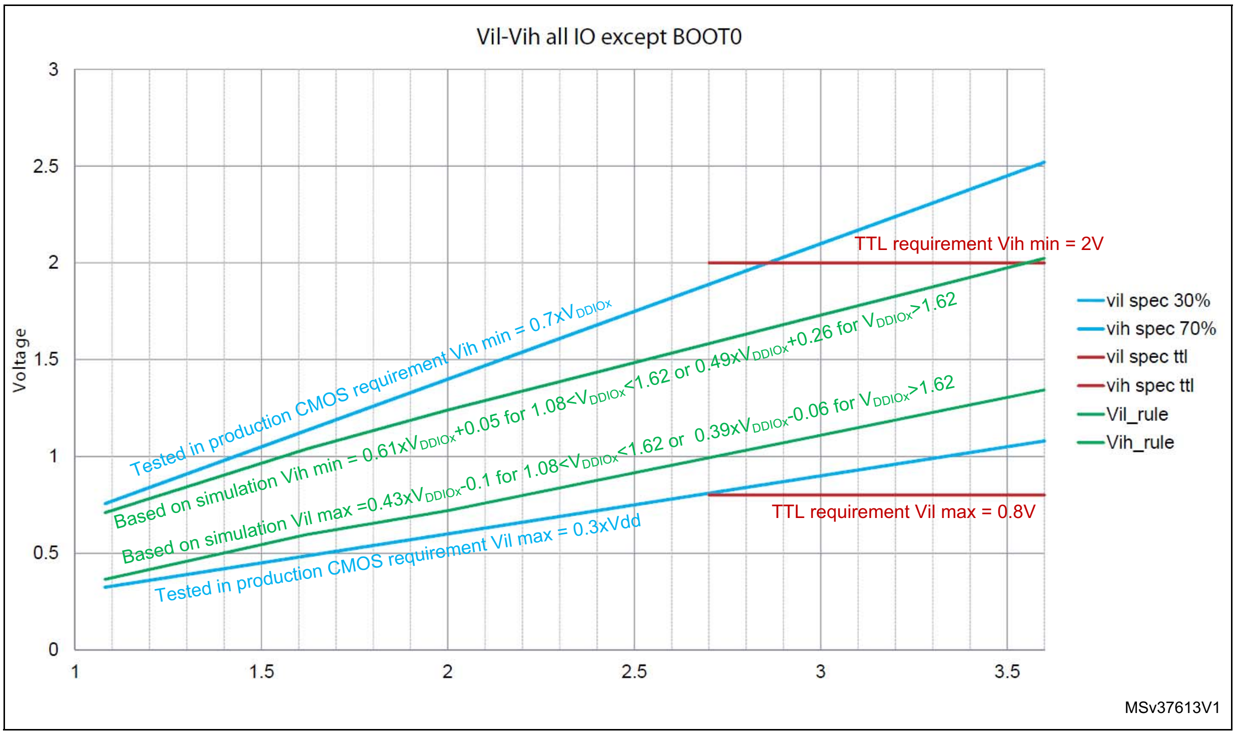
---

1. Refer to *Figure 24: I/O input characteristics*

2. Data based on characterization results, not tested in production
3. Guaranteed by design.
4. This value represents the pad leakage of the I/O itself. The total product pad leakage is provided by this formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of I/Os where VIN is applied on the pad] x I_{lkg}(Max).
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 24* for standard I/Os, and in *Figure 24* for 5 V tolerant I/Os.

Figure 24. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 58. Output voltage characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(3)	Output low level voltage for an I/O pin	CMOS port $\lvert I_{IO}\rvert$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port $\lvert I_{IO}\rvert$ = 2 mA for FT_c I/Os = 8 mA for other I/Os V_{DD} ≥ 2.7 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	All I/Os except FT_c $\lvert I_{IO}\rvert$ = 20 mA V_{DD} ≥ 2.7 V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 1 mA for FT_c I/Os = 4 mA for other I/Os V_{DD} ≥ 1.62 V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with “f” option)	$\lvert I_{IO}\rvert$ = 20 mA V_{DD} ≥ 2.7 V	-	0.4	
		$\lvert I_{IO}\rvert$ = 10 mA V_{DD} ≥ 1.62 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 14: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 25* and *Table 59*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 59. I/O (except FT_c) AC characteristics(1) (2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	1	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	1.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	52	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	37	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	15	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	16	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	9	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	25	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	37.5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DD}≤2.7 V	-	11	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	5	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	50	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	75	
	Tr/Tf	Output rise and fall time(4)	C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DD}≤2.7 V	-	6	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	1.7	
			C=10 pF, 1.62 V≤V_{DD}≤2.7 V	-	3.3	

Table 59. I/O (except FT_c) AC characteristics[1] [2] (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
FM+	Fmax[5]	Maximum frequency	C=50 pF, 1.6 V≤V_{DD}≤3.6 V	-	1	MHz
	Tr/TF[4]	Output high to low level fall time		-	5	ns

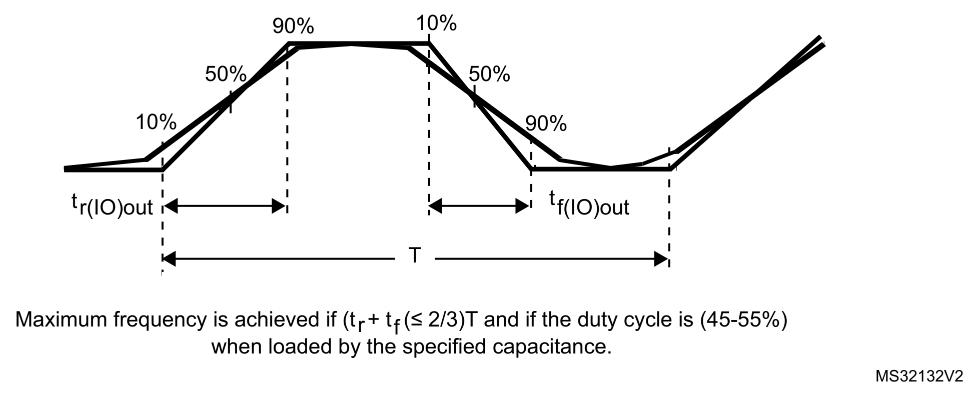
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs" for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represented the I/O capability but maximum system frequency is 170 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I2C specification.
5. The maximum frequency is defined with the following conditions:
   - (Tr+ Tf) ≤ 2/3 T.
   - 45%<Duty cycle<55%

Table 60. I/O FT_c AC characteristics[1] [2]

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	2	MHz
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	1	
	Tr/Tf	Output H/L to L/H level fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	170	ns
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	330	
1	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	10	MHz
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	5	
	Tr/Tf	Output H/L to L/H level fall time	C=50 pF, 2.7 V≤V_{DD}≤3.6 V	-	35	ns
			C=50 pF, 1.6 V≤V_{DD}≤2.7 V	-	65	

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs" for a description of GPIO Port configuration register.
2. Guaranteed by design.

Figure 25. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

1. Refer to *Table 59: I/O (except FT_c) AC characteristics*.

5.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

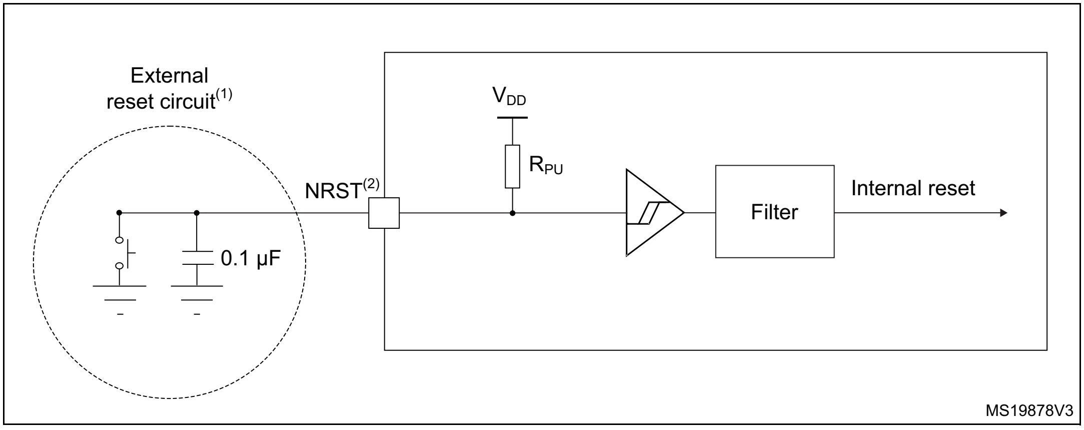
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 61. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3xV_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7xV_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 26. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61: NRST pin characteristics*. Otherwise the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.16 High-resolution timer (HRTIM)

The parameters given in *Table 62* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 62. HRTIM characteristics[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Timer ambient temperature range	f_{HRTIM}=170 MHz	-40	-	125	°C
f_{HRTIM}	HRTIM input clock for DLL calibration	As per T_A conditions	-	-	170	MHz
t_{HRTIM}			5.88	-	-	ns
$t_{RES(HRTIM)}$	high-resolution step size	f_{HRTIM}=170 MHz, T_A from -40 to 105°C	-	184	-	ps
Res_{HRTIM}	Timer resolution	-	-	-	16	bit
t_{DTG}	Dead time generator clock period	-	0.125	-	16	t_{HRTIM}
		f_{HRTIM}=170 MHz	0.735	-	94.1	ns
$\lvert t_{DTR}\rvert / \lvert t_{DTF}\rvert$ max	Dead time range (absolute value)	-	-	-	511	t_{DTG}
		f_{HRTIM}=170 MHz	-	-	48.09	µs
f_{CHPFRQ}	Chopper stage clock frequency	-	1/256	-	1/16	f_{HRTIM}
		f_{HRTIM}=170 MHz	0.664	-	10.625	MHz
t_{1STPW}	Chopper first pulse length	-	16	-	256	t_{HRTIM}
		f_{HRTIM}=170 MHz	0.094	-	1.506	µs

1. Data based on characterization results, not tested in production.

Table 63. HRTIM output response to fault protection[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.[2]	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIM1_FLTx digital input to HRTIM_CHxy output pin	-	9	20	ns
$t_{W(FLT)}$	Minimum Fault pulse width	-	7	-	-	
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin	-	16	31	

1. Refer to Fault paragraph in HRTIM section of RM0440.
2. Data based on characterization results, not tested in production.

Table 64. HRTIM output response to external events 1 to 5 (Low-Latency mode[1])

Symbol	Parameter	Conditions	Min	Typ[2]	Max[2]	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load)	-	12	23	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator COMPx_INP input pin to HRTIM_CHxy output pin (30pF load)	-	19	31	

1. EExFAST bit in HRTIM_EECR1 register is set (Low Latency mode). This functionality is available on external events channels 1 to 5. Refer to Latency to external events paragraph in HRTIM section of RM0440.
2. Data based on characterization results, not tested in production.

Table 65. HRTIM output response to external events 1 to 10 (Synchronous mode (1))

Symbol	Parameter	Conditions	Min.	Typ.	Max.(2)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM1_EEVx digital input to HRTIM_CHxy output pin (30pF load) (3)	-	56	66	ns
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load) (3)	-	62	76	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	ns
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM1_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM} (4)

1. EExFAST bit in HRTIM_EECR1 or HRTIM_EECR2 register is cleared (synchronous mode). External event filtering is disabled, i.e. EExF[3:0]=0000 in HRTIM_EECR2 register. Refer to Latency to external events paragraph in HRTIM section of RM0440.
2. Data based on characterization results, not tested in production.
3. This parameter is given for f_{HRTIM} = 170 MHz.
4. T_{HRTIM} = 1 / f_{HRTIM} with f_{HRTIM}= 170 MHz.

Table 66. HRTIM synchronization input / output(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM_SCIN	-	2	-	-	t_{HRTIM}
$t_{RES(ESR)}$	Response time to external synchronization request	-	-	-	3	t_{HRTIM}
$t_{W(SYNCOUT)}$	Pulse width on HRTIM_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM}=170 MHz	-	94.1	-	ns

1. Guaranteed by design, not tested in production.

5.3.17 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 67. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

5.3.18 Analog switches booster

Table 68. Analog switches booster characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for $1.62\ V \leq V_{DD} \leq 2.0\ V$	-	-	250	µA
	Booster consumption for $2.0\ V \leq V_{DD} \leq 2.7\ V$	-	-	500	
	Booster consumption for $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	-	900	

1. Guaranteed by design.

5.3.19 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 69* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 17: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 69. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
V_{CMIN}	Input common mode	Differential	$(V_{REF+}+V_{REF-})/2 - 0.18$	$(V_{REF+} + V_{REF-})/2$	$(V_{REF+} + V_{REF-})/2 + 0.18$	V
f_{ADC}	ADC clock frequency	Range 1, single ADC operation	0.14	-	60	MHz
		Range 2	-	-	26	
		Range 1, all ADCs operation, single ended mode $V_{DDA} \geq 2.7$ V	0.14	-	52	
		Range 1, all ADCs operation, single ended mode $V_{DDA} \geq 1.62$ V	0.14	-	42	
		Range 1, all ADCs operation, differential mode $V_{DDA} \geq 1.62$ V	0.14	-	56	
f_s	Sampling rate, continuous mode	For given resolution and sampling time cycles (t_s)	0.001	f_{ADC} / (sampling time [cycles] + resolution [bits] + 0.5)		Msps
T_{TRIG}	External trigger period	Considering trigger conversion latency time (t_{LATR} or $t_{LATRINJ}$)	-	-	1ms	-
		Resolution = 12 bits, $f_{ADC=60\ MHz}$	tconv + [t_{LATR} or $t_{LATRINJ}$]	-		
V_{AIN} (3)	Conversion voltage range	-	0	-	V_{REF+}	V

Table 69. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{AIN}(4)	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 60 MHz	1.93			µs
		-	116			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2.0	
		CKMODE = 10	-	-	2.25	
		CKMODE = 11	-	-	2.125	
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 60 MHz	0.0416	-	10.675	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 60 MHz Resolution = 12 bits	0.25	-	10.883	µs
		-	t_s[cycles] + resolution [bits] +0.5 = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 4 Msps	-	590	730	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 4 Msps	-	110	140	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 4 Msps	-	220	270	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design

2. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disabled when $V_{DDA} \geq 2.4$ V.
3. V_{REF+} can be internally connected to V_{DDA}, depending on the package.
   Refer to *Section 4: Pinouts and pin description* for further details.
4. The maximum value of RAIN can be found in *Table 70: Maximum ADC RAIN*.

The maximum value of R_{AIN} can be found in *Table 70: Maximum ADC RAIN*.

Table 70. Maximum ADC R_{AIN} (1)(2)

Resolution	Sampling cycle @60 MHz	Sampling time [ns]	R_{AIN} max (Ω)	
			Fast channels(3)	Slow channels(4)
12 bits	2.5	41.67	100	N/A
	6.5	108.33	330	100
	12.5	208.33	680	470
	24.5	408.33	1500	1200
	47.5	791.67	2200	1800
	92.5	1541.67	4700	3900
	247.5	4125	12000	10000
	640.5	10675	39000	33000
10 bits	2.5	41.67	120	N/A
	6.5	108.33	390	180
	12.5	208.33	820	560
	24.5	408.33	1500	1200
	47.5	791.67	2200	1800
	92.5	1541.67	5600	4700
	247.5	4125	12000	10000
	640.5	10675	47000	39000
8 bits	2.5	41.67	180	N/A
	6.5	108.33	470	270
	12.5	208.33	1000	680
	24.5	408.33	1800	1500
	47.5	791.67	2700	2200
	92.5	1541.67	6800	5600
	247.5	4125	15000	12000
	640.5	10675	50000	50000
6 bits	2.5	41.67	220	N/A
	6.5	108.33	560	330
	12.5	208.33	1200	1000
	24.5	408.33	2700	2200
	47.5	791.67	3900	3300
	92.5	1541.67	8200	6800
	247.5	4125	18000	15000
	640.5	10675	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enabled when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$V). It is disabled when $V_{DDA} \geq 2.4$ V.
3. Fast channels are: ADCx_IN1 to ADCx_IN5.
4. Slow channels are: all ADC inputs except the fast channels.

Table 71. ADC accuracy - limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ADC operation ADC clock frequency ≤ 60 MHz, V_{DDA} = VREF+ = 3 V, TA = 25 °C Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	5.9	6.9	LSB
				Slow channel (max speed)	-	5.5	6.9	
			Differential	Fast channel (max speed)	-	4.6	5.6	
				Slow channel (max speed)	-	4	5.6	
EO	Offset error		Single ended	Fast channel (max speed)	-	2.5	4	
				Slow channel (max speed)	-	1.9	4	
			Differential	Fast channel (max speed)	-	1.8	2.8	
				Slow channel (max speed)	-	1.1	2.8	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.6	6.6	
				Slow channel (max speed)	-	4.5	6.6	
			Differential	Fast channel (max speed)	-	3.6	4.6	
				Slow channel (max speed)	-	3.3	4.6	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.1	1.9	
				Slow channel (max speed)	-	1.3	1.9	
			Differential	Fast channel (max speed)	-	1.3	1.6	
				Slow channel (max speed)	-	1.4	1.6	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.3	3.4	
				Slow channel (max speed)	-	2.4	3.4	
			Differential	Fast channel (max speed)	-	2.1	3.2	
				Slow channel (max speed)	-	2.2	3.2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.6	-	bits
				Slow channel (max speed)	10.4	10.6	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65.6	-	dB
				Slow channel (max speed)	64.4	65.6	-	
			Differential	Fast channel (max speed)	66.8	67.5	-	
				Slow channel (max speed)	66.8	67.5	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66.9	-	
				Slow channel (max speed)	65	66.9	-	
			Differential	Fast channel (max speed)	67	69	-	
				Slow channel (max speed)	67	69	-	

Table 71. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	Single ADC operation ADC clock frequency ≤ 60 MHz, V_{DDA} = VREF+ = 3 V, TA = 25 °C Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	-73	-72	dB
				Slow channel (max speed)	-	-73	-72	
			Differential	Fast channel (max speed)	-	-73	-72	
				Slow channel (max speed)	-	-73	-72	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

Table 72. ADC accuracy - limited test conditions 2[1][2][3]

Sym-bol	Parameter	Conditions[4]			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ADC operation ADC clock frequency ≤ 60 MHz, 2 V ≤ V_{DDA} Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	5.9	8.4	LSB
				Slow channel (max speed)	-	5.5	8	
			Differential	Fast channel (max speed)	-	4.6	6.6	
				Slow channel (max speed)	-	4	6	
EO	Offset error		Single ended	Fast channel (max speed)	-	2.5	6	
				Slow channel (max speed)	-	1.9	6.9	
			Differential	Fast channel (max speed)	-	1.8	3.3	
				Slow channel (max speed)	-	1.1	3.3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.6	8.1	
				Slow channel (max speed)	-	4.5	8.1	
			Differential	Fast channel (max speed)	-	3.6	4.6	
				Slow channel (max speed)	-	3.3	4.6	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.1	1.8	
				Slow channel (max speed)	-	1.3	1.8	
			Differential	Fast channel (max speed)	-	1.3	1.6	
				Slow channel (max speed)	-	1.4	1.6	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.3	4.4	
				Slow channel (max speed)	-	2.4	4.4	
			Differential	Fast channel (max speed)	-	2.1	4.1	
				Slow channel (max speed)	-	2.2	3.7	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.6	-	bits
				Slow channel (max speed)	10	10.6	-	
			Differential	Fast channel (max speed)	10.7	10.9	-	
				Slow channel (max speed)	10.7	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65.6	-	dB
				Slow channel (max speed)	62	65.6	-	
			Differential	Fast channel (max speed)	65	67.5	-	
				Slow channel (max speed)	65	67.5	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	66.9	-	
				Slow channel (max speed)	64	66.9	-	
			Differential	Fast channel (max speed)	66.5	69	-	
				Slow channel (max speed)	66.5	69	-	

Table 72. ADC accuracy - limited test conditions 2(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	Single ADC operation ADC clock frequency ≤ 60 MHz, 2 V ≤ V_{DDA} Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	-73	-65	dB
				Slow channel (max speed)	-	-73	-67	
			Differential	Fast channel (max speed)	-	-73	-70	
				Slow channel (max speed)	-	-73	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disabled when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 73. ADC accuracy - limited test conditions 3[(1)(2)(3)]

Symbol	Parameter	Conditions[(4)]			Min	Typ	Max	Unit
ET	Total unadjusted error	Single ADC operation ADC clock frequency ≤ 60 MHz, 1.62 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	5.9	7.9	LSB
				Slow channel (max speed)	-	5.5	7.5	
			Differential	Fast channel (max speed)	-	4.6	7.6	
				Slow channel (max speed)	-	4	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2.5	5.5	
				Slow channel (max speed)	-	1.9	5.5	
			Differential	Fast channel (max speed)	-	1.8	3.5	
				Slow channel (max speed)	-	1.1	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.6	7.1	
				Slow channel (max speed)	-	4.5	7	
			Differential	Fast channel (max speed)	-	3.6	4.1	
				Slow channel (max speed)	-	3.3	4.8	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.1	1.9	
				Slow channel (max speed)	-	1.3	1.9	
			Differential	Fast channel (max speed)	-	1.3	1.6	
				Slow channel (max speed)	-	1.4	1.6	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.3	4.4	
				Slow channel (max speed)	-	2.4	4.4	
			Differential	Fast channel (max speed)	-	2.1	3.7	
				Slow channel (max speed)	-	2.2	3.7	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.6	-	bits
				Slow channel (max speed)	10	10.6	-	
			Differential	Fast channel (max speed)	10.6	10.9	-	
				Slow channel (max speed)	10.6	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	65.6	-	dB
				Slow channel (max speed)	62	65.6	-	
			Differential	Fast channel (max speed)	65	67.5	-	
				Slow channel (max speed)	65	67.5	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	66.9	-	
				Slow channel (max speed)	63	66.9	-	
			Differential	Fast channel (max speed)	66	69	-	
				Slow channel (max speed)	66	69	-	

Table 73. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	Single ADC operation ADC clock frequency ≤ 60 MHz, 1.62 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Continuous mode, sampling rate: Fast channels@4Msps Slow channels@2Msps	Single ended	Fast channel (max speed)	-	-73	-67	dB
				Slow channel (max speed)	-	-73	-67	
			Differential	Fast channel (max speed)	-	-73	-71	
				Slow channel (max speed)	-	-73	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

Table 74. ADC accuracy (Multiple ADCs operation) - limited test conditions 1(1)(2)(3)

Symbol	Parameter	Conditions(4)	-	Min	Typ	Max	Unit
ET	Total unadjusted error	Multiple ADC operation ADC clock frequency: single ended ≤ 52 MHz, differential ≤ 56 MHz, $V_{DDA} = V_{REF} = 3.3$ V, 25°C, Continuous mode, sampling time: Fast channels: 2.5 cycles Slow channels: 6.5 cycles LQFP100 package	Single ended	-	4.5	-	LSB
			Differential	-	4.1	-	
EO	Offset error		Single ended	-	1.3	-	
			Differential	-	0.4	-	
EG	Gain error		Single ended	-	3.9	-	
			Differential	-	3.4	-	
ED	Differential linearity error		Single ended	-	1.5	-	
			Differential	-	1.2	-	
EL	Integral linearity error		Single ended	-	1.7	-	
			Differential	-	2.1	-	
ENOB	Effective number of bits		Single ended	-	10.7	-	bits
			Differential	-	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	-	66.3	-	dB
			Differential	-	67.2	-	
SNR	Signal-to-noise ratio		Single ended	-	67.3	-	
			Differential	-	68.6	-	
THD	Total harmonic distortion		Single ended	-	-73.5	-	dB
			Differential	-	-73	-	

1. Data based on characterization result, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disabled when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 75. ADC accuracy (Multiple ADCs operation) - limited test conditions 2(1)(2)(3)

Symbol	Parameter	Conditions(4)	-	Min	Typ	Max	Unit
ET	Total unadjusted error	Multiple ADC operation ADC clock frequency: single ended ≤ 52 MHz, differential ≤ 56 MHz, V_{DDA} ≥ 2.7 V, V_{REF}≥ 1.62 V, -40 to 125°C, Continuous mode, sampling time: Fast channels: 2.5 cycles Slow channels: 6.5 cycles LQFP100 package	Single ended	-	7.1	-	LSB
			Differential	-	4.6	-	
EO	Offset error		Single ended	-	4.2	-	
			Differential	-	2.8	-	
EG	Gain error		Single ended	-	6.8	-	
			Differential	-	4.3	-	
ED	Differential linearity error		Single ended	-	1.5	-	
			Differential	-	1.7	-	
EL	Integral linearity error		Single ended	-	3.1	-	
			Differential	-	2.4	-	
ENOB	Effective number of bits		Single ended	-	10.2	-	bits
			Differential	-	10.6	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	-	62.9	-	dB
			Differential	-	65.3	-	
SNR	Signal-to-noise ratio		Single ended	-	63.6	-	
			Differential	-	66.3	-	
THD	Total harmonic distortion		Single ended	-	-70.9	-	dB
			Differential	-	-71.8	-	

1. Data based on characterization result, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

Table 76. ADC accuracy (Multiple ADCs operation) - limited test conditions 3(1)(2)(3)

Symbol	Parameter	Conditions(4)	-	Min	Typ	Max	Unit
ET	Total unadjusted error	Multiple ADC operation ADC clock frequency: single ended ≤ 42 MHz, differential ≤ 56 MHz, V_{DDA}= V_{REF}≥ 1.62 V, -40 to 125°C, Continuous mode, sampling time: Fast channels: 2.5 cycles Slow channels: 6.5 cycles LQFP100 package	Single ended	-	7.4	-	LSB
			Differential	-	4.6	-	
EO	Offset error		Single ended	-	4	-	
			Differential	-	2.8	-	
EG	Gain error		Single ended	-	7.2	-	
			Differential	-	4.3	-	
ED	Differential linearity error		Single ended	-	1.8	-	
			Differential	-	1.7	-	
EL	Integral linearity error		Single ended	-	3.1	-	
			Differential	-	2.4	-	
ENOB	Effective number of bits		Single ended	-	10.1	-	bits
			Differential	-	10.6	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	-	62.6	-	dB
			Differential	-	65.3	-	
SNR	Signal-to-noise ratio		Single ended	-	63.2	-	
			Differential	-	66.3	-	
THD	Total harmonic distortion		Single ended	-	-70.6	-	dB
			Differential	-	-71.8	-	

1. Data based on characterization result, not tested in production.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disabled when V_{DDA} ≥ 2.4 V. No oversampling.

Figure 27. ADC accuracy characteristics

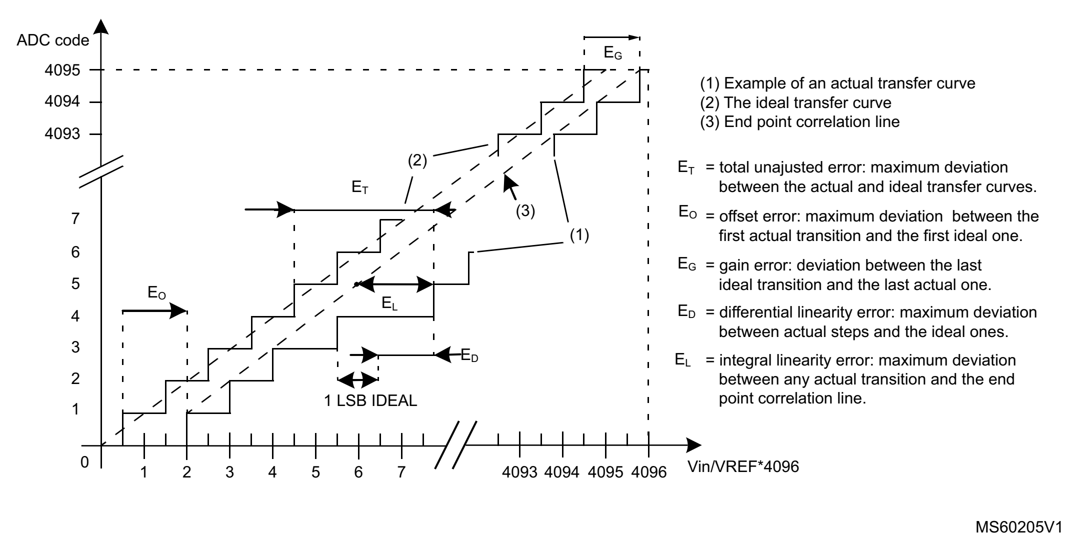
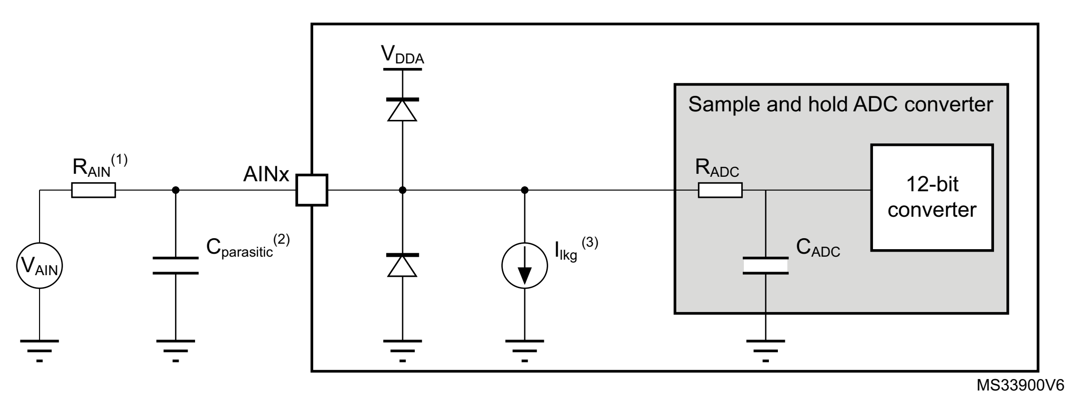


Figure 28. Typical connection diagram using the ADC



1. Refer to *Table 69: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 57: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 57: I/O static characteristics* for the values of I_{lkg}.

General PCB design guidelines

Power supply decoupling must be performed as shown in *Figure 15: Power supply scheme*. The decoupling capacitor on V_{DDA} must be ceramic (good quality) and it must be placed as close as possible to the chip.

5.3.20 Digital-to-Analog converter characteristics

Table 77. DAC 1MSPS characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	3.6	V
		Other modes		1.80	-		
V_{REF+}	Positive reference voltage	DAC output buffer OFF, DAC_OUT pin not connected (internal connection only)		1.71	-	V_{DDA}	
		Other modes		1.80	-		
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	$V_{REF+} - 0.2$	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

Table 77. DAC 1MSPS characteristics(1) (continued)

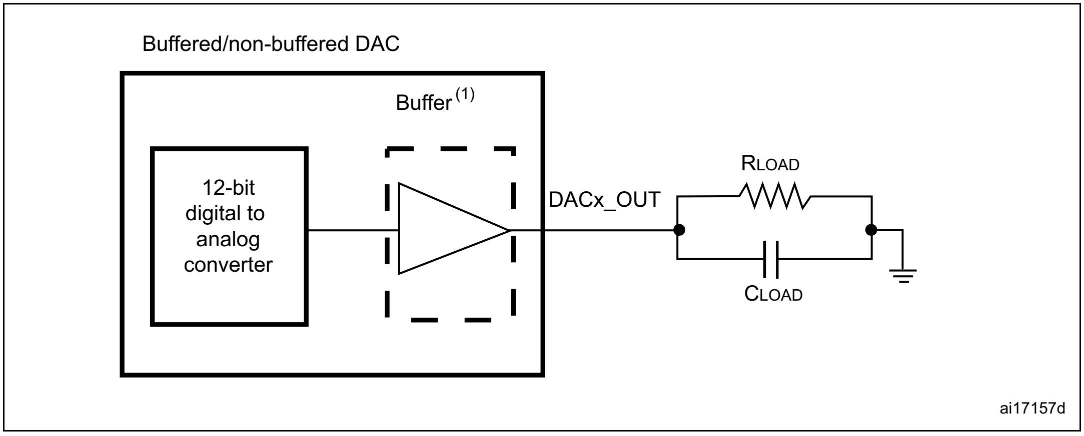
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{W\_to\_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)				-	-	µs
	DAC_MCR:MODEx[2:0] = 000 or 001	CL ≤ 50 pF, RL ≥ 5 kΩ		1			
	DAC_MCR:MODEx[2:0] = 010 or 011	CL ≤ 10 pF		1.4			
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	3.5	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	10.5	18	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	2	3.5	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-(3)	nA
CI_{int}	Internal sample and hold capacitor	-		5.2	7	8.8	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	V_{REF+} = 3.6 V		-	1500	-	µV
		V_{REF+} = 1.8 V		-	750	-	
$I_{DDA}(DAC)$	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	315	500	µA
			No load, worst code (0xF1C)	-	450	670	
		DAC output buffer OFF	No load, middle code (0x800)	-	-	0.2	
		Sample and hold mode, C_{SH} = 100 nF		-	315 x Ton/(Ton +Toff) (4)	670 x Ton/(Ton +Toff) (4)	

Table 77. DAC 1MSPS characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 57: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs" for more details.

Figure 29. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 78. DAC 1MSPS accuracy[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity [2]	DAC output buffer ON		-	-	±2	LSB
		DAC output buffer OFF		-	-	±2	
-	monotonicity	10 bits		Guaranteed			
INL	Integral non linearity[3]	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±4	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±4	
Offset	Offset error at code 0x800[3]	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±12	
			V_{REF+} = 1.8 V	-	-	±25	
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±8	
Offset1	Offset error at code 0x001[4]	DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±5	
OffsetCal	Offset Error at code 0x800 after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	V_{REF+} = 3.6 V	-	-	±5	
			V_{REF+} = 1.8 V	-	-	±7	
Gain	Gain error[5]	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±0.5	%
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±0.5	
TUE	Total unadjusted error	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±30	LSB
		DAC output buffer OFF CL ≤ 50 pF, no RL		-	-	±12	
TUECal	Total unadjusted error after calibration	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ 1 kHz, BW 500 kHz		-	71.2	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz BW 500 kHz		-	71.6	-	
THD	Total harmonic distortion	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz		-	-78	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz		-	-79	-	

Table 78. DAC 1MSPS accuracy[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distortion ratio	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	70.4	-	dB
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	71	-	
ENOB	Effective number of bits	DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ, 1 kHz	-	11.4	-	bits
		DAC output buffer OFF CL ≤ 50 pF, no RL, 1 kHz	-	11.5	-	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{REF+} – 0.2) V when buffer is ON.

Table 79. DAC 15MSPS characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.71	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.71	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		V_{SSA}			
V_{DAC_OUT}	Voltage on DAC_OUT output	-		0	-	V_{REF+}	V
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value)	V_{DDA}>2,7V With One comparator on DAC output	10%-90%	-	16	22	ns
			5%-95%	-	21	29	
			1%-99%	-	33	46	
			32lsb	-	40	53	
			1lsb	-	64	87	
		V_{DDA}>2,7V With One comparator and OPAMP on DAC output	10%-90%	-	24	32	
			5%-95%	-	32	43	
			1%-99%	-	49	67	
			32lsb	-	57	75	
			1lsb	-	93	125	

Table 79. DAC 15MSPS characteristics[1] (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value)	V_{DDA}<2,7V With One comparator on DAC output	10%-90%	-	16	88	ns
			5%-95%	-	21	116	
			1%-99%	-	33	181	
			32lsb	-	40	196	
			1lsb	-	64	332	
		V_{DDA}<2,7V With One comparator and OPAMP on DAC output	10%-90%	-	24	128	
			5%-95%	-	32	170	
			1%-99%	-	49	265	
			32lsb	-	57	284	
			1lsb	-	93	483	
t_{WAKEUP}[2]	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode CL ≤ 10 pF		-	1.4	3.5	µs
PSRR	V_{DDA} supply rejection ratio	V_{DD} > 2.7 V		65	85	-	dB
		V_{DD} <2.7 V		40	85	-	
t_{SAMP}	Sampling time in sample and hold mode (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1LSB)	-		-	TBD	TBD	µs
CI_{int}	Internal sample and hold capacitor	-		-	4	5	pF
dV/dt (hold phase)	Voltage decay rate in Sample and hold mode, during hold phase	CSH = 4 pF T = 55°C		-	TBD	-	µV/ms
I_{DDA}(DAC)	DAC consumption from V_{DDA}	No load, middle code (0x800)		-	TBD	TBD	µA
I_{DDV}(DAC)	DAC consumption from V_{REF+}	No load, middle code (0x800)[3]		-	720	955	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Worst case consumption is at code 0x800.

Table 80. DAC 15MSPS accuracy(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity (2)	-	-2	-	2	LSB
INL	Integral non linearity(3)	CL ≤ 50 pF, no RL	-5	-	5	
TUE	Total unadjusted error	CL ≤ 50 pF, no RL	-5	-	5	
DCS	Dynamic code spike	Spike amplitude on DAC voltage when DAC output value is decreasing	-	0	4	

1. Guaranteed by design.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at code i and the value at code i on a line drawn between code 0 and last code 4095. Offset error is included.

5.3.21 Voltage reference buffer characteristics

Table 81. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	VRS = 00	2.4	-	3.6	V
			VRS = 01	2.8	-	3.6	
			VRS = 10	3.135	-	3.6	
		Degraded mode(2)	VRS= 00	1.65	-	2.4	
			VRS = 01	1.65	-	2.8	
			VRS= 10	1.65	-	3.135	
V_{REFBUF_OUT}	Voltage reference output	Normal mode(3)	VRS= 00	2.044	2.048	2.052	
			VRS= 01	2.496	2.5	2.504	
			VRS = 10	2.896	2.9	2.904	
		Degraded mode(2)	VRS= 00	V_{DDA} -250 mV	-	V_{DDA}	
			VRS = 01	V_{DDA} -250 mV	-	V_{DDA}	
			VRS = 10	V_{DDA} -250 mV	-	V_{DDA}	
V_{REFOUT_TEMP}(3)	Voltage reference output spread over the temperature range	V_{DDA} = 3V		-	-	See *Figure 30*, *Figure 31*, *Figure 32*	mV
TRIM	Trim step resolution	-		-	±0.05	±0.1	%
CL	Load capacitor	-		0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-		-	-	2	Ω
I_{load}	Static load current	-		-	-	6.5	mA
I_{line_reg}(4)	Line regulation	-		-	1000	2000	ppm/V
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	Tcoeff_vrefint + 50(5)	ppm/ °C
		0 °C < TJ < +50 °C		-	-		
PSRR	Power supply rejection	DC		40	55	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(6)		-	300	350	µs
		CL = 1.1 µF(6)		-	500	650	
		CL = 1.5 µF(6)		-	650	800	

Table 81. VREFBUF characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_ OUT during start-up phase (7)	-	-	8	-	mA
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	
		I_{load} = 6.5 mA	-	45	80	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which follows (V_{DDA} - drop voltage).
3. Guaranteed by characterization results.
4. Line regulation is given for overall supply variation, in normal mode.
5. Tcoeff_vrefint refer to Tcoeff parameter in the embedded voltage reference section.
6. The capacitive load must include a 100 nF low ESR capacitor in order to cut-off the high frequency noise.
7. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V], [2.8 V to 3.6 V] and [3.135 V to 3.6 V] respectively for VRS=0,1 and 2.

Figure 30. V_{REFOUT_TEMP} in case VRS = 00

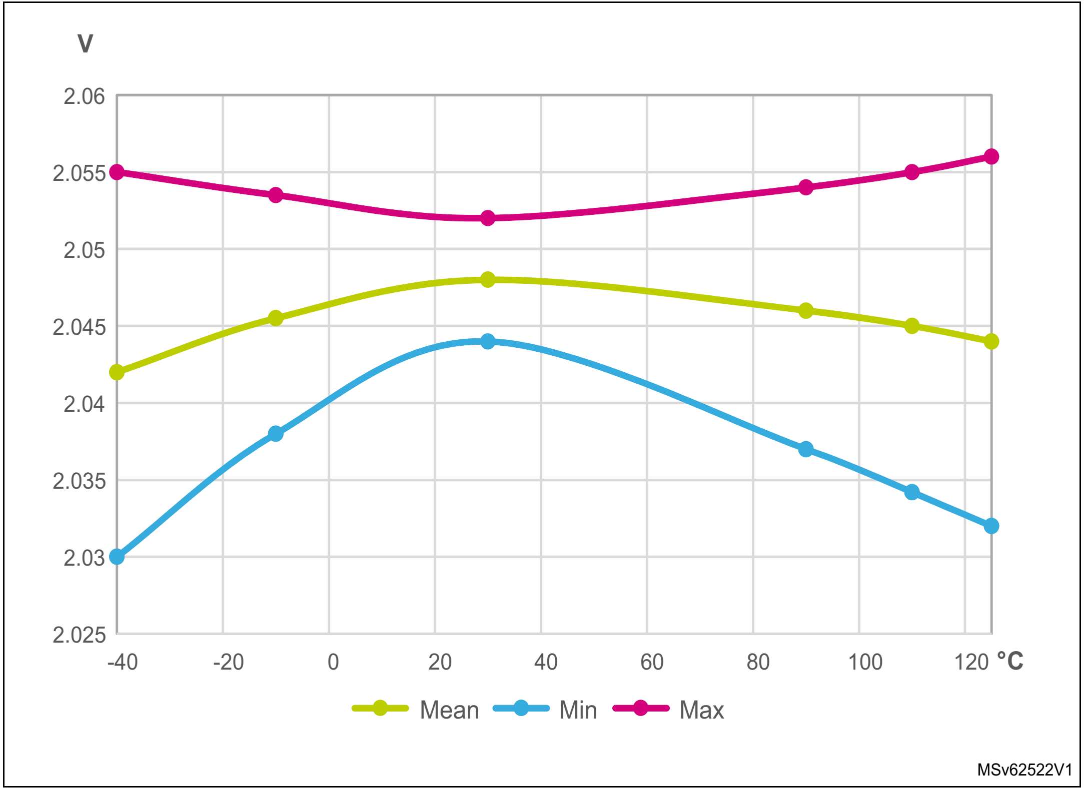


Figure 31. V_{REFOUT_TEMP} in case VRS = 01

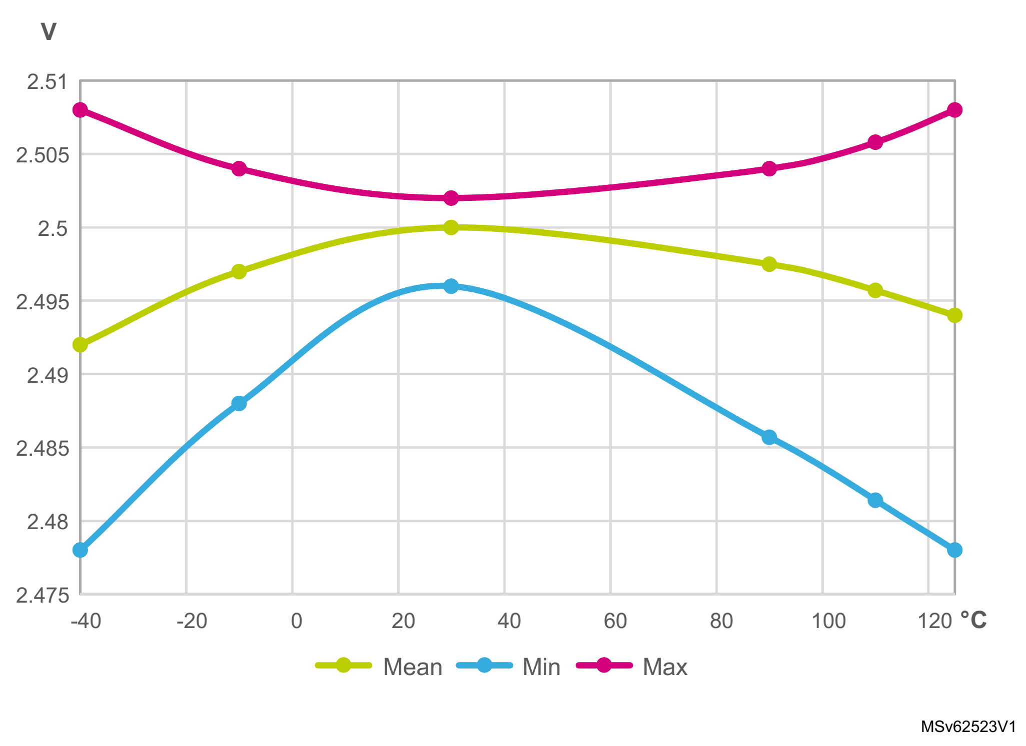
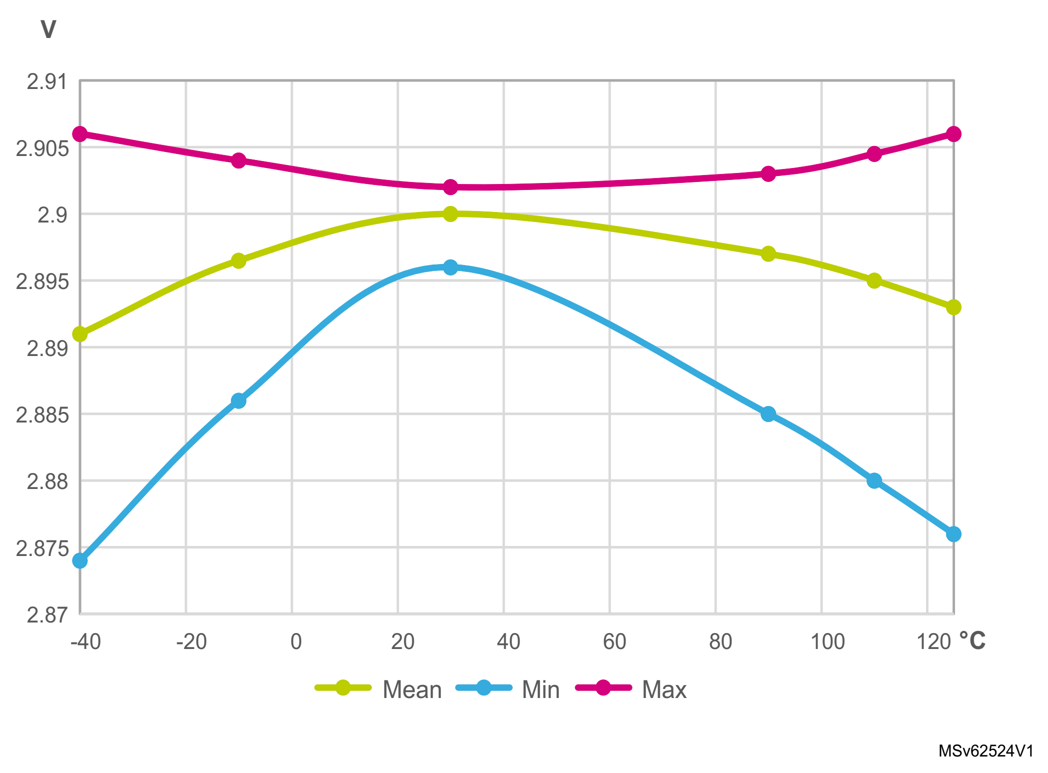


Figure 32. V_{REFOUT_TEMP} in case VRS = 10



5.3.22 Comparator characteristics

Table 82. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		VREFINT			
V_{SC}(3)	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	-		-	-	5	µs
t_D(4)	Propagation delay (From COMP input pin to COMP output pin) for 200 mV step with 100 mV overdrive	50pF load on output	V_{DDA} < 2.7 V	-	-	35	ns
			V_{DDA} ≥2.7 V	-	16.7	31	ns
V_{offset}(3)	Comparator offset error	Full V_{DDA} voltage range, full temperature range		-9	-6/+2	3	mV
V_{hys}	Comparator hysteresis	HYST[2:0] = 0		-	0	-	mV
		HYST[2:0] =1		4	9	16	
		HYST[2:0] = 2		7	18	32	
		HYST[2:0] = 3		11	27	47	
		HYST[2:0] = 4		15	36	63	
		HYST[2:0] = 5		19	45	79	
		HYST[2:0] = 6		23	54	95	
		HYST[2:0] = 7		26	63	110	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Static		-	450	720	µA
		With 50 kHz ±100 mV overdrive square signal		-	TBD	-	

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 20: Embedded internal voltage reference*.
3. Guaranteed by characterization results.
4. Typical value (3V) is an average for all comparators propagation delay.

5.3.23 Operational amplifiers characteristics

Table 83. OPAMP characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	3.3	3.6	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
VI_{OFFSET}(3)	Input offset voltage	25 °C, No Load on output.	-	-	±1.5	mV
		All voltage/temperature.	-	-	±3	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±10	-	µV/°C
TRIMOFFSETP	Offset trim step at low common input voltage (0.1 x V_{DDA})	-	-	1.1	1.2	mV
TRIMOFFSETN	Offset trim step at high common input voltage (0.9 x V_{DDA})	-	-	1.3	1.65	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	60	-	dB
PSRR	Power supply rejection ratio	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ DC Vcom=V_{DDA}/2	TBD	80	-	dB
GBW	Gain Bandwidth Product	100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV	7	13	-	MHz
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	2.5	6.5	-	V/µs
		High-speed mode	18	45	-	
AO	Open loop gain	100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV	65	95	-	dB
		200mV ≤ Output dynamic range ≤ V_{DDA} - 200mV	75	95	-	
V_{OHSAT}(3)	High saturation voltage	I_{load} = max or R_{load} = min Input at V_{DDA}. Follower mode	V_{DDA} - 100	-	-	mV
V_{OLSAT}(3)	Low saturation voltage	I_{load} = max or R_{load} = min Input at 0. Follower mode	-	-	100	
φ_m	Phase margin	Follower mode, Vcom=V_{DDA}/2	-	65	-	°
GM	Gain margin	Follower mode, Vcom=V_{DDA}/2	-	10	-	dB

Table 83. OPAMP characteristics(1) (2) (continued)

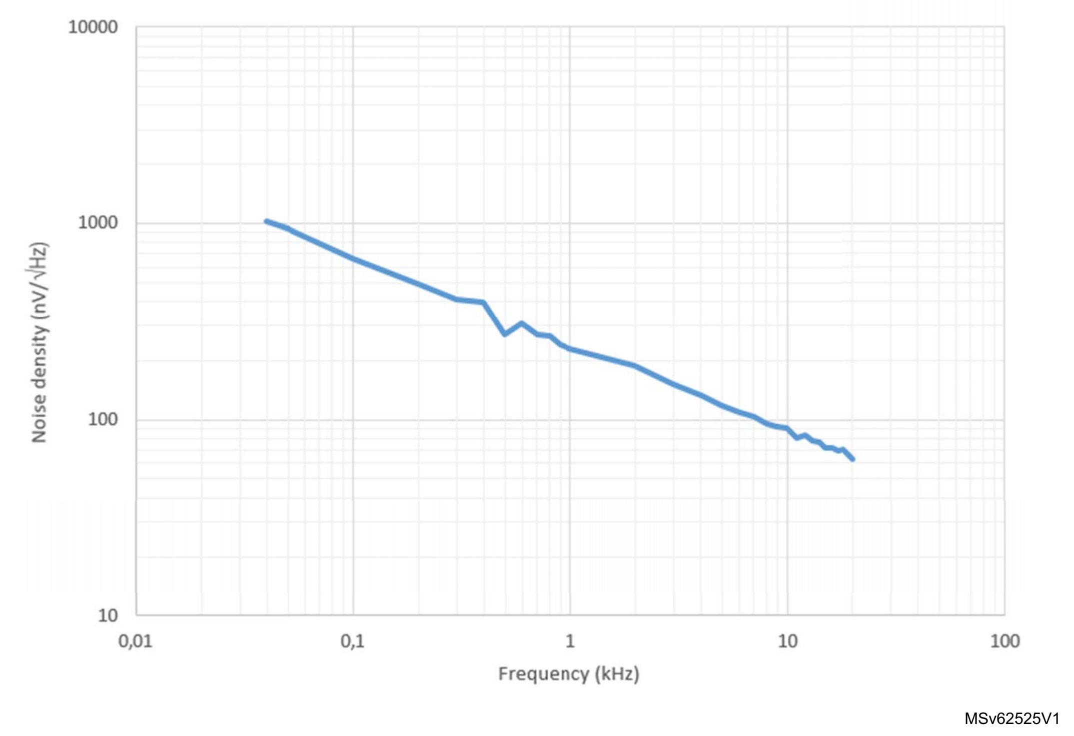
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WAKEUP}(3)	Wake up time from OFF state.	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ follower configuration	-	3	6	µs
		High-speed mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq$ 20 kΩ follower configuration	-	3	6	
I_{bias}	OPAMP input bias current	See I_{leak} parameter in *Table 57: I/O static characteristics* for given pin.					
PGA gain	Non inverting gain value(4)	PGA Gain = 2 0.1 ≤ Out dynamic range ≤ V_{DDA} - 0.1	$V_{DDA} < 2.2$	-2	-	2	%
			$V_{DDA} \geq 2.2$	-1	-	1	
		PGA Gain=4, 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=8 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=16, 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=32 200mV ≤ Output ≤ V_{DDA} - 200mV		-2	-	2	
		PGA Gain=64 200mV ≤ Output dynamic range ≤ V_{DDA} - 200mV		-2	-	2	
	Inverting gain value	PGA Gain = -1 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV	$V_{DDA} < 2.2$	-2	-	2	%
			$V_{DDA} \geq 2.2$	-1	-	1	
		PGA Gain=-3, 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=-7 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=-15, 100mV ≤ Output dynamic range ≤ V_{DDA} - 100mV		-1	-	1	
		PGA Gain=-31 200mV ≤ Output ≤ V_{DDA} - 200mV		-2	-	2	
		PGA Gain=-63 200mV ≤ Output dynamic range ≤ V_{DDA} - 200mV		-5	-	2	

Table 83. OPAMP characteristics(1) (2) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{network}$	R2/R1 internal resistance values in non-inverting PGA mode(5)	PGA Gain = 2		-	10/10	-	kΩ/kΩ
		PGA Gain = 4		-	30/10	-	
		PGA Gain = 8		-	70/10	-	
		PGA Gain = 16		-	150/10	-	
		PGA Gain = 32		-	310/10	-	
		PGA Gain = 64		-	630/10	-	
	R2/R1 internal resistance values in inverting PGA mode(5)	PGA Gain = -1		-	10/10	-	
		PGA Gain = -3		-	30/10	-	
		PGA Gain = -7		-	70/10	-	
		PGA Gain = -15		-	150/10	-	
		PGA Gain = -31		-	310/10	-	
		PGA Gain = -63		-	630/10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	+15	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2		-	GBW/2	-	MHz
		Gain = 4		-	GBW/4	-	
		Gain = 8		-	GBW/8	-	
		Gain = 16		-	GBW/16	-	
		Gain = 32		-	GBW/32	-	
		Gain = 64		-	GBW/64	-	
	PGA bandwidth for different inverting gain	Gain = -1		-	GBW/2	-	MHz
		Gain = -3		-	GBW/4	-	
		Gain = -7		-	GBW/8	-	
		Gain = -15		-	GBW/16	-	
		Gain = -31		-	GBW/32	-	
		Gain = -63		-	GBW/64	-	
eN	Voltage noise density	at 1 kHz, Output loaded with 4 kΩ		-	250	-	nV/√Hz
		at 10 kHz, Output loaded with 4 kΩ		-	90	-	
I_{DDA}(OPAMP)	OPAMP consumption from V_{DDA}	Normal mode	No load, follower mode	-	1.3	2.2	mA
		High-speed mode		-	1.4	2.6	
$T_{S\_OPAMP\_VOUT}$	ADC sampling time when reading the OPAMP output. OPAINTOEN=1	$V_{DDA} < 2V$		300	-	-	ns
		$V_{DDA} \geq 2V$		200	-	-	
I_{DDA}(OPAMPINT)	OPAMP consumption from V_{DDA}. OPAINTOEN=1	Normal mode	no load, follower mode	-	0.45	0.7	mA
		High-speed mode		-	0.5	0.8	

1. Guaranteed by design, unless otherwise specified.
2. Data guaranteed on normal and high speed mode unless otherwise specified.
3. Guaranteed by characterization results.
4. Valid also for inverting gain configuration with external bias.
5. R2 is the internal resistance between OPAMP output and OPAMP inverting input. R1 is the internal resistance between OPAMP inverting input and ground. The PGA gain =1+R2/R1

Figure 33. OPAMP noise density @ 25°C



5.3.24 Temperature sensor characteristics

Table 84. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(2)	0.742	0.76	0.785	V
$t_{START-RUN}$(1)	Start-up time in Run mode (start-up of buffer)	-	8	15	µs
t_{START_CONT}(3)	Start-up time when entering in continuous mode	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from VDD, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 5: Temperature sensor calibration values*.
3. Continuous mode means RUN mode or Temperature Sensor ON.

5.3.25 V_{BAT} monitoring characteristics

Table 85. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	12	-	-	µs

1. Guaranteed by design.

Table 86. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

5.3.26 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 87. TIMx(1) characteristics(2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	6.66	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 170 MHz	0	75	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	0.00666	436.9	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 170 MHz	-	28.63	s
f_{ENC}	Encoder frequency on TI1 and TI2 input pins	-	0	$f_{TIMxCLK}/4$	MHz
		$f_{TIMxCLK}$ = 170MHz	0	37.5	MHz
$t_{W(INDEX)}$	Index pulsewidth on ETR input	-	2	-	Tck
$t_{W(TI1, TI2)}$	Min pulsewidth on TI1 and TI2 inputs in all encoder modes except directional clock x1	-	2	-	Tck
	Min pulsewidth on TI1 and TI2 inputs in directional clock x1	-	3	-	Tck

1. TIMx, is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16, 17 or 20.
2. Guaranteed by design.

Table 88. IWDG min/max timeout period at 32 kHz (LSI)(1)(2)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. Guaranteed by design.
2. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 89. WWDG min/max timeout value at 170 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0241	1.542	ms
2	1	0.0482	3.084	
4	2	0.0964	6.168	
8	3	0.1928	12.336	

1. Guaranteed by design.

5.3.27 Communication interfaces characteristics

I^{2}C interface characteristics

The I2C interface meets the timings requirements of the I^{2}C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs") and when the I2CCLK frequency is greater than the minimum shown in the table below.

Table 90. Minimum I2CCLK frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f(I2CCLK)	I2CCLK frequency	Standard mode		2	MHz
		Fast-mode	Analog Filtre ON DNF=0	8	
			Analog Filtre OFF DNF=1	9	
		Fast-mode Plus	Analog Filtre ON DNF=0	17	
			Analog Filtre OFF DNF=1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present.
- The 20mA output drive requirement in Fast-mode Plus is supported partially. This limits the maximum load Cload supported in Fm+, which is given by these formulas:
  - t_r(SDA/SCL)=0.8473 x R_p x C_{load}
  - R_p(min)= (V_{DD} - V_{OL}(max)) / I_{OL}(max)

Where Rp is the I2C lines pull-up. Refer to *Section 5.3.14: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 91* below for the analog filter characteristics:

Table 91. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	90(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI characteristics

Unless otherwise specified, the parameters given in *Table 92* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 17: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 92. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max[2]	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	-	75	MHz
		Master mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Master transmitter mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1			50	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range V1			41	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range V1			27	
		1.71 V < V_{DD} < 3.6 V Voltage Range V2			13	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*T_{pclk}$	-	-	-
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*T_{pclk}$	-	-	-
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI prescaler = 2	$T_{pclk}-1$	T_{pclk}	$T_{pclk}+1$	ns
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	-	ns
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns

Table 92. SPI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max[2]	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range V1	-	9	12	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V1	-	9	18	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range V2	-	13	22	
$t_{v(MO)}$		Master mode	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	
		Slave mode Range V2	9	-	-	
$t_{h(MO)}$		Master mode	2	-	-	

1. Guaranteed by characterization results.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high-phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while Duty(SCK) = 50%.

Figure 34. SPI timing diagram - slave mode and CPHA = 0

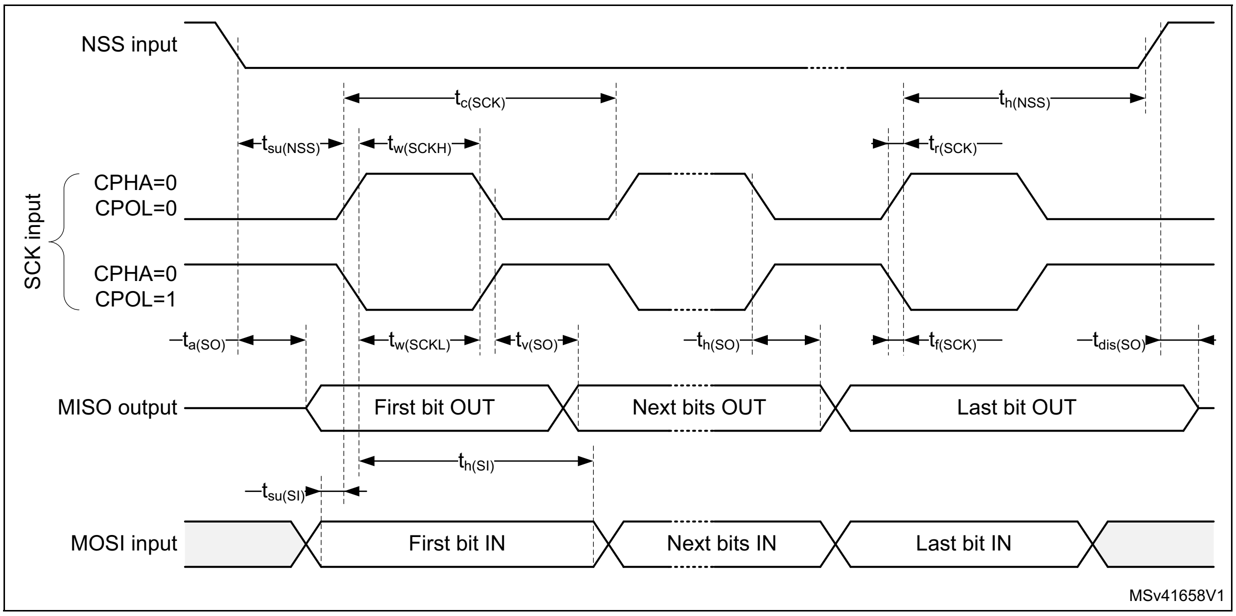
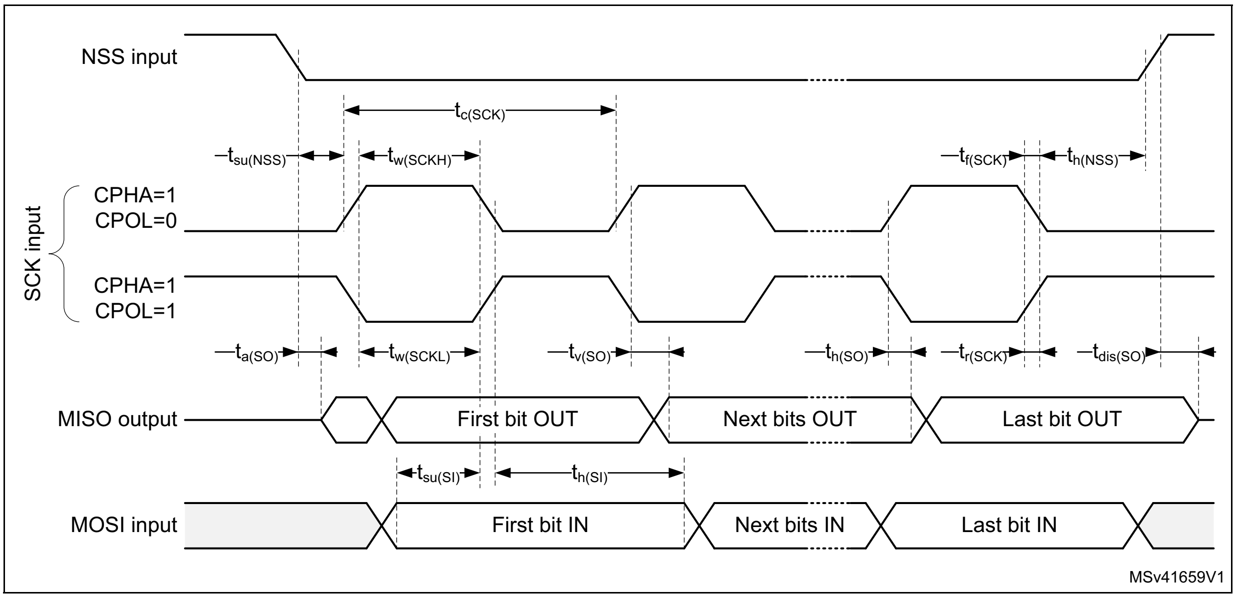
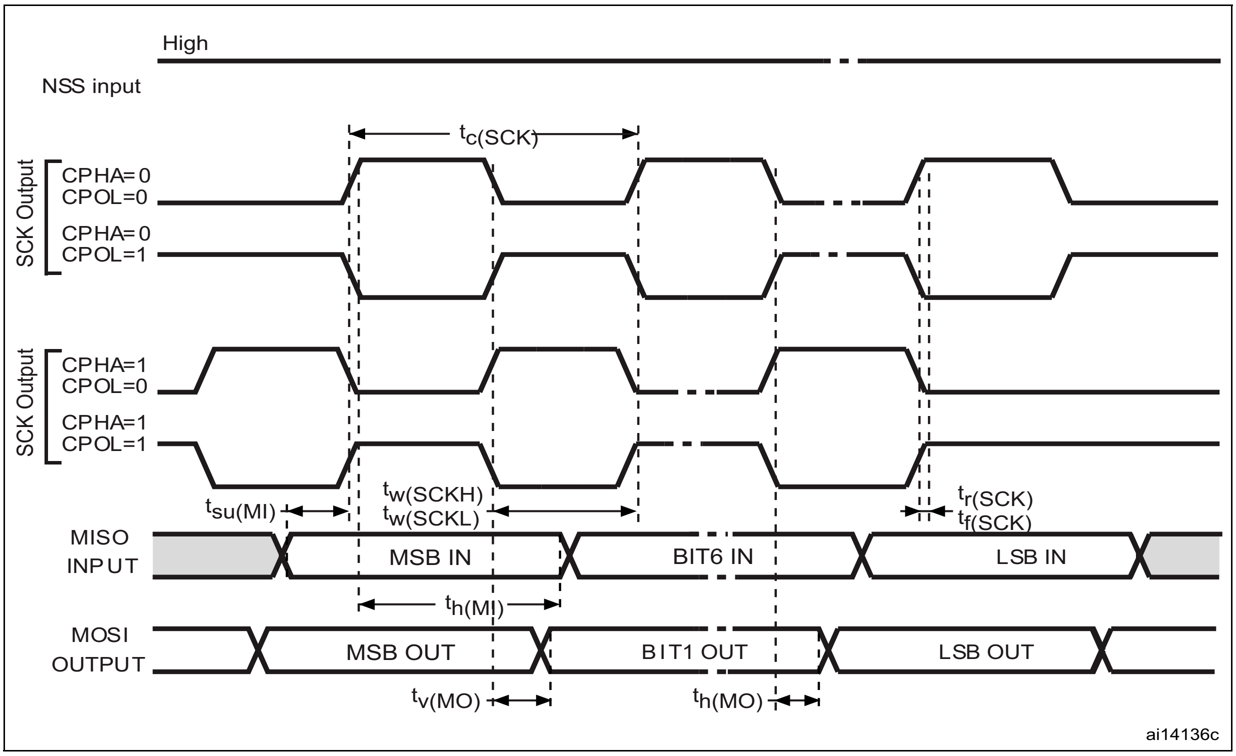


Figure 35. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 36. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

I2S characteristics

Unless otherwise specified, the parameters given in *Table 93* for I2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 93. I2S characteristics(1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{MCLK}	I2S Main clock output	-		256x8K	256*Fs(2)	MHz
f_{CK}	I2S clock frequency	Master data		-	64xFs	MHz
		Slave data		-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver		30	70	%
$t_{v(WS)}$	WS valid time	Master mode		-	6	ns
$t_{h(WS)}$	WS hold time	Master mode		3	-	
		Slave mode		2	-	
$t_{su(WS)}$	WS setup time	Slave mode		4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver		3	-	
$t_{su(SD\_SR)}$		Slave receiver		4	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver		4	-	
$t_{h(SD\_SR)}$		Slave receiver		2	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	15	
			$1.65\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-	22	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)		-	3	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)		7	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)		1	-	

1. Guaranteed by characterization results, not tested in production.
2. 256xFs maximum is 49.152 MHz.

Note: *Refer to the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs" I2S section for more details about the sampling frequency (Fs), f_{MCK}, f_{CK}, D_{CK} values reflect only the digital peripheral behavior, source clock precision might slightly change the values D_{CK} depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*

SAI characteristics

Unless otherwise specified, the parameters given in *Table 94* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in*Table 17: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 94. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	33	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	22	
		Master receiver Voltage Range 1	-	22	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	45	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	29	
		Slave receiver Voltage Range 1	-	50	
		Slave transmitter Voltage Range 2	-	13	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	22	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	2	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	1	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	2.5	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11	ns
		Slave transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	17	
		Slave transmitter (after enable edge) voltage range V2	-	20	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	ns

Table 94. SAI characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	14	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	21	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	10	-	ns

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.

Figure 37. SAI master timing waveforms

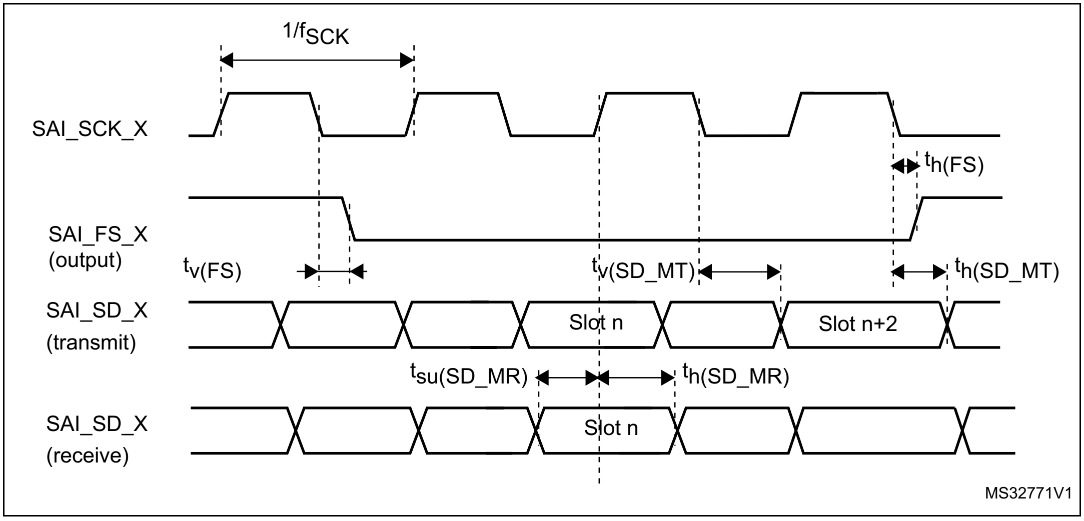
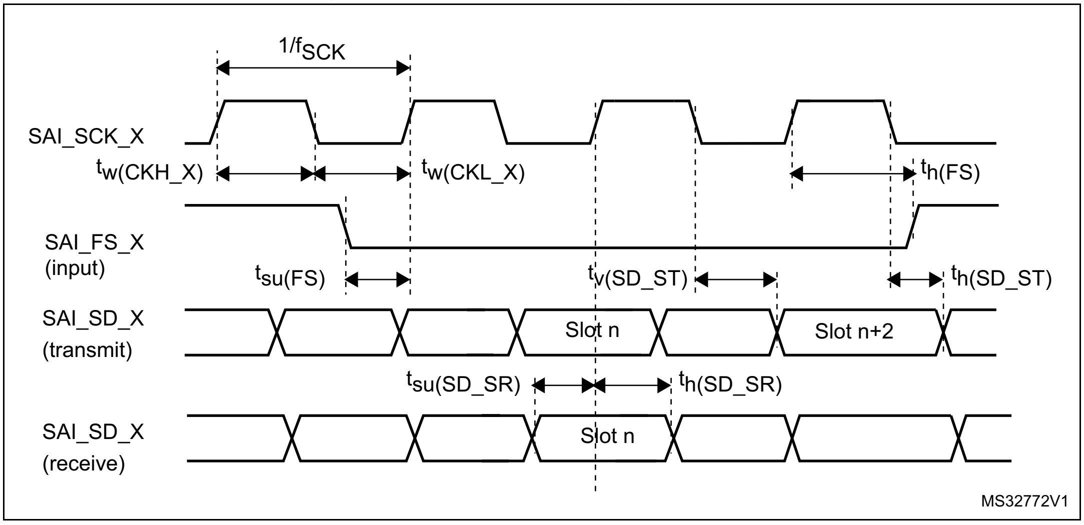


Figure 38. SAI slave timing waveforms



CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

USB characteristics

The device USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 95. USB electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	USB transceiver operating voltage		3.0(2)	-	3.6	V
$t_{Crystal\_less}$	USB crystal less operation temperature		-15	-	85	°C
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1500	Ω
R_{PUR}	Embedded USB_PD pull-up value during reception		1400	2300	3200	
Z_{sDRV}(3)	Output driver impedance(4)	Driving high and low	28	36	44	Ω

1. TA = -40 to 125 °C unless otherwise specified.
2. The device USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics, which are degraded in the 2.7-to-3.0 V voltage range.
3. Guarantee by design.
4. No external termination series resistors are required on USB_PD (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USART interface characteristics

Unless otherwise specified, the parameters given in *Table 96* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 96*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 96. USART electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	21	MHz
		Slave mode	-	-	22	
$t_{su}(NSS)$	NSS setup time	Slave mode	t_{ker} + 2	-	-	ns
$t_h(NSS)$	NSS hold time	Slave mode	2	-	-	
$t_w(CKH)$ $t_w(CKL)$	CK high and low time	Master mode	$1/f_{ck}/2-1$	$1/f_{ck}/2$	$1/f_{ck}/2+1$	ns
$t_{su}(RX)$	Data input setup time	Master mode	t_{ker} + 2	-	-	ns
		Slave mode	2	-	-	
$t_h(RX)$	Data input hold time	Master mode	1	-	-	
		Slave mode	0.5	-	-	

Table 96. USART electrical characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_v(TX)	Data output valid time	Master mode	-	0.5	1.5	ns
		Slave mode	-	10	22	
t_h(RX)	Data output hold time	Master mode	0	-	-	
		Slave mode	7	-	-	

1. Based on characterization, not tested in production.

5.3.28 FSMC characteristics

Unless otherwise specified, the parameters given in *Table 97* to *Table 110* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 39 through *Figure 42* represent asynchronous waveforms and *Table 97* through *Table 104* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataHoldTime = 0x1
- ByteLaneSetup = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the THCLK is the HCLK clock period.

Figure 39. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

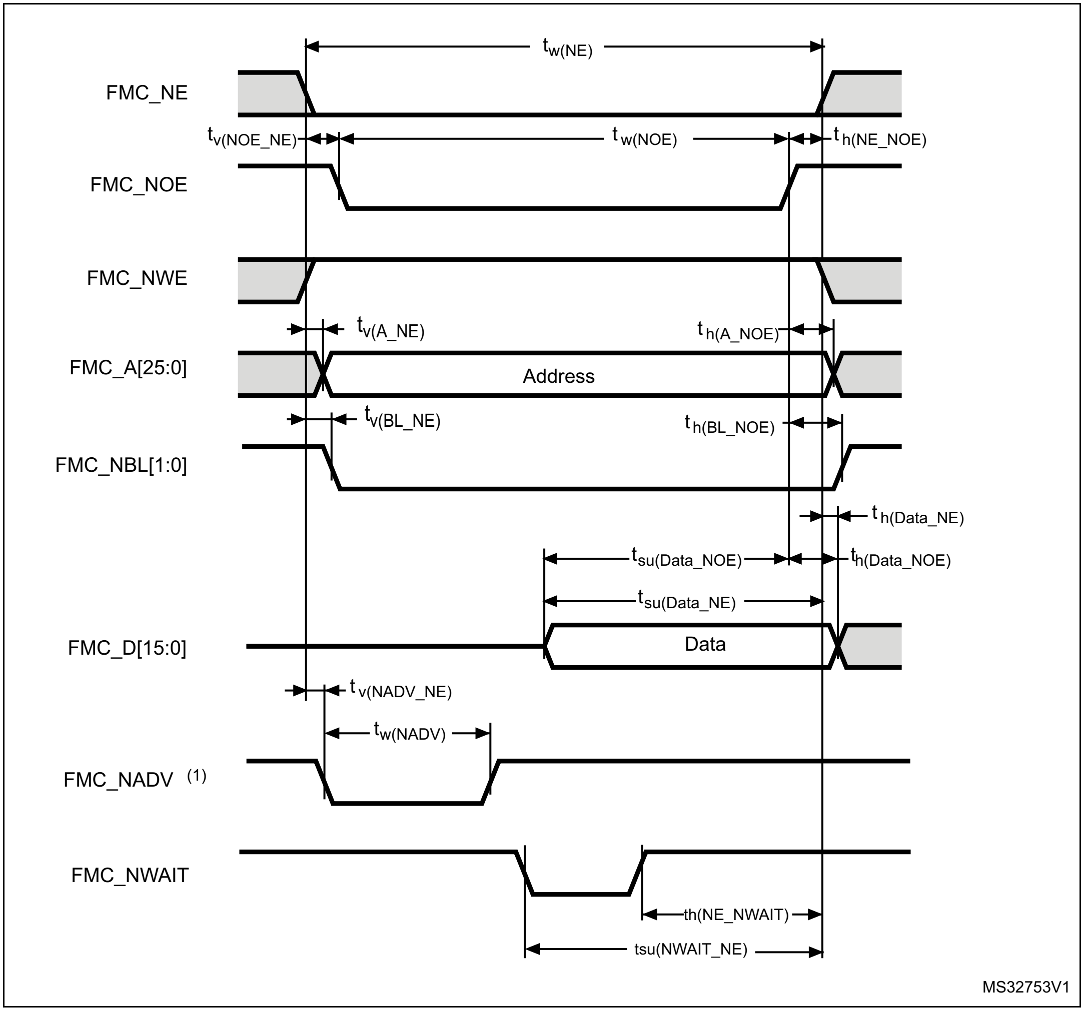


Table 97. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3 T_{HCLK} – 0.5	3T_{HCLK} + 1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	2 T_{HCLK} – 0.5	2 T_{HCLK} + 1	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	2 T_{HCLK} – 1	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK} + 20	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	20	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1.5	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK} + 8	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 98. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	-	8 T_{HCLK} + 1	ns
$t_{w(NOE)}$	FMC_NWE low time	7 T_{HCLK} - 1	7 T_{HCLK} + 0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	T_{HCLK}	-	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5 T_{HCLK} + 17	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4 T_{HCLK} + 17	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 40. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

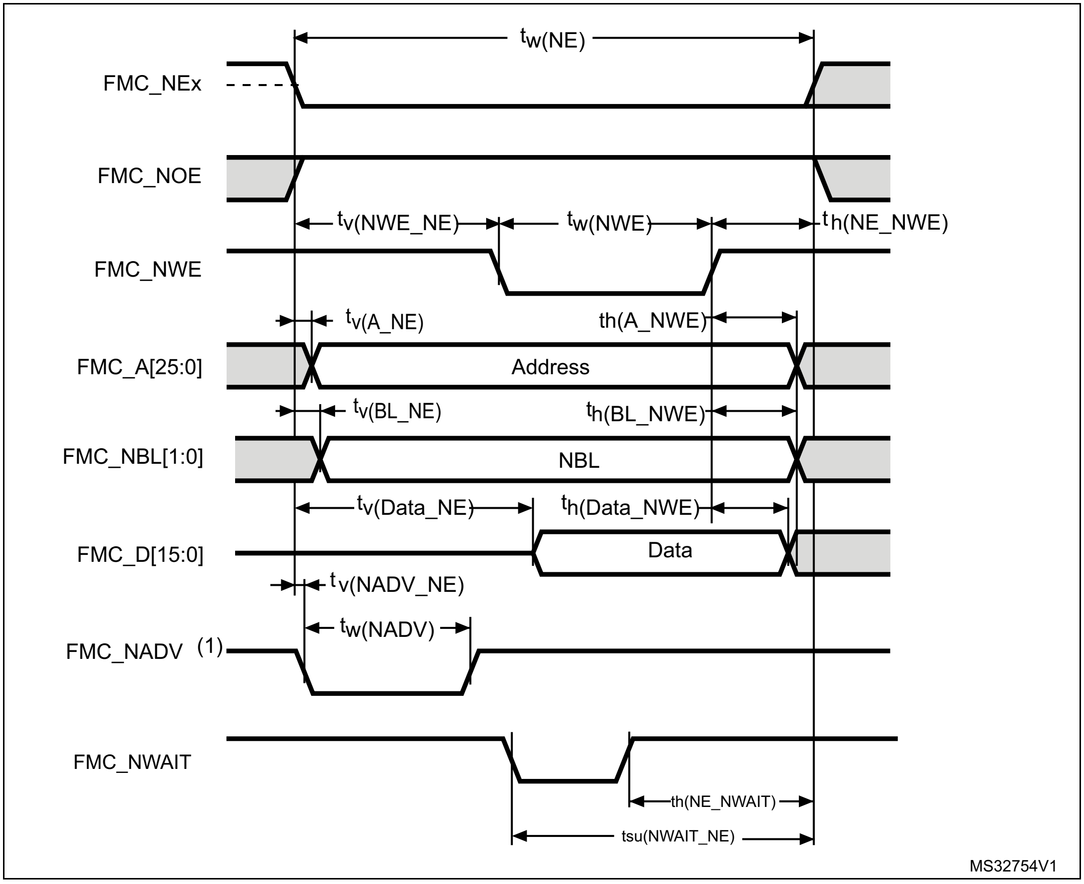


Table 99. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3 T_{HCLK} - 0.5	3 T_{HCLK} + 1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK} - 0.5	T_{HCLK} + 1	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK} -2	T_{HCLK} + 1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	T_{HCLK} - 0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	T_{HCLK} - 1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	T_{HCLK} + 0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK} + 2	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	T_{HCLK} + 6	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1.5	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK} + 0.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 100. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9 T_{HCLK} - 1	9 T_{HCLK} + 1	ns
$t_{w(NWE)}$	FMC_NWE low time	6 T_{HCLK} - 1	6 T_{HCLK} + 1	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	7 T_{HCLK} + 17	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	7 T_{HCLK} + 17	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 41. Asynchronous multiplexed PSRAM/NOR read waveforms

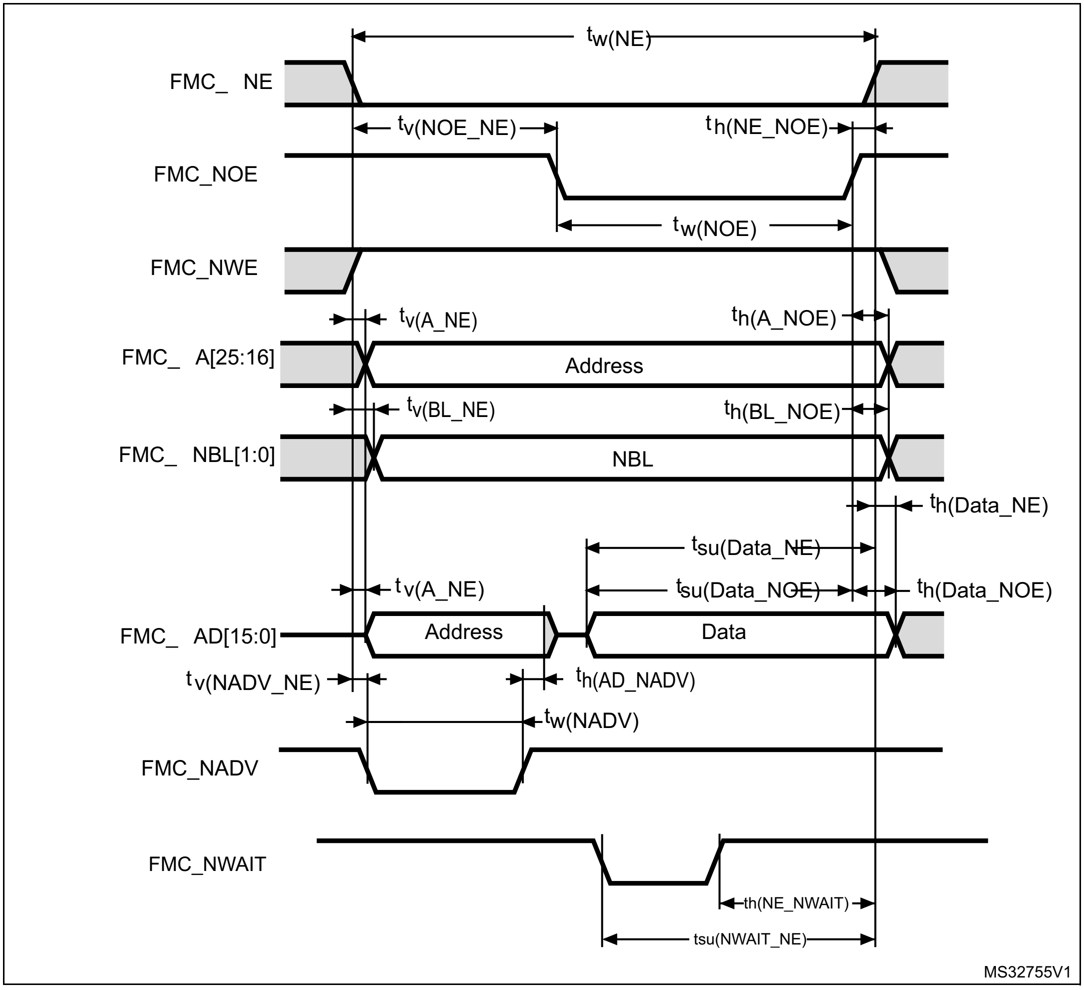


Table 101. Asynchronous multiplexed PSRAM/NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	3 T_{HCLK} - 0.5	3 T_{HCLK} + 1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	2 T_{HCLK} - 0.5	2 T_{HCLK} + 0.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	T_{HCLK}	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0.5	1.5	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}	T_{HCLK} + 1.5	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	T_{HCLK} - 0.3	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	Address hold until next read operation	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	T_{HCLK} + 20	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	20	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 102. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8 T_{HCLK} - 1	8 T_{HCLK} + 1	ns
$t_{w(NOE)}$	FMC_NWE low time	7 T_{HCLK} - 1	7 T_{HCLK} + 0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5 T_{HCLK} + 17	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4 T_{HCLK} + 17	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Figure 42. Asynchronous multiplexed PSRAM/NOR write waveforms

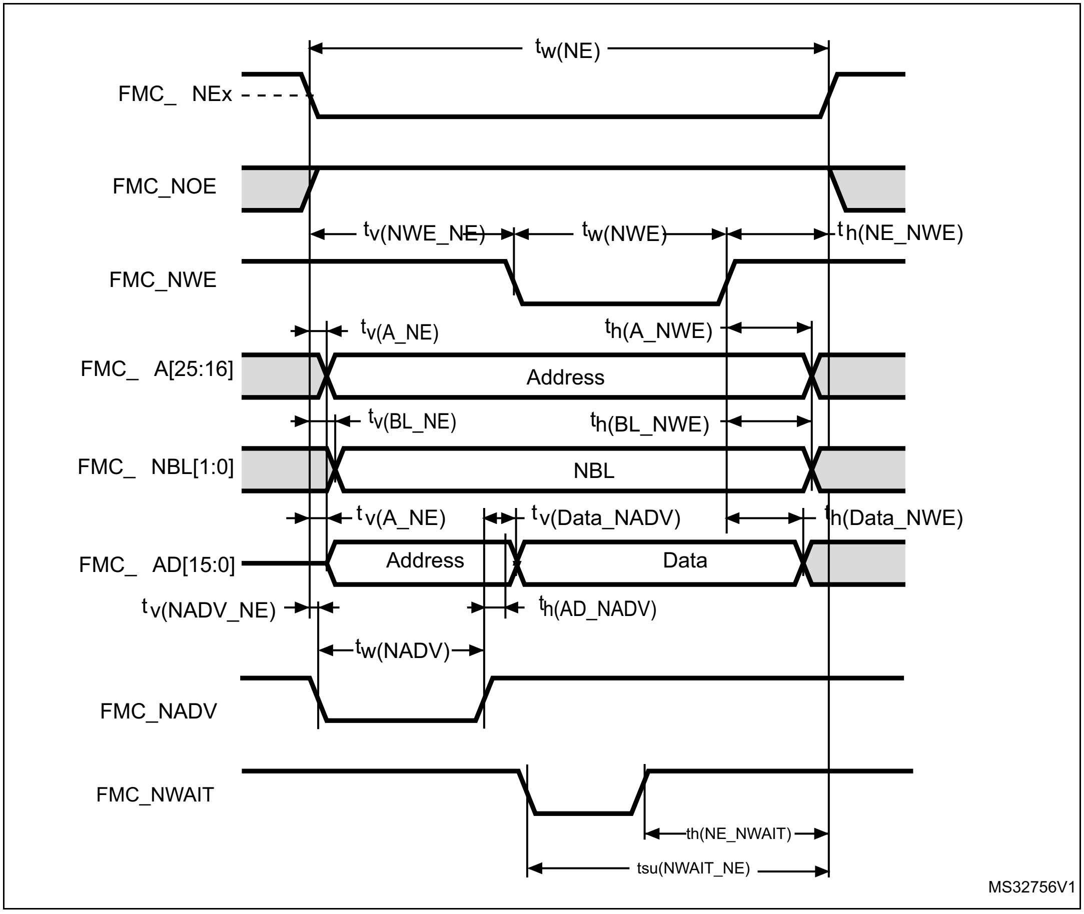


Table 103. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3\ T_{HCLK} - 0.5$	$3\ T_{HCLK} + 1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{HCLK} - 0.5$	$T_{HCLK} + 1$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{HCLK} - 2$	$T_{HCLK} + 1$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{HCLK} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{HCLK} + 0.5$	$T_{HCLK} + 1.5$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{HCLK} - 3$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	Address hold until next write operation	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{HCLK} + 2$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$T_{HCLK} + 6$	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 104. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9\ T_{HCLK} - 1$	$9\ T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6\ T_{HCLK} - 1$	$6\ T_{HCLK} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$7\ T_{HCLK} + 17$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$5\ T_{HCLK} + 17$	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Synchronous waveforms and timings

Figure 43 through *Figure 46* represent synchronous waveforms and *Table 105* through *Table 108* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the T_{HCLK} is the HCLK clock period.

- For 2.7 V ≤ V_{DD} ≤ 3.6 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 54 MHz for CLKDIV = 0x0 at CL = 30 pF (on FMC_CLK).
- For 1.71 V ≤ V_{DD} ≤ 2.7 V, maximum FMC_CLK = 60 MHz for CLKDIV = 0x1 and 32 MHz for CLKDIV = 0x0 at CL= 20 pF (on FMC_CLK).

Figure 43. Synchronous multiplexed NOR/PSRAM read timings

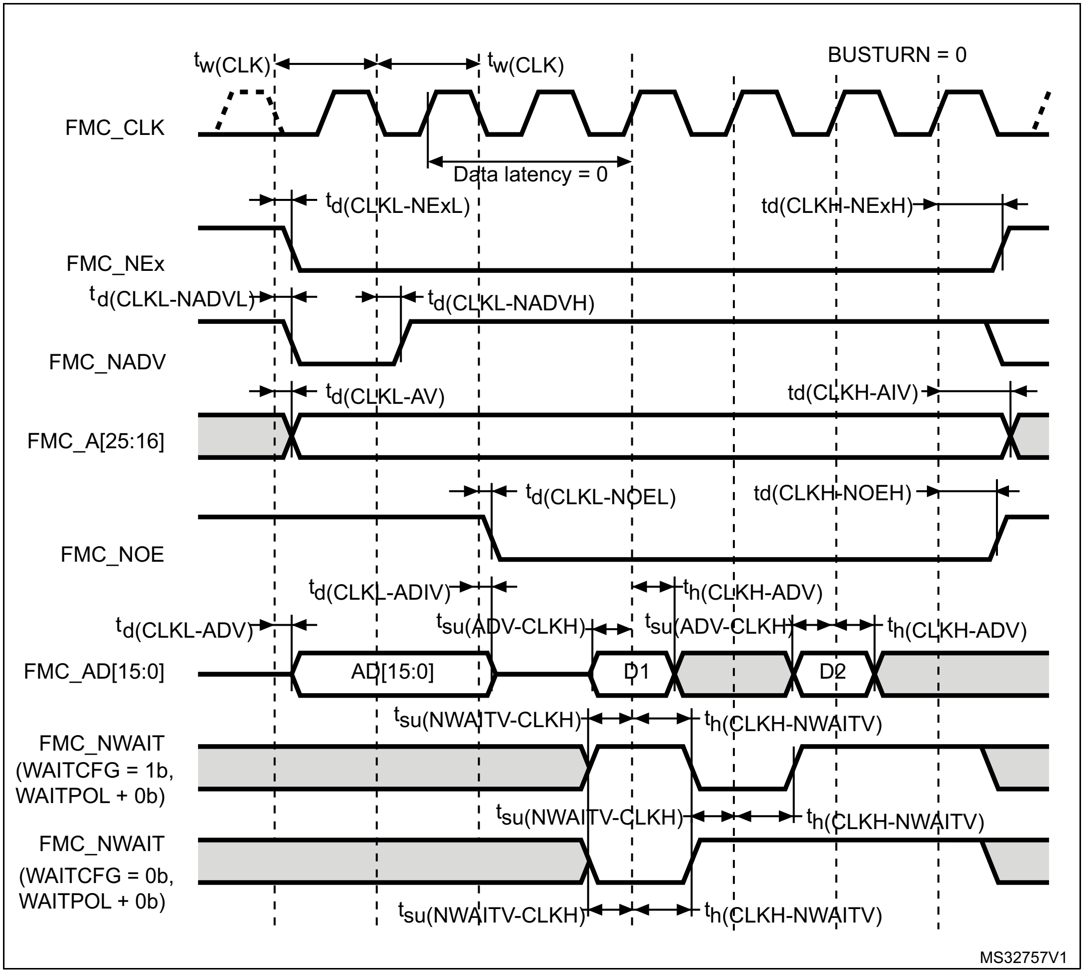


Table 105. Synchronous multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R*T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	3.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	4	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 44. Synchronous multiplexed PSRAM write timings

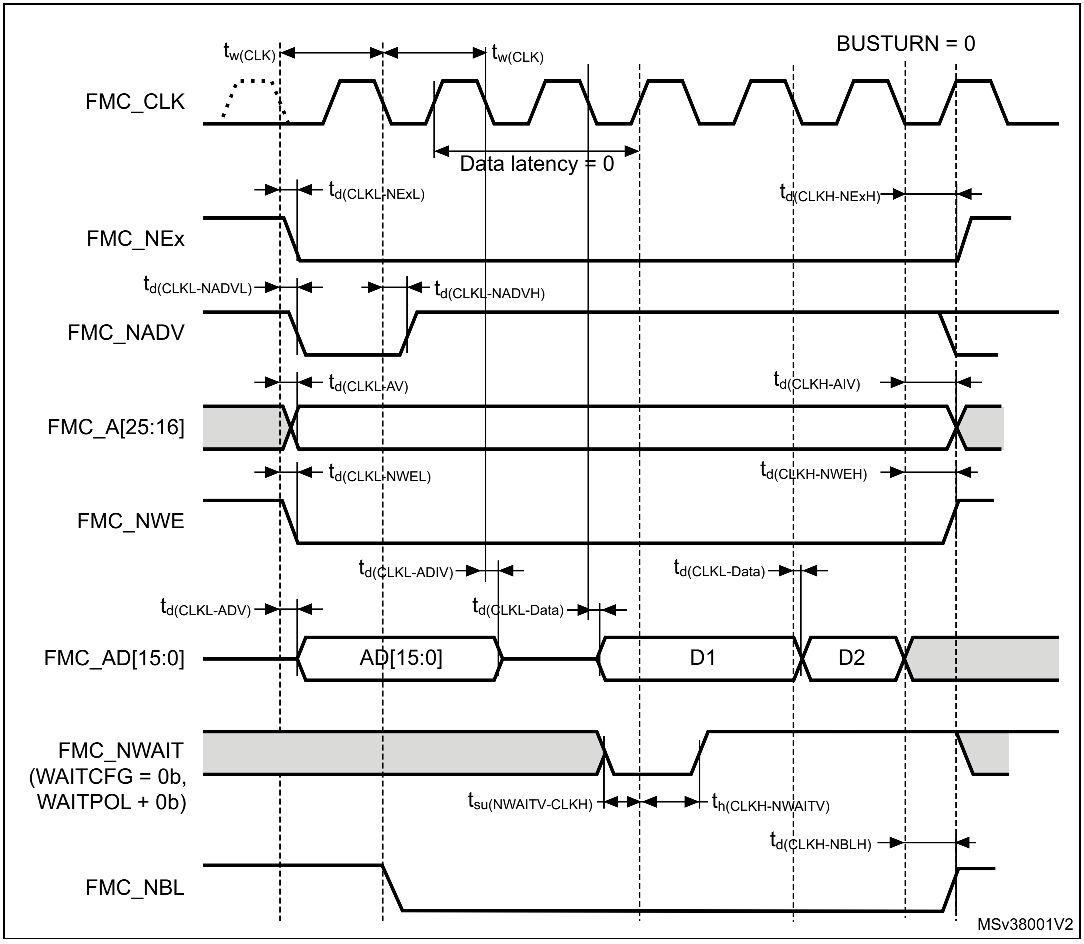


Table 106. Synchronous multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R*T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R*T_{HCLK}/2$ + 1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	3.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R*T_{HCLK}/2$ + 1	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R*T_{HCLK}/2$ + 1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R*T_{HCLK}/2$ + 1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 45. Synchronous non-multiplexed NOR/PSRAM read timings

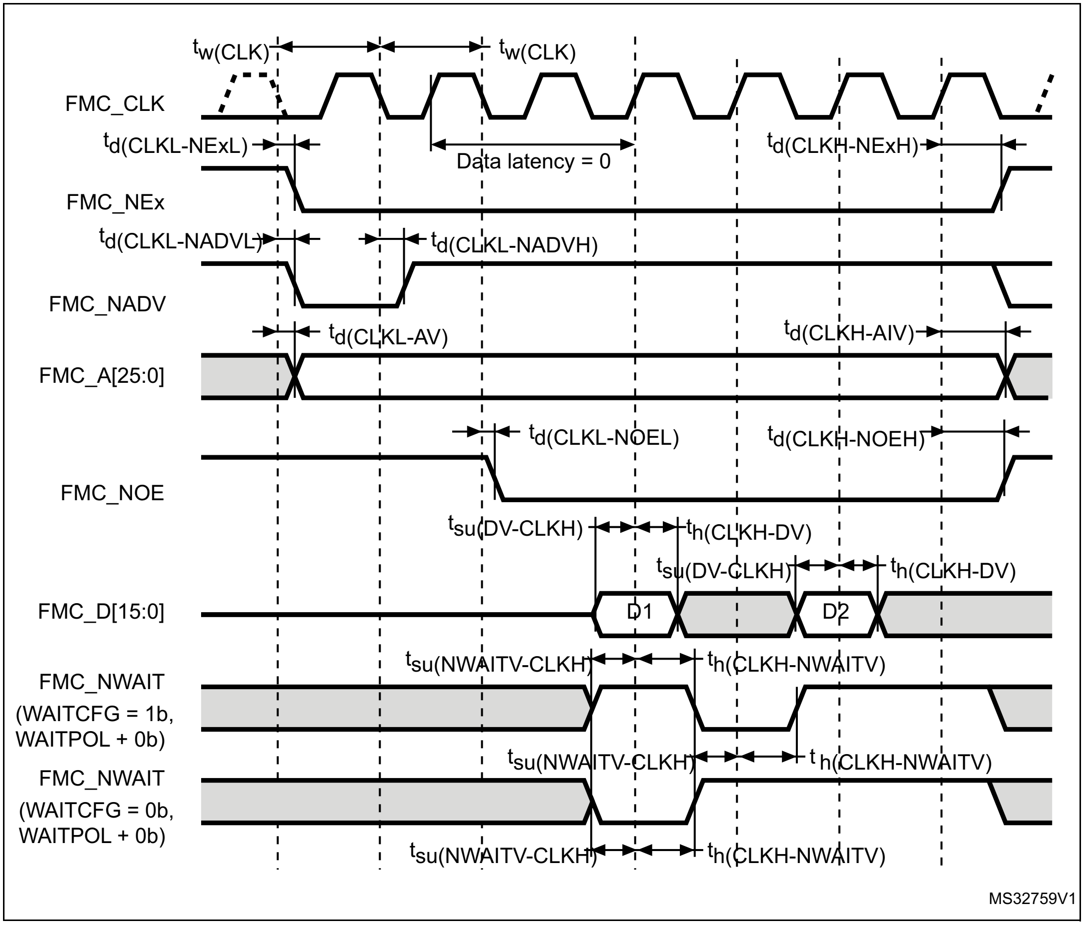


Table 107. Synchronous non-multiplexed NOR/PSRAM read timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R*T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R*T_{HCLK}/2$ + 1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	3.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R*T_{HCLK}/2$+- 1	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	2	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R*T_{HCLK}/2$ + 1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	4	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

Figure 46. Synchronous non-multiplexed PSRAM write timings

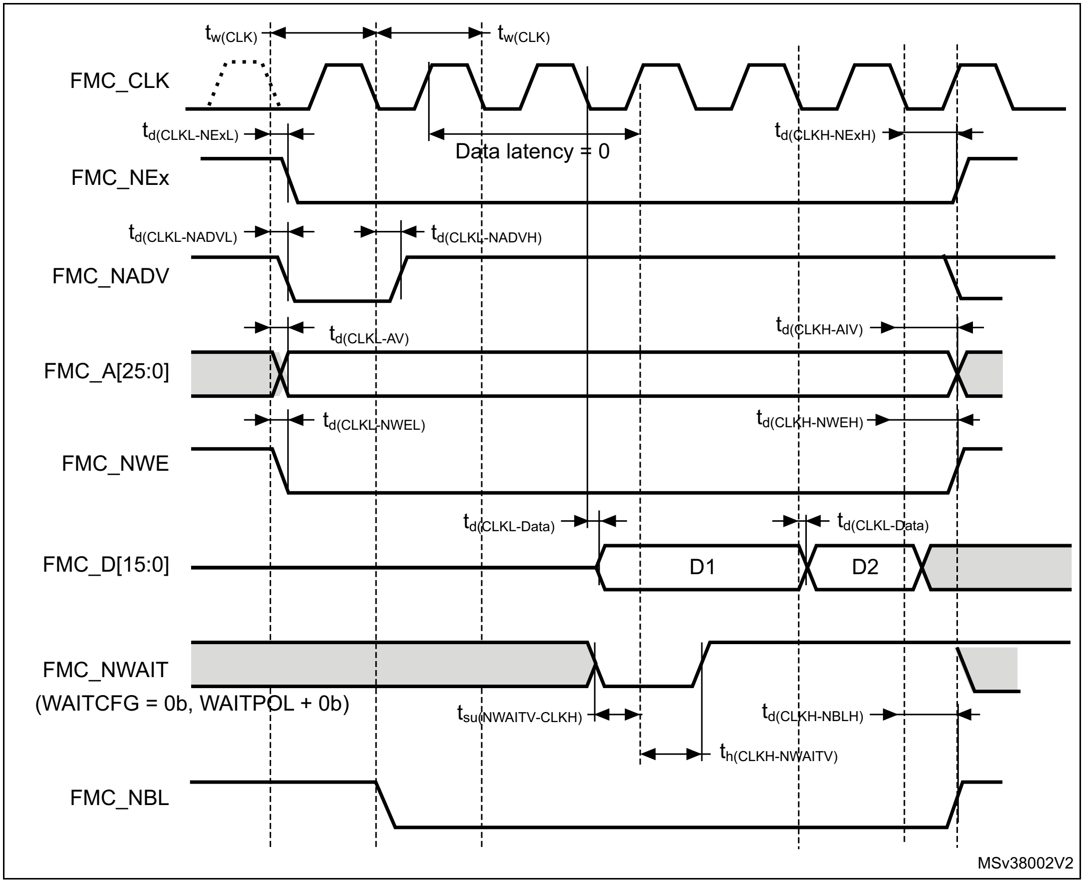


Table 108. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R*T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	3.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R*T_{HCLK}/2 + 1$	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R*T_{HCLK}/2 + 1.5$	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

Figure 47 through *Figure 50* represent synchronous waveforms, and *Table 109* and *Table 110* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 47. NAND controller waveforms for read access

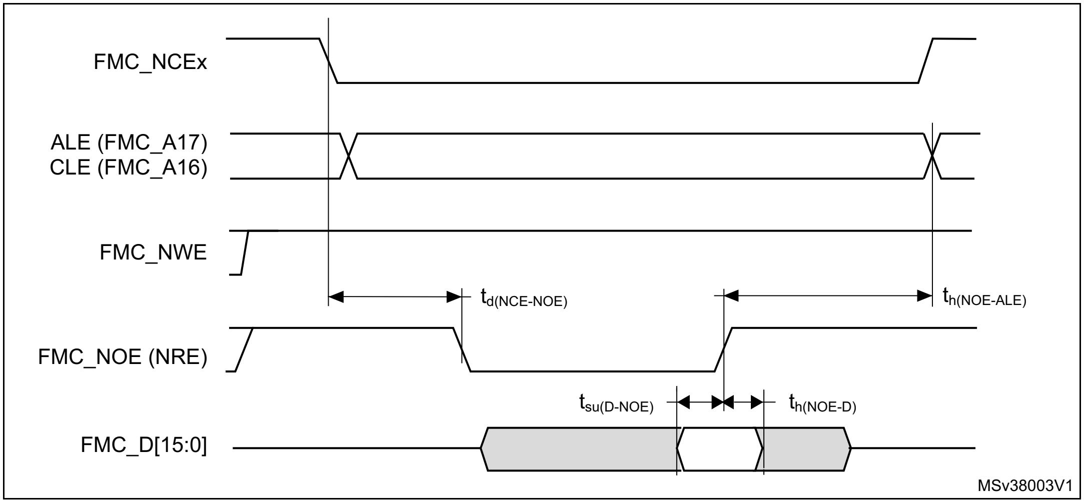


Figure 48. NAND controller waveforms for write access

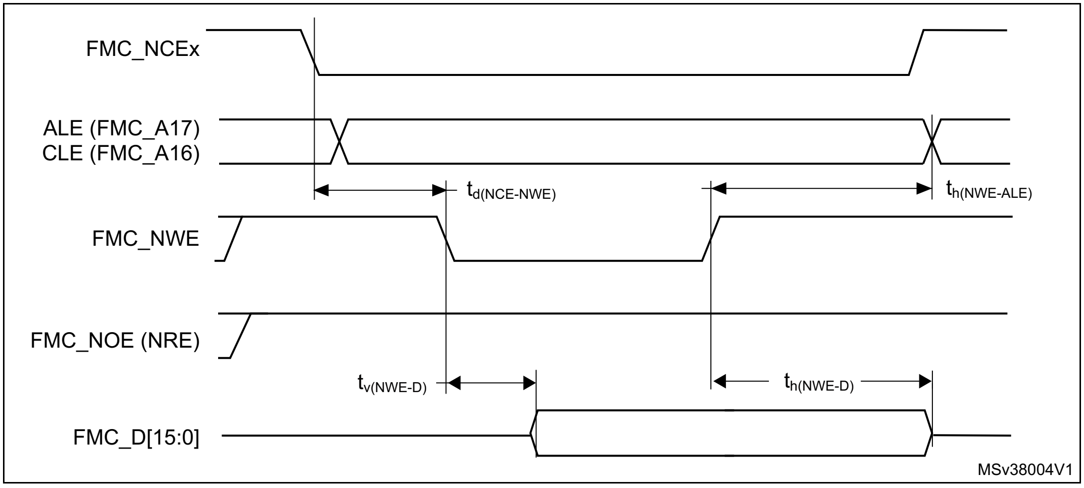


Figure 49. NAND controller waveforms for common memory read access

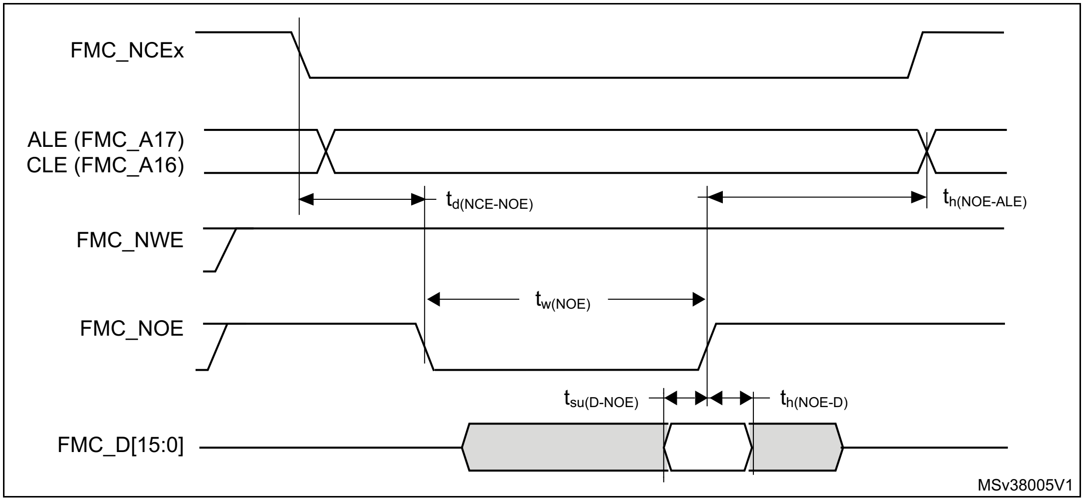


Figure 50. NAND controller waveforms for common memory write access

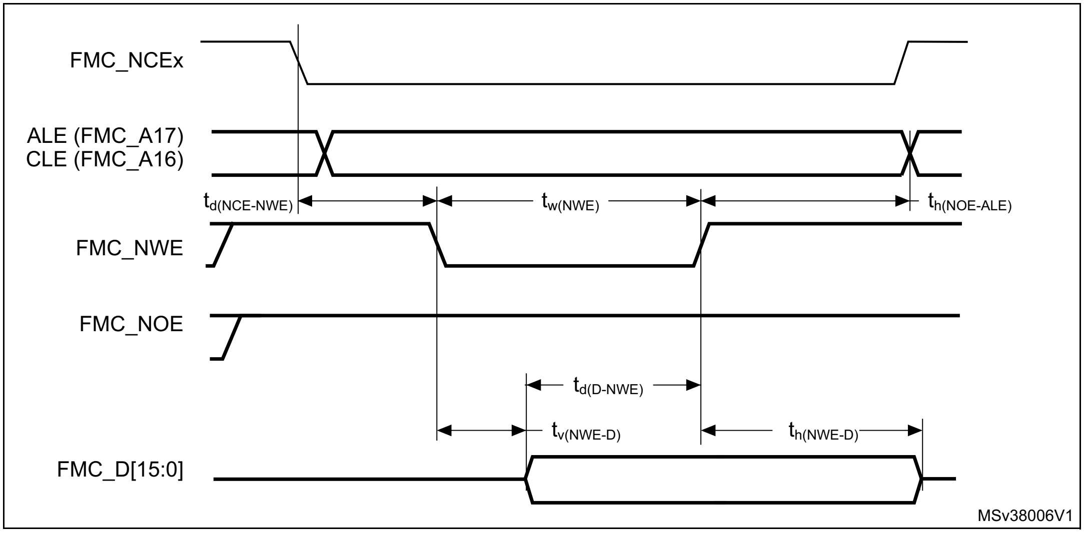


Table 109. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(N0E)}$	FMC_NOE low width	4 T_{HCLK} - 1	4 T_{HCLK}	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	19	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	3 T_{HCLK}	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	3 T_{HCLK}	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 110. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	4 T_{HCLK} -1	4 T_{HCLK}	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	3 T_{HCLK} - 1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	5 T_{HCLK}	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	3 T_{HCLK}	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	3 T_{HCLK}	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

5.3.29 QUADSPI characteristics

Unless otherwise specified, the parameters given in *Table 111* and *Table 112* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 111. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	Quad SPI clock frequency	$1.71 < V_{DD} < 3.6$ V, C_{LOAD} = 15 pF Voltage Range 1	-	-	50	MHz
		$1.71 < V_{DD} < 3.6$ V, C_{LOAD} = 20 pF Voltage Range 2	-	-	110	
$t_{w(CKH)}$	Quad SPI clock high and low time Even division	PRESCALER [7:0] n =0,1, 3, 5 ...	$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	
$t_{w(CKH)}$	Quad SPI clock high and low time Odd division	PRESCALER [7:0] n =2,4, 6, 8...	$(n/2)*t_{(CK)}/(n+1) - 0.5$	-	$(n/2)*t_{(CK)}/(n+1) + 1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/(n+1) - 1$	-	$(n/2+1)*t_{(CK)}/(n+1) +0.5$	
$t_{s(IN)}$	Data input setup time	$1.71 < V_{DD} < 3.6$ V	1	-	-	
$t_{h(IN)}$	Data input hold time	$1.71 < V_{DD} < 3.6$ V	5	-	-	
$t_{v(OUT)}$	Data output valid time	$1.71 < V_{DD} < 3.6$ V	-	1	1.5	
$t_{h(OUT)}$	Data output hold time	$1.71 < V_{DD} < 3.6$ V	0.5	-	-	

1. Guaranteed by characterization results.

Table 112. QUADSPI characteristics in DDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F(QCK)	Quad SPI clock frequency	$1.71 < V_{DD} < 3.6$ V, C_{LOAD} = 15 pF Voltage Range 1	-	-	50	MHz
		$1.71 < V_{DD} < 3.6$ V, C_{LOAD} = 20 pF Voltage Range 2	-	-	70	

Table 112. QUADSPI characteristics in DDR mode[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	Quad SPI clock high and low time Even division	PRESCALER [7:0] n =0,1, 3, 5 ...	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	Quad SPI clock high and low time Odd division	PRESCALER [7:0] n =2,4, 6, 8...	$(n/2)*t_{(CK)}/(n+1)$	-	$(n/2)*t_{(CK)}/(n+1) + 1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/(n+1) - 1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{sr(IN)}$	Data input setup time on rising edge	1.71 < V_{DD}< 3.6 V	1	-	-	
$t_{sf(IN)}$	Data input setup time on falling edge	1.71 < V_{DD}< 3.6 V	1	-	-	
$t_{hr(IN)}$	Data input hold time on rising edge	1.71 < V_{DD}< 3.6 V	6	-	-	
$t_{hf(IN)}$	Data input hold time on falling edge	1.71 < V_{DD}< 3.6 V	5	-	-	
$t_{vr(OUT)}$	Data output valid time on rising edge	1.71 < V_{DD}< 3.6 V DHHC = 0	-	7.5	8	
		1.71 < V_{DD}< 3.6 V DHHC = 1		Thclk/2 +1	Thclk/2+1.5	
$t_{vf(OUT)}$	Data output valid time	1.71 < V_{DD}< 3.6 V DHHC = 0	-	7	10	
		1.71 < V_{DD}< 3.6 V DHHC = 1		Thclk/2 +1	Thclk/2+2	
$t_{hr(OUT)}$	Data output hold time on rising edge	1.71 < V_{DD}< 3.6 V DHHC = 0	2	-	-	
		1.71 < V_{DD}< 3.6 V DHHC = 1	Thclk/2+ 0.5	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge	1.71 < V_{DD}< 3.6 V DHHC = 0	3	-	-	
		1.71 < V_{DD}< 3.6 V DHHC = 1	Thclk/2+0.5	-	-	

1. Guaranteed by characterization results.

Figure 51. Quad SPI timing diagram - SDR mode

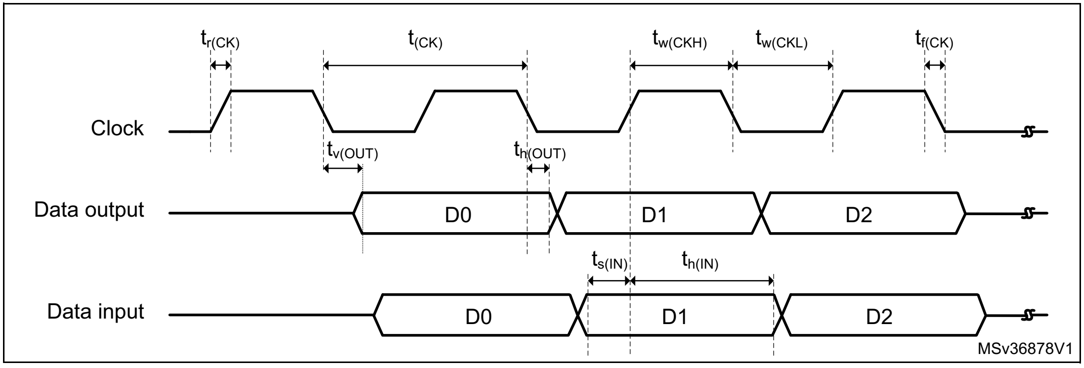
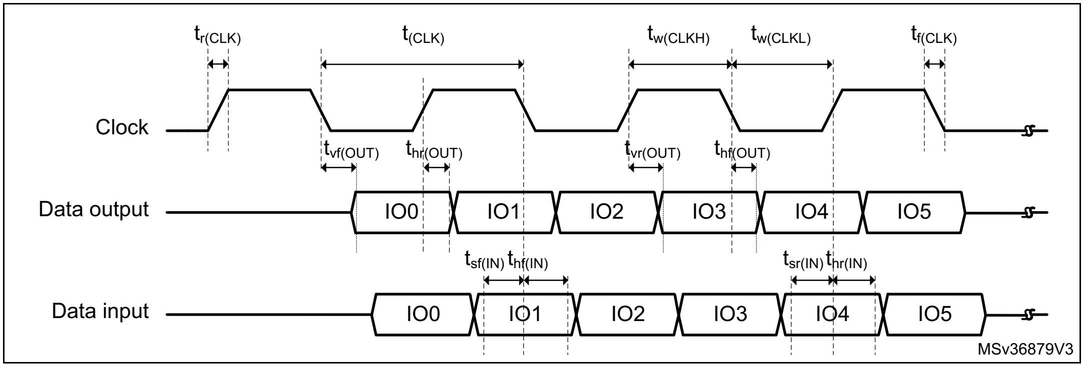


Figure 52. Quad SPI timing diagram - DDR mode



5.3.30 UCPD characteristics

UCPD1 controller complies with USB Type-C Rev.1.2 and USB Power Delivery Rev. 3.0 specifications.

Table 113. UCPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	Sink mode only	3.0	3.3	3.6	V
		Sink and source mode	3.135	3.3	3.465	V

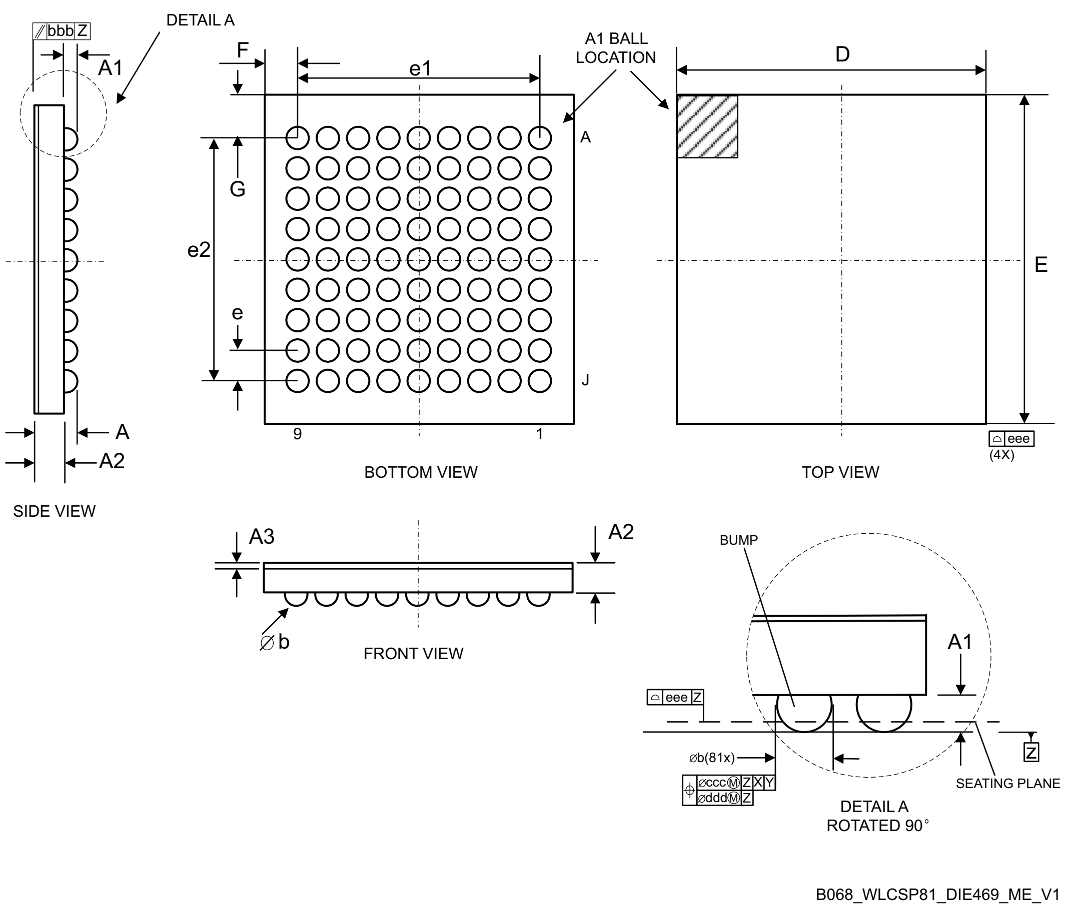
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 WLCSP81 package information

WLCSP81 is a 81-ball, 4.02x4.27 mm, 0.4 mm pitch wafer level chip scale package.

Figure 53. WLCSP81 - outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 114. WLCSP81 - mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	4.00	4.02	4.04	0.157	0.158	0.159
E	4.25	4.27	4.29	0.167	0.168	0.169
e	-	0.40	-	-	0.016	-
e1	-	3.20	-	-	0.126	-
e2	-	3.20	-	-	0.126	-
F[3]	-	0.410	-	-	0.016	-
G[3]	-	0.535	-	-	0.021	-
aaa	-	-	0.10	-	-	0.004
bbb	-	-	0.10	-	-	0.004
ccc	-	-	0.10	-	-	0.004
ddd	-	-	0.05	-	-	0.002
eee	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Calculated dimensions are rounded to the 3rd decimal place

Figure 54. WLCSP81 - recommended footprint

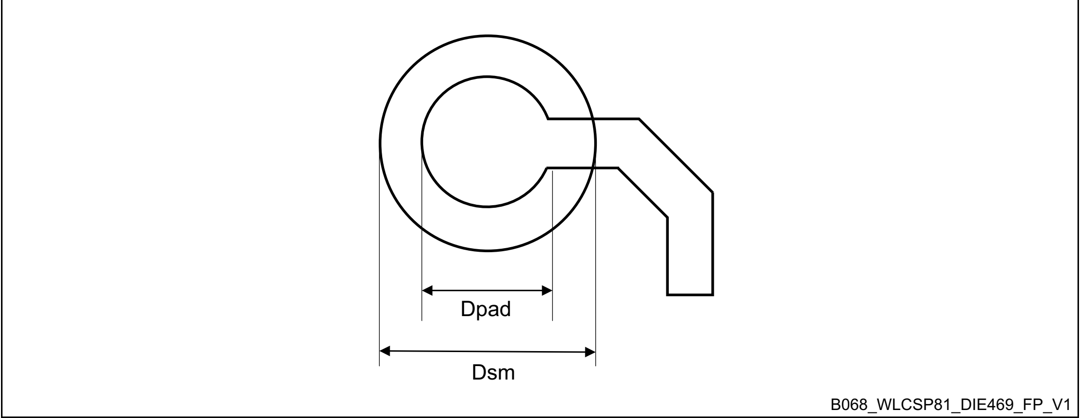


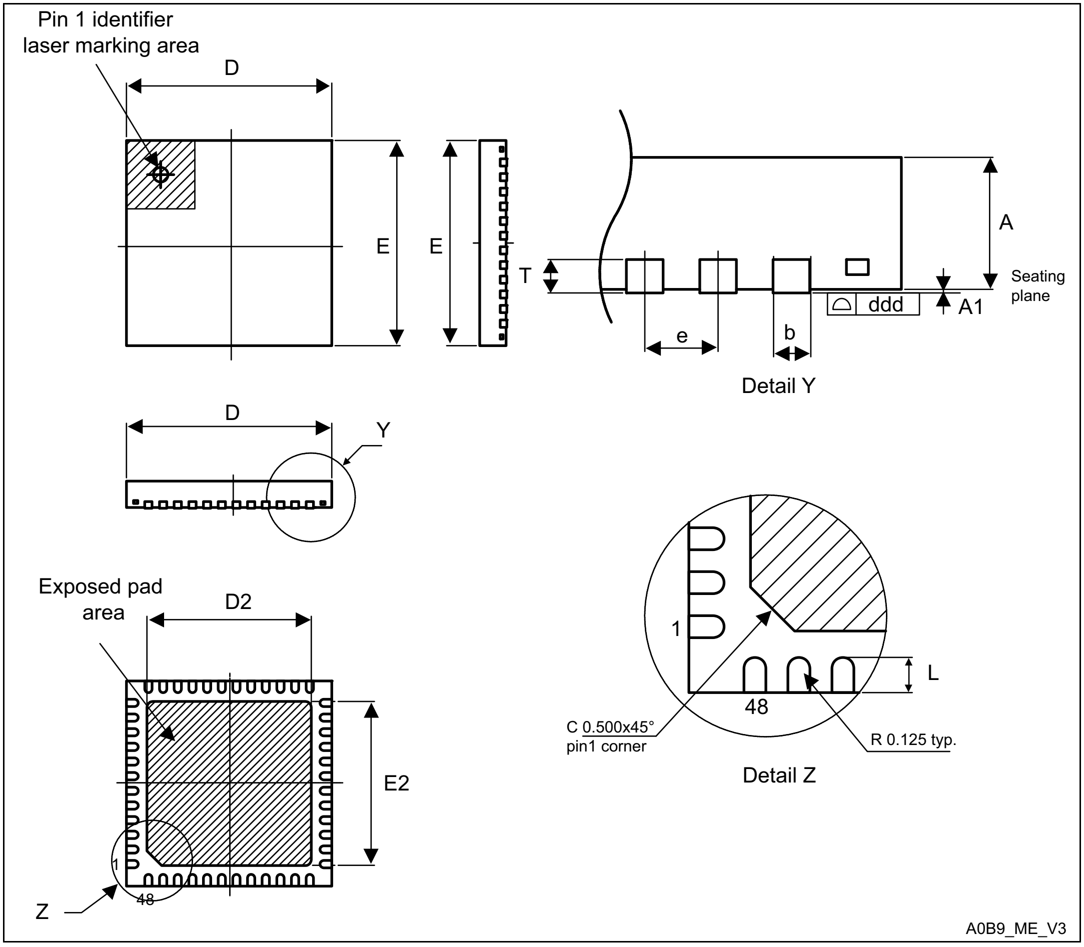
Table 115. WLCSP81 - recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

6.2 UFQFPN48 package information

UFQFPN48 is a 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 55. UFQFPN48 - outline



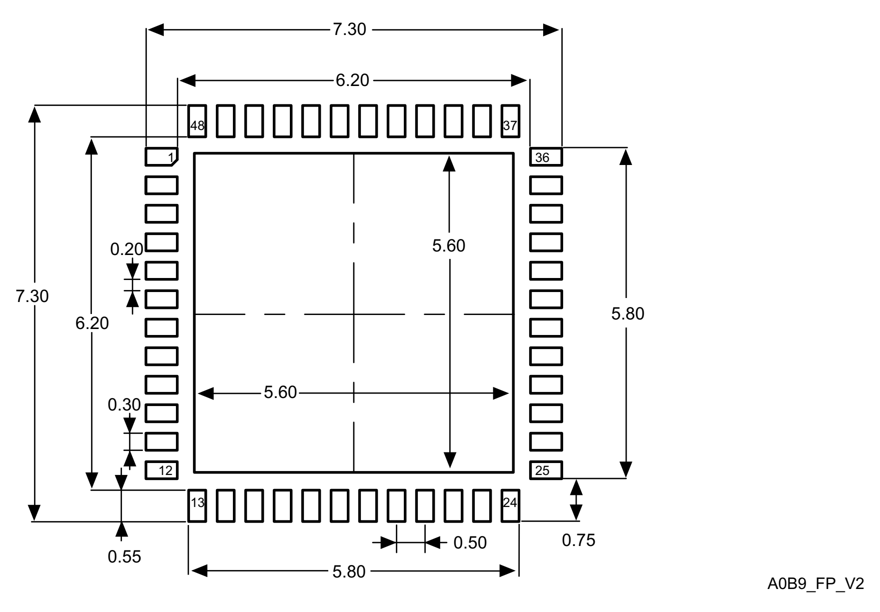
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 116. UFQFPN48 - mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 56. UFQFPN48 - recommended footprint



1. Dimensions are expressed in millimeters.

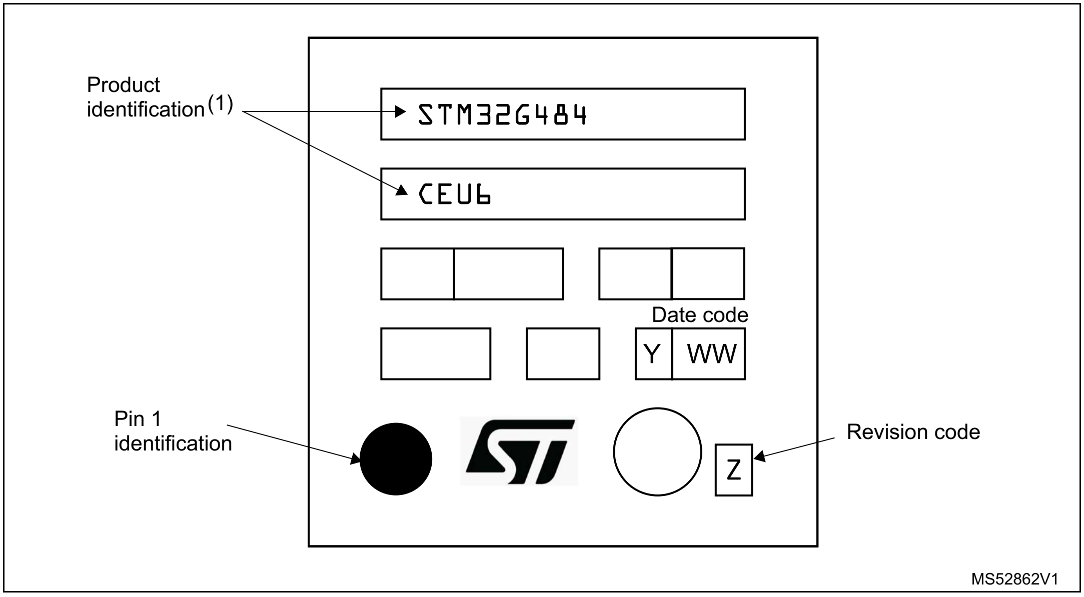
UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 57. UFQFPN48 top view example

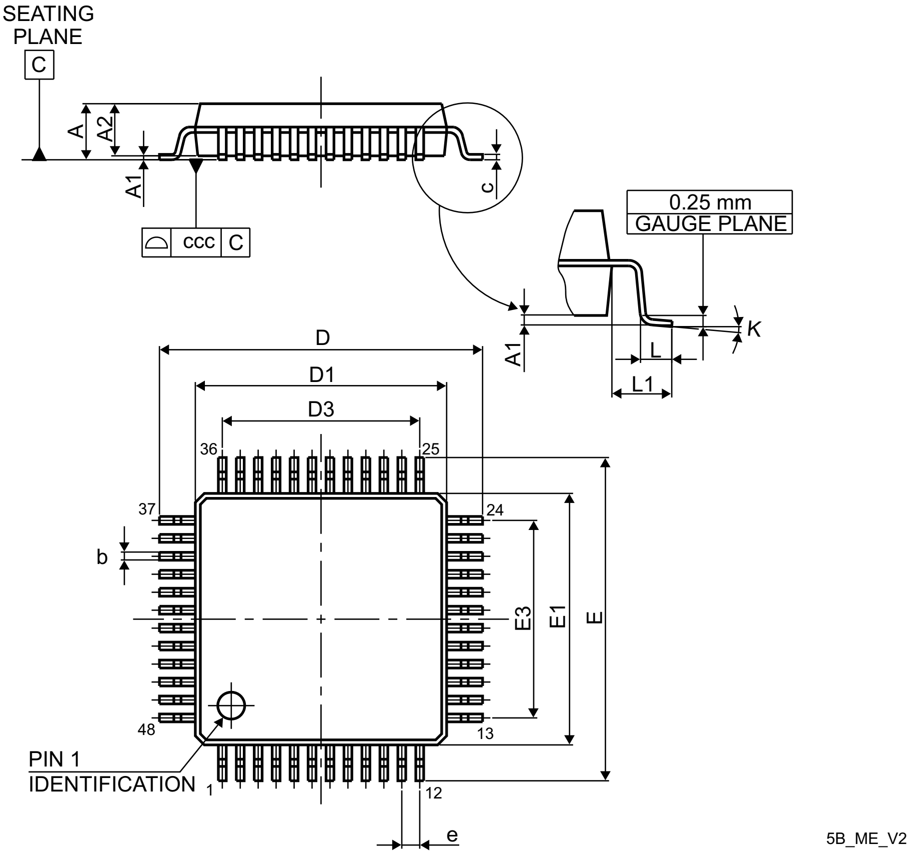


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.3 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 58. LQFP48 - outline



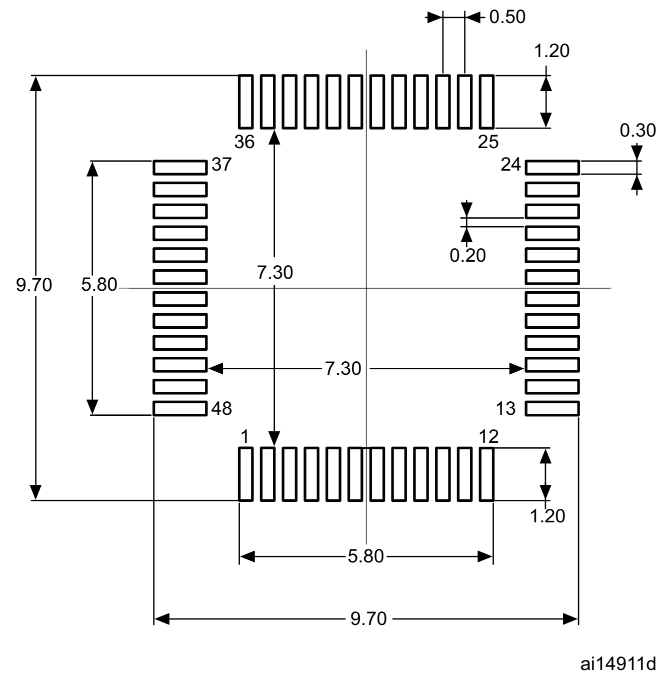
1. Drawing is not to scale.

Table 117. LQFP48 - mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 59. LQFP48 - recommended footprint



1. Dimensions are expressed in millimeters.

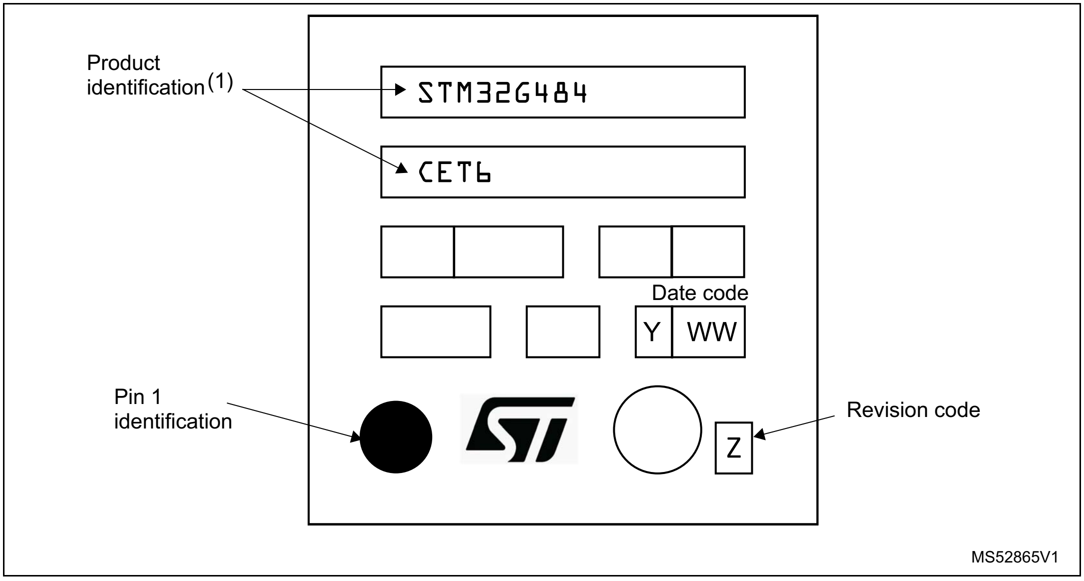
LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 60. LQFP48 top view example

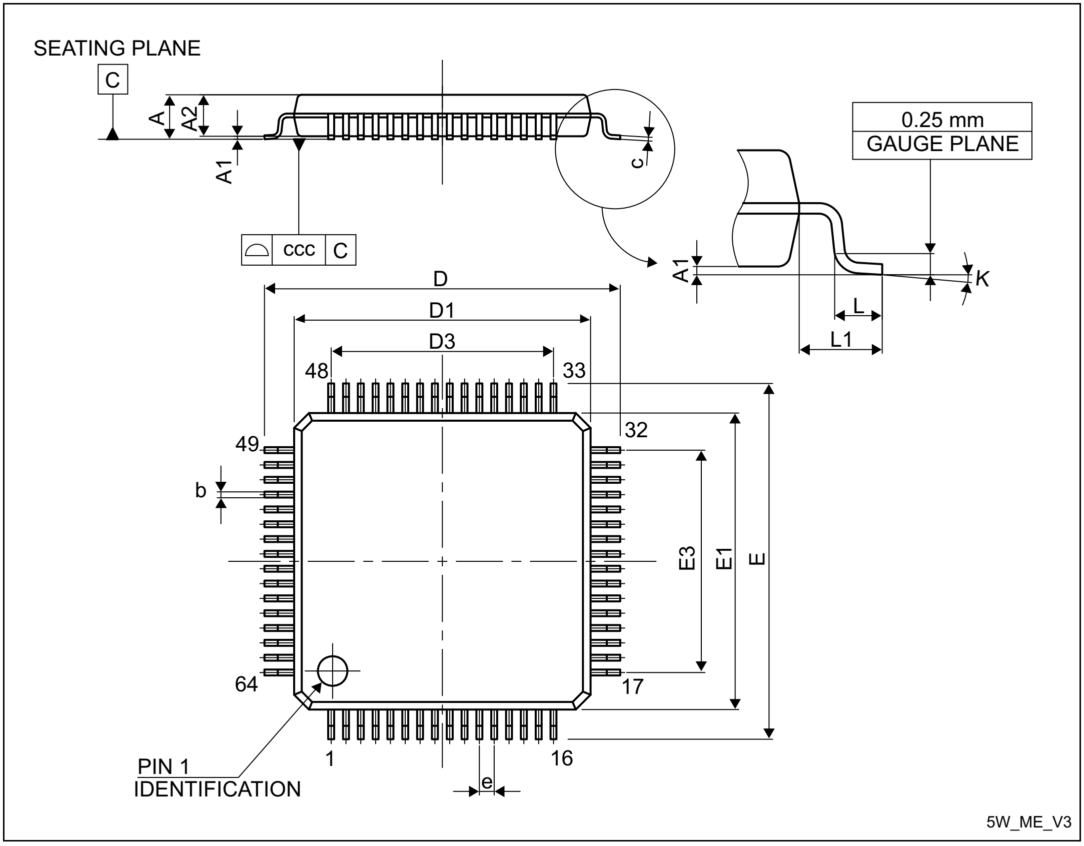


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 61. LQFP64 - outline



1. Drawing is not to scale.

Table 118. LQFP64 - mechanical data

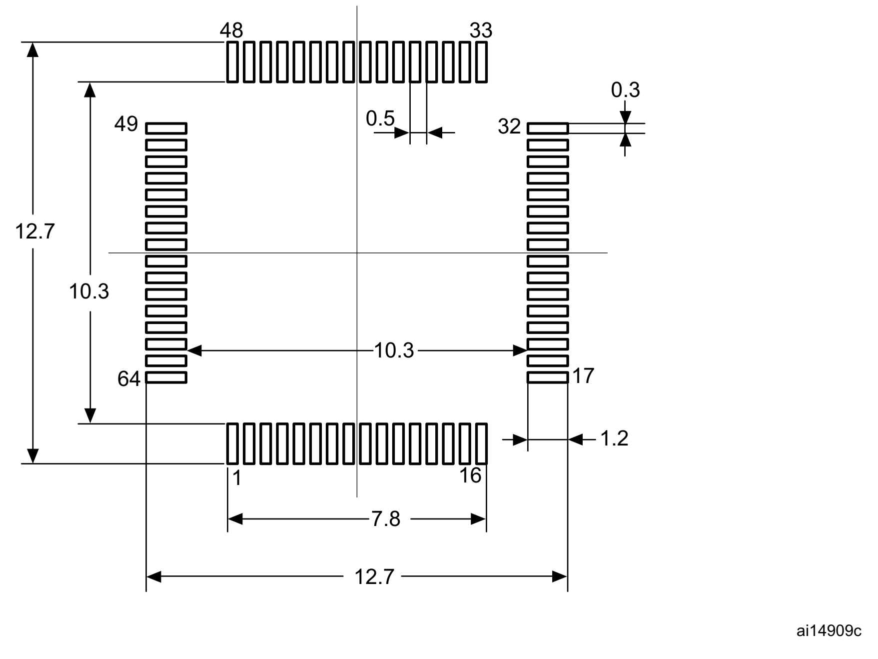
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 118. LQFP64 - mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 62. LQFP64 - recommended footprint



1. Dimensions are expressed in millimeters.

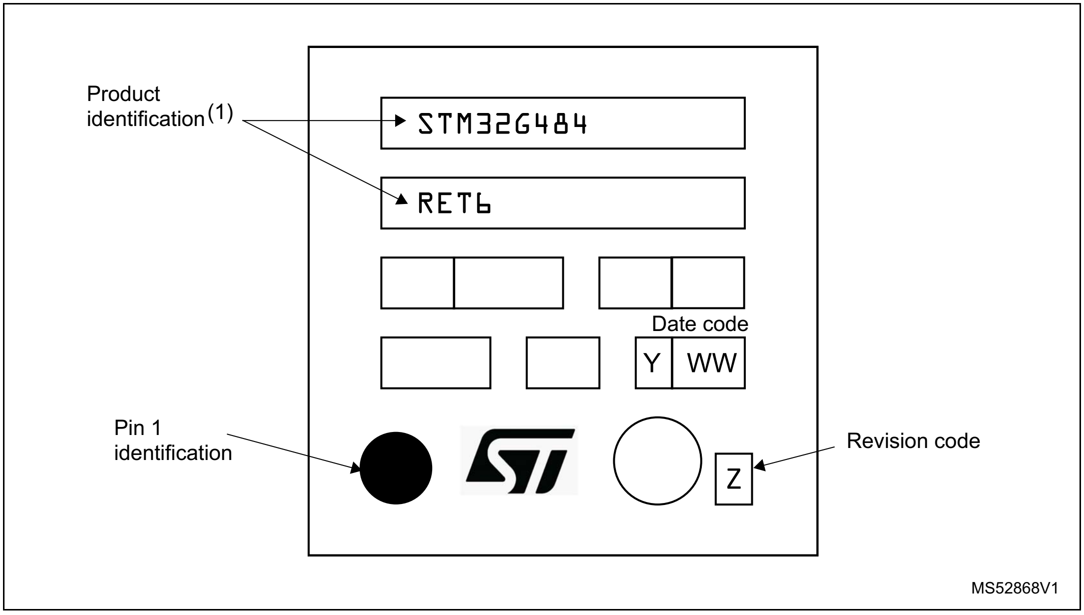
LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 63. LQFP64 top view example

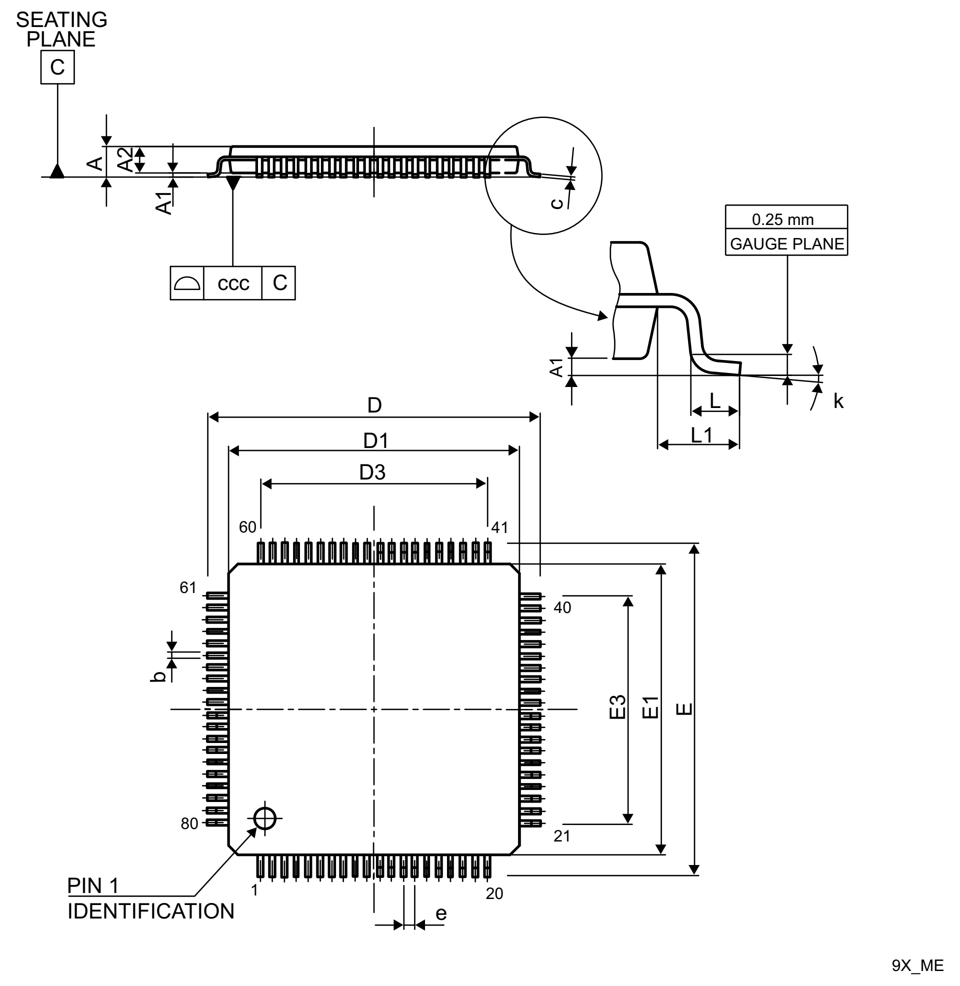


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.5 LQFP80 package information

LQFP80 is a 80-pin, 12 x 12 mm low-profile quad flat package.

Figure 64. LQFP80 - outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 119. LQFP80 - mechanical data

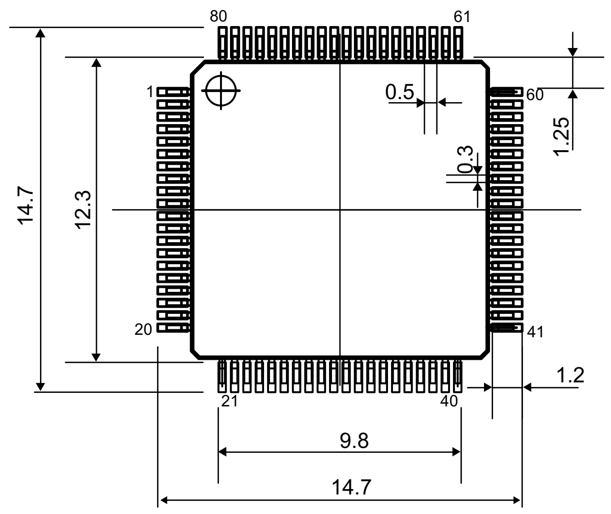
Symbol	Millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079

Table 119. LQFP80 - mechanical data (continued)

Symbol	Millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	14.000	-	-	0.5512	-
D1	-	12.000	-	-	0.4724	-
D2	-	9.500	-	-	0.3740	-
E	-	14.000	-	-	0.5512	-
E1	-	12.000	-	-	0.4724	-
E3	-	9.500	-	-	0.3740	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
k	0.0°	-	7.0°	0.0°	-	7.0°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 65. LQFP80 - recommended footprint



1. Dimensions are expressed in millimeters.

6.6 TFBGA100 package information

TFBGA is a 100-ball, 8 x 8 mm, 0.8 mm pitch fine pitch ball grid array package

Figure 66. TFBGA100 - outline

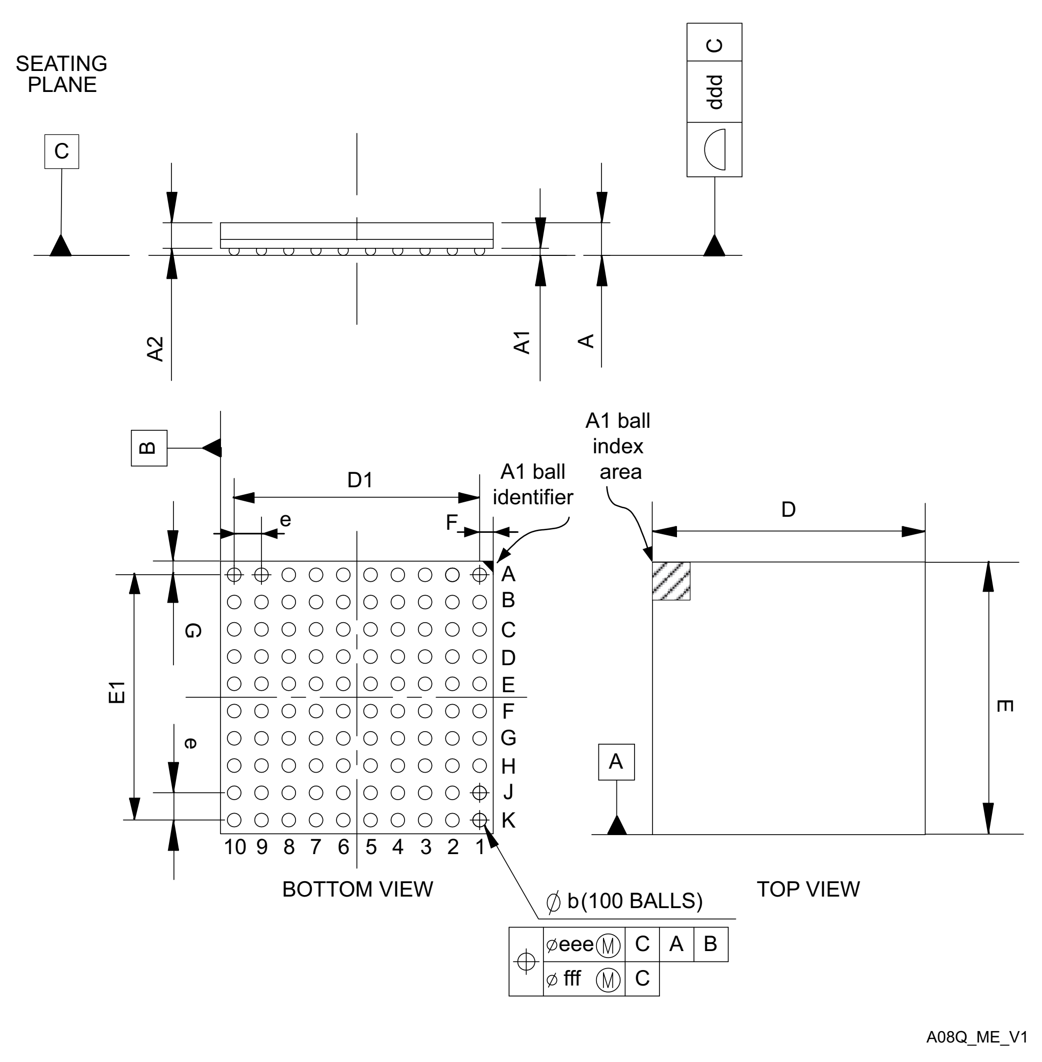


Table 120. TFBGA100 - mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	7.850	8.000	8.150	0.3091	0.3150	0.3209
D1	-	7.200	-	-	0.2835	-
E	7.850	8.000	8.150	0.3091	0.3150	0.3209
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	0.400	-	-	0.0157	-
G	-	0.400	-	-	0.0157	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. TFBGA100 - recommended footprint

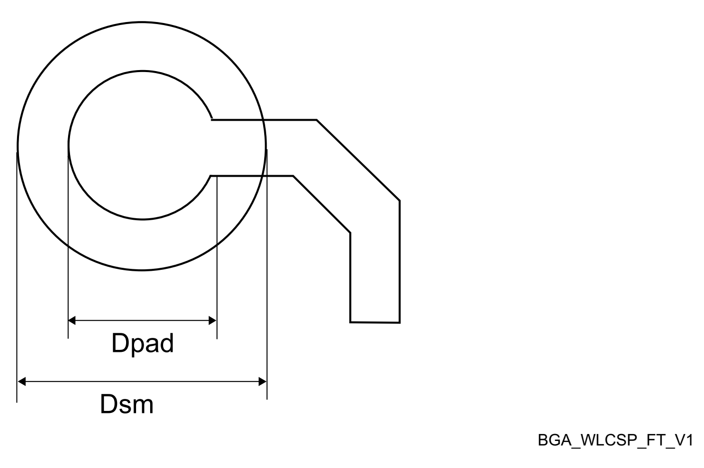


Table 121. TFBGA100 - recommended PCB design rules

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)

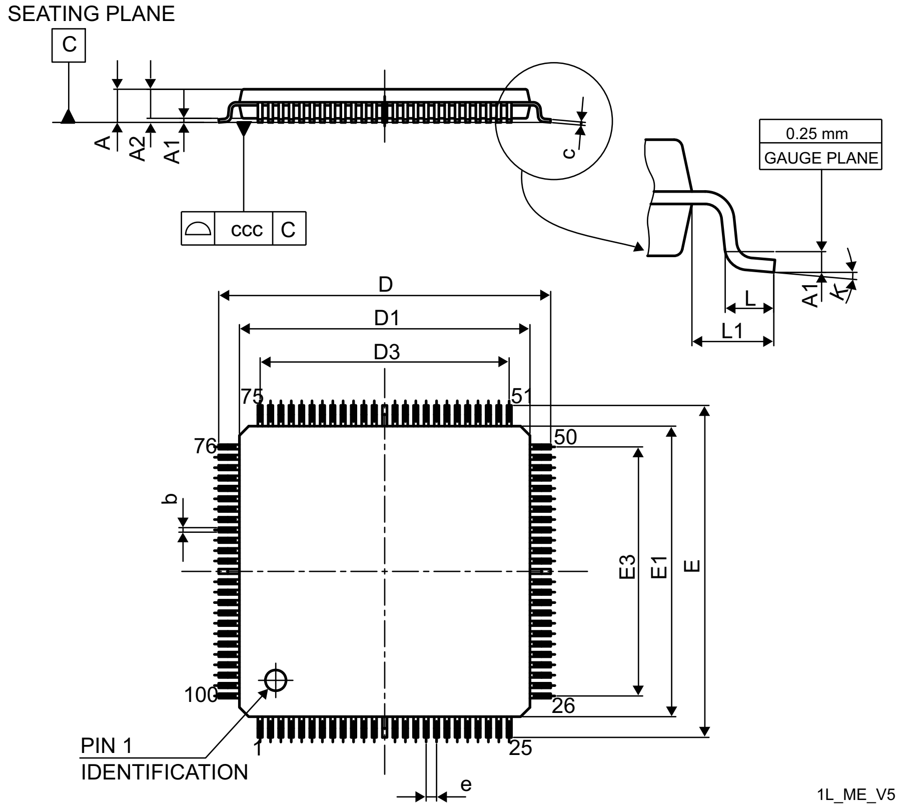
Table 121. TFBGA100 - recommended PCB design rules (continued)

Dimension	Recommended values
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

6.7 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 68. LQFP100 - outline



1. Drawing is not to scale.

Table 122. LQPF100 - mechanical data

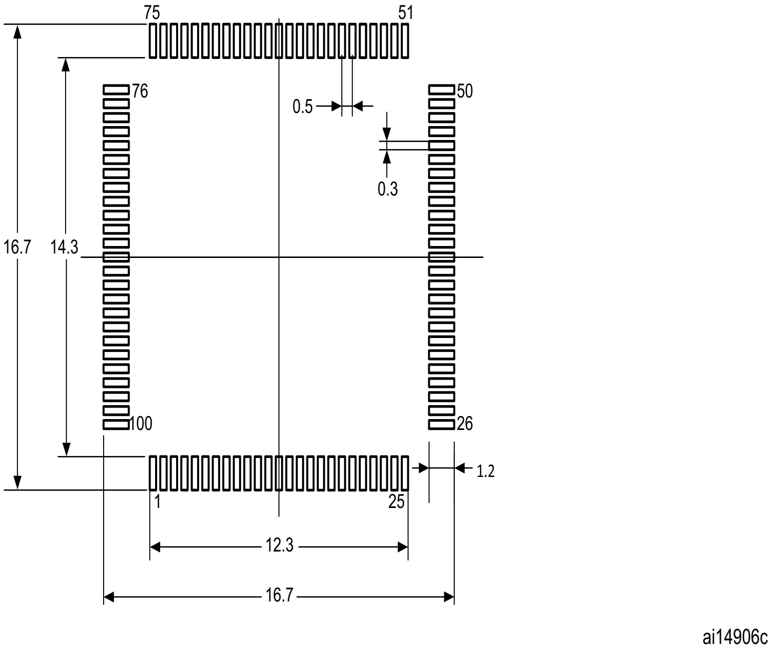
Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-

Table 122. LQPF100 - mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 69. LQFP100 - recommended footprint



1. Dimensions are expressed in millimeters.

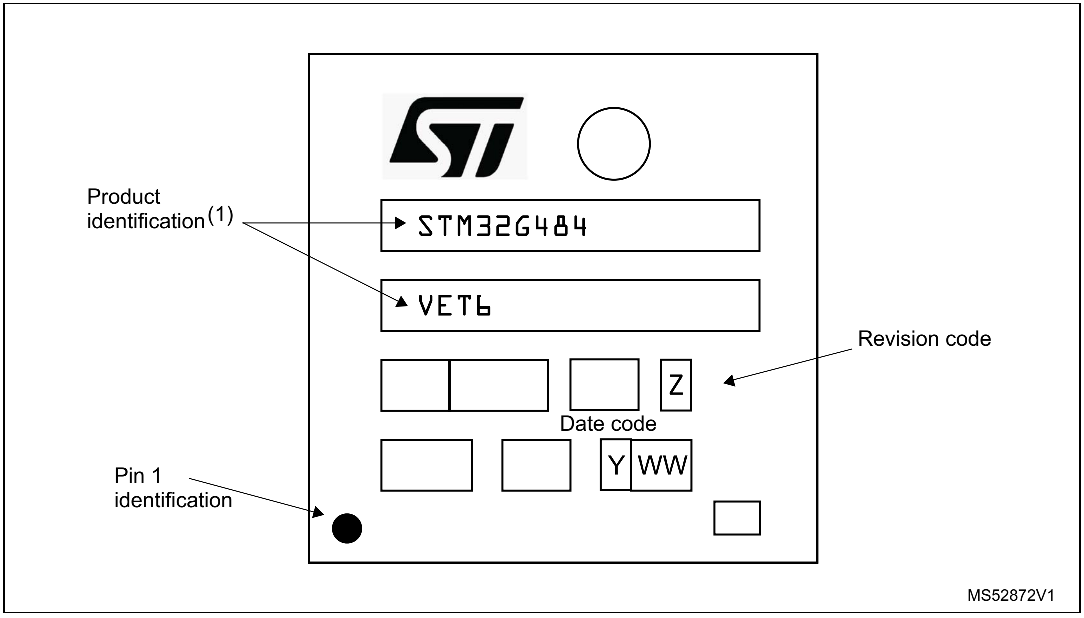
LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 70. LQFP100 top view example



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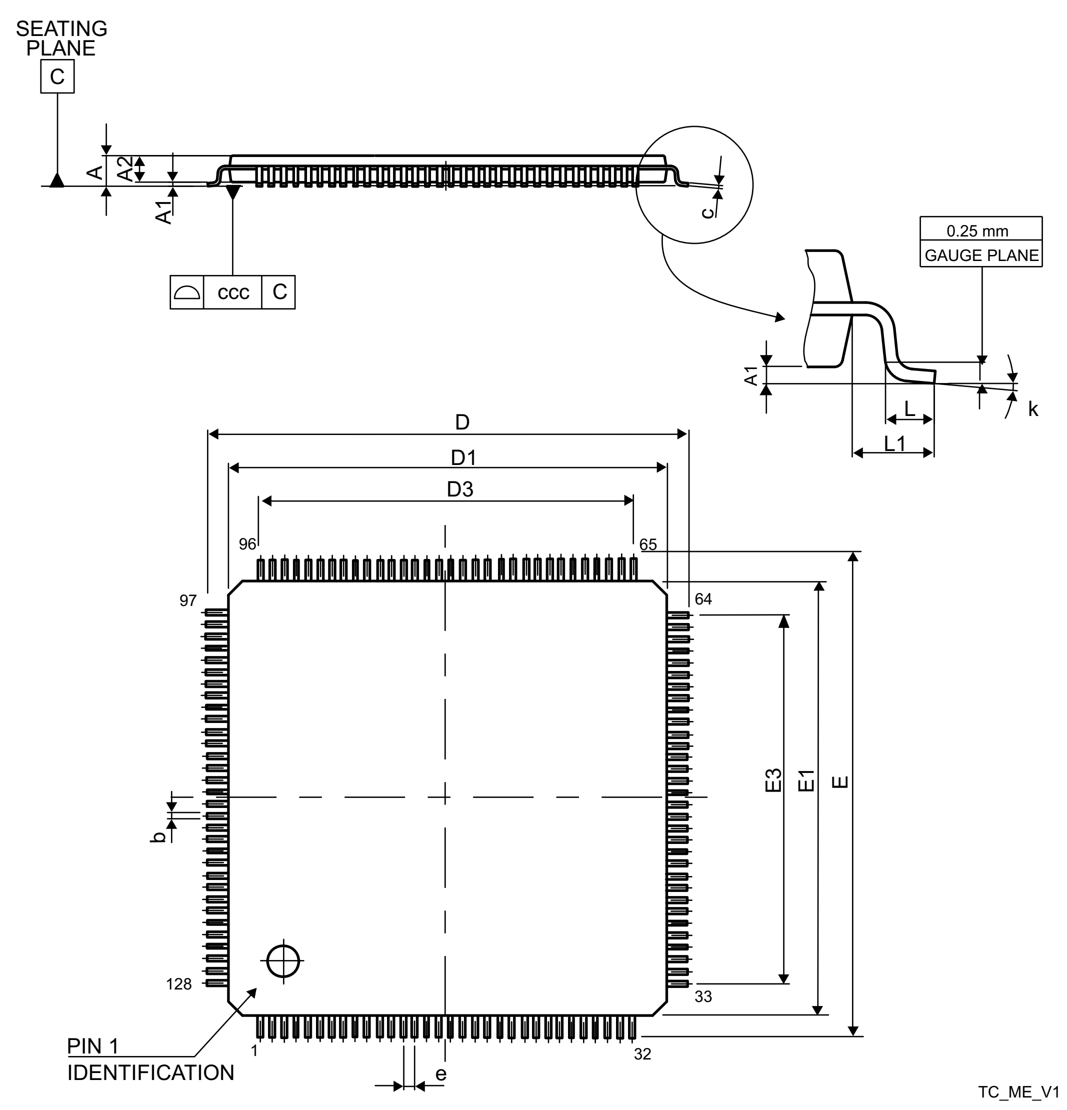
6.8 LQFP128 package information

LQFP is a 128-pin, 14 x 14 mm low-profile quad flat package

Figure 71. LQFP128 - outline



1. Drawing is not to scale.

Table 123. LQFP128 - mechanical data

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.130	0.180	0.230	0.0051	0.0071	0.0091

Table 123. LQFP128 - mechanical data (continued)

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.400	-	-	0.4882	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.400	-	-	0.4882	-
e	-	0.400	-	-	0.0157	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

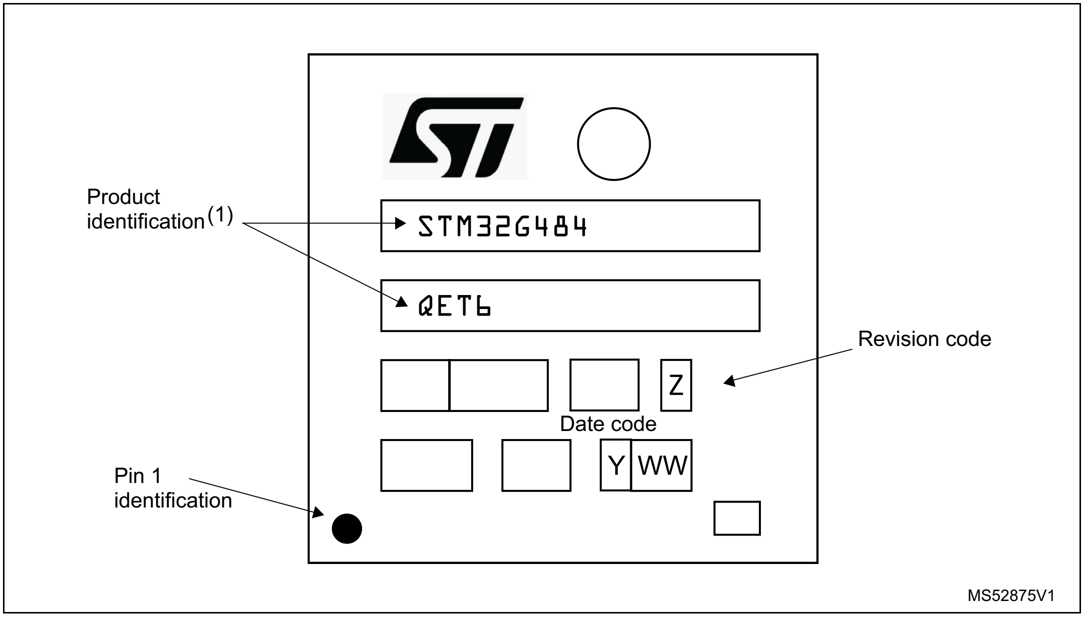
LQFP128 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 72. LQFP128 top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.9 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ ((V_{DDIOx} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 124. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP128 - 14 × 14 mm	43.0	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm	46.2	
	Thermal resistance junction-ambient LQFP80 - 12 × 12 mm	TBD	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm	47.9	
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55.2	
	Thermal resistance junction-ambient TFBGA100 - 8 × 8 mm	30.8	
	Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm	26.8	
	Thermal resistance junction-ambient WLCSP81 - 4.02 X 4.27 mm	45	

Table 124. Package thermal characteristics (continued)

Symbol	Parameter	Value	Unit
Θ_{JC}	**Thermal resistance junction-case** LQFP128 - 14 × 14 mm	7.0	°C/W
	Thermal resistance junction-case LQFP100 - 14 × 14 mm	8.3	
	Thermal resistance junction-case LQFP80 - 12 × 12 mm	TBD	
	Thermal resistance junction-case LQFP64 - 10 × 10 mm	8.0	
	Thermal resistance junction-case LQFP48 - 7 × 7 mm	9.6	
	Thermal resistance junction-case TFBGA100 - 8 × 8 mm	13	
	Thermal resistance junction-case UFQFPN48 - 7 × 7 mm	2(1) 7.5	
	Thermal resistance junction-case WLCSP81 - 4.02 X 4.27 mm	1.46	
Θ_{JB}	**Thermal resistance junction-board** LQFP128 - 14 × 14 mm	19.9	°C/W
	Thermal resistance junction-board LQFP100 - 14 × 14 mm	22.9	
	Thermal resistance junction-board LQFP80 - 12 × 12 mm	TBD	
	Thermal resistance junction-board LQFP64 - 10 × 10 mm	21.8	
	Thermal resistance junction-board LQFP48 - 7 × 7 mm	24.3	
	Thermal resistance junction-board TFBGA100 - 8 × 8 mm	13.42	
	Thermal resistance junction-board UFQFPN48 - 7 × 7 mm	11	
	Thermal resistance junction-board WLCSP81 - 4.02 X 4.27 mm	27.45	

1. Thermal resistance junction-case where the case is the bottom thermal pad on the UFQFPN package.

6.9.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

6.9.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 7: Ordering information*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32G484xE at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

$P_{INTmax} =$ 50 mA × 3.5 V= 175 mW

$P_{IOmax} =$ 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

$P_{Dmax} =$ 175 + 272 = 447 mW

Using the values obtained in T_{Jmax} is calculated as follows:

- For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 7: Ordering information*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 7: Ordering information*).

Note: With this given P_{Dmax} we can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax}$ - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 3: $T_{Amax} = T_{Jmax}$ - (42°C/W × 447 mW) = 130-18.774 = 111.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$P_{INTmax} =$ 20 mA × 3.5 V= 70 mW

$P_{IOmax} = 20$ × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

$P_{Dmax} =$ 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 3 (see *Section 7: Ordering information*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

7 Ordering information

Table 125. Ordering information

Example: STM32 G 484 V E T 6 x

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

G = General-purpose

Sub-family

484 = STM32G484xE

Pin count

C = 48 pins
R = 64 pins
M = 80 pins, 81 pins
V = 100 pins
Q = 128 pins

Code size

E = 512 Kbyte

Package

H = TFBGA
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, - 40 to 85 °C (105 °C junction)
3 = Industrial temperature range, - 40 to 125 °C (130 °C junction)

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

8 Revision history

Table 126. Document revision history

Date	Revision	Changes
08-May-2019	1	Initial release.
16-Dec-2019	2	Updated: – *Features*, *Section 2: Description*, *Section 3.6: Multi-AHB bus matrix*, *Section 3.22: Operational amplifier (OPAMP)*, *Section 3.25.2: Advanced motor control timer (TIM1, TIM8, TIM20)* – *Table 2: STM32G484xE features and peripheral counts*, *Table 7: Timer feature comparison*, *Table 38: Peripheral current consumption*,*Table 17: General operating conditions*, *Table 69: ADC characteristics*, *Table 70: Maximum ADC RAIN*, *Table 78: DAC 1MSPS accuracy*, *Table 121: TFBGA100 - recommended PCB design rules*, *Table 124: Package thermal characteristics*, *Table 125: Ordering information* – *Figure 2: Multi-AHB bus matrix* Added: – *Section 3.39: Quad SPI memory interface (QUADSPI)*, *Section 5.3.29: QUADSPI characteristics*, – *Table 74: ADC accuracy (Multiple ADCs operation) - limited test conditions 1*, *Table 75: ADC accuracy (Multiple ADCs operation) - limited test conditions 2*, *Table 76: ADC accuracy (Multiple ADCs operation) - limited test conditions 3* – *Figure 57: UFQFPN48 top view example*, *Figure 60: LQFP48 top view example*, *Figure 70: LQFP100 top view example*, *Figure 72: LQFP128 top view example*.

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