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FAIRCHILD SEMICONDUCTOR®

2013 年 10 月

FAN7390
高电流、高端与低端、栅极驱动 IC

特性

- 浮动通道可实现高达 +600V 的自举运行
- 所有通道的拉电流和灌电流驱动能力为 4.5A/4.5A
- 共模 dv/dt 噪声消除电路
- 两个通道均内置欠压闭锁功能
- 适用于两个通道的匹配传播延迟
- 逻辑地 (V_{SS}) 和功率 (COM) 接地 +/- 7V 偏压
- 兼容 3.3V 和 5V 输入逻辑
- 输出与输入同相

应用

- PDP 维持驱动
- HID 灯镇流器
- SMPS
- 电动机驱动

说明

FAN7390 是单片高端和低端栅极驱动 IC，可以驱动工作电压最高达 +600V 的高速 MOSFET 和 IGBT。它具有缓冲输出级，且所有 NMOS 晶体管设计为具有高脉冲电流驱动能力和最低交叉传导。

飞兆半导体的高压工艺和共模噪声消除技术，即使在较高 dv/dt 噪声环境中，也能够保证高端驱动器工作稳定。先进的电平转换电路，使高端栅极驱动器在电源电压为 V_{BS}=15V 时能够承受高达 V_S=-9.8V（典型值）正常工作。

UVLO 电路可防止驱动电路当 V_{DD} 和 V_{BS} 低于指定的阈值电压时发生故障。

其高电流和低输出电压跌落的特点可确保此器件适用于 PDP 维持脉冲驱动，电动机驱动，开关电源以及大功率直流转换器等应用。

8-SOP

14-SOP

Ordering Information

器件编号	封装	工作 温度范围	包装方法
FAN7390MX	8-SOP	-40°C ~ 125°C	卷带和卷盘
FAN7390M1X	14-SOP		卷带和卷盘

典型应用电路

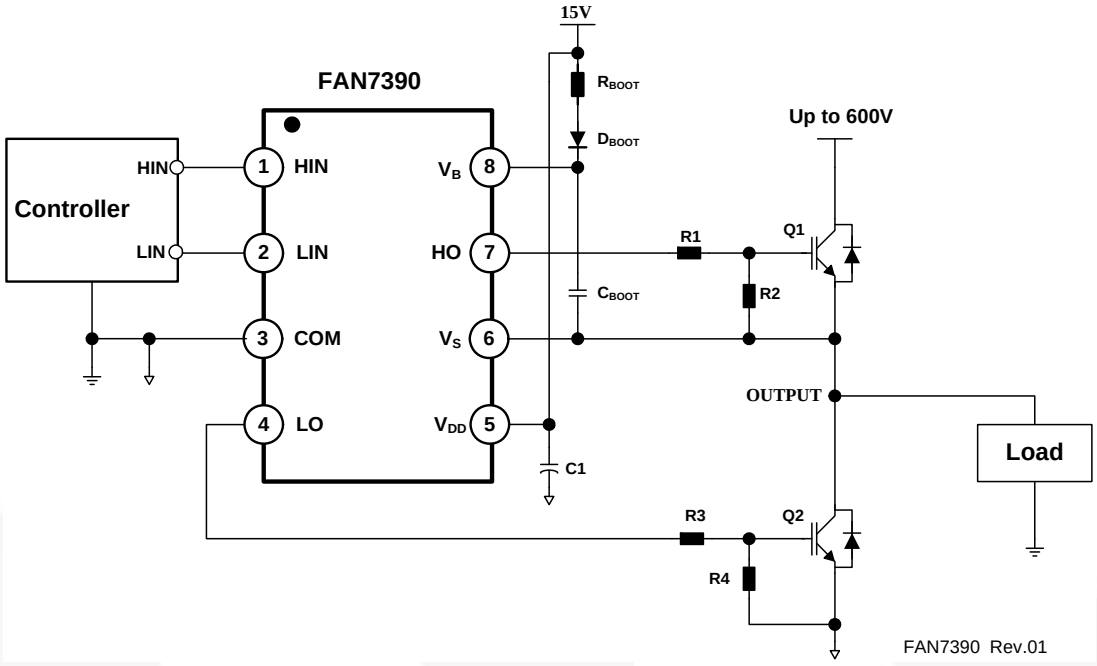

图 1. 半桥应用参考电路 （参考 8-SOP）

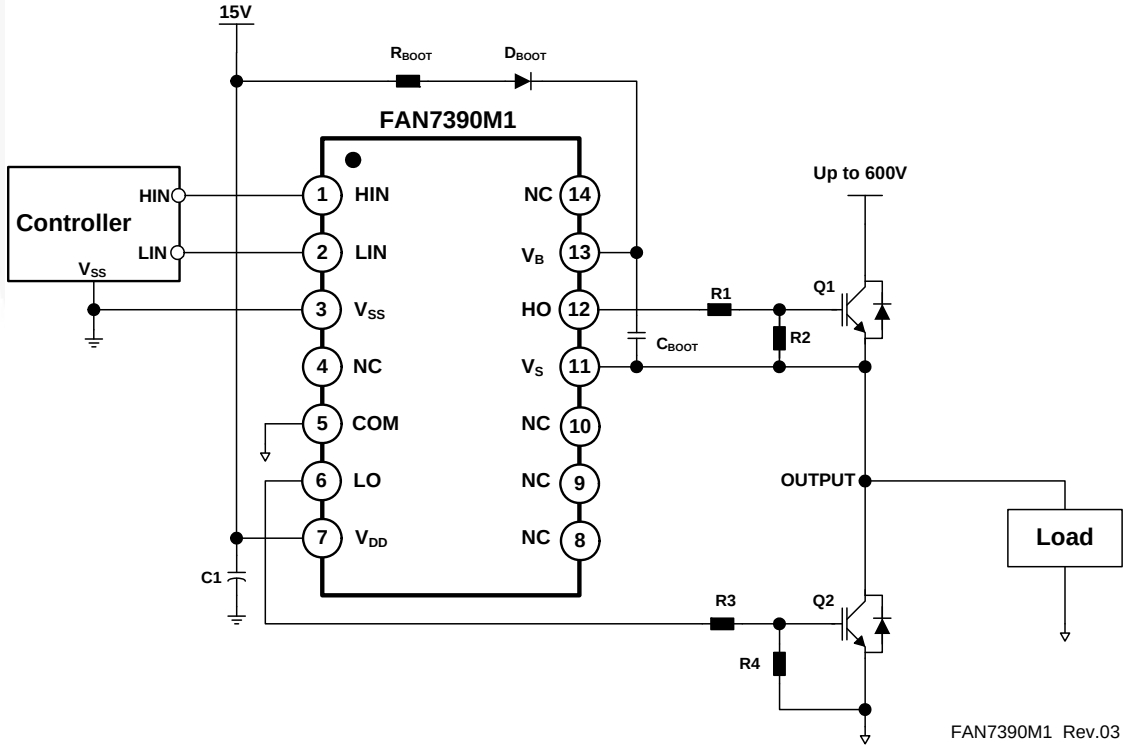

图 2. 半桥应用参考电路 （参考 14-SOP）

内部框图

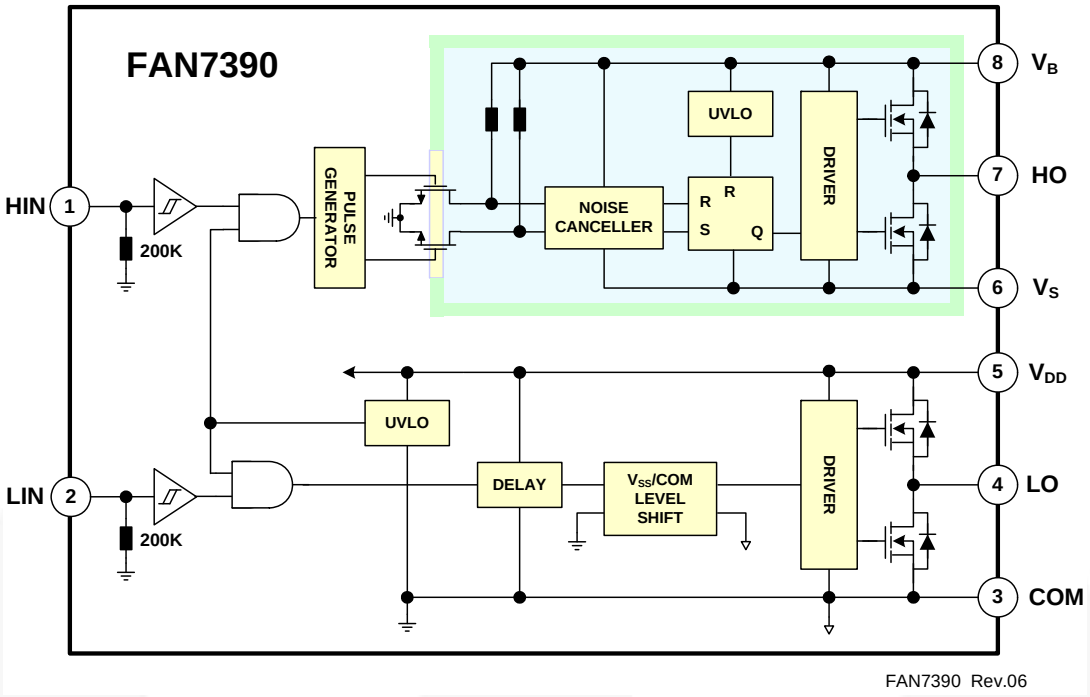

图 3. 功能模块框图 （参考 8-SOP）

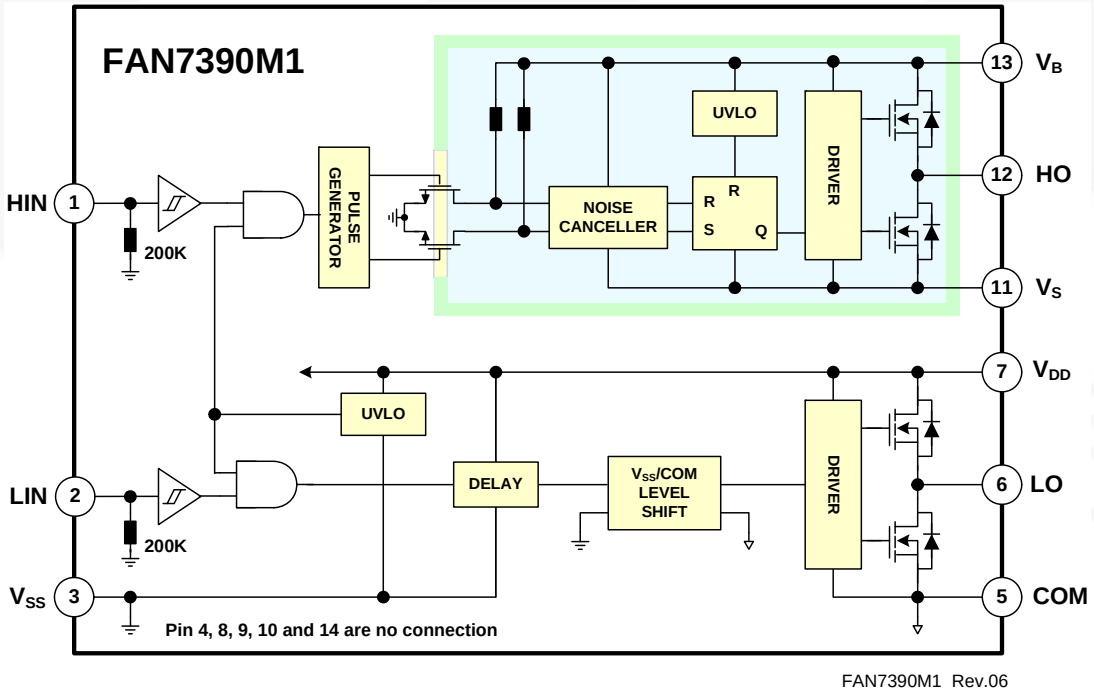

图 4. 功能模块框图 （参考 14-SOP）

引脚布局

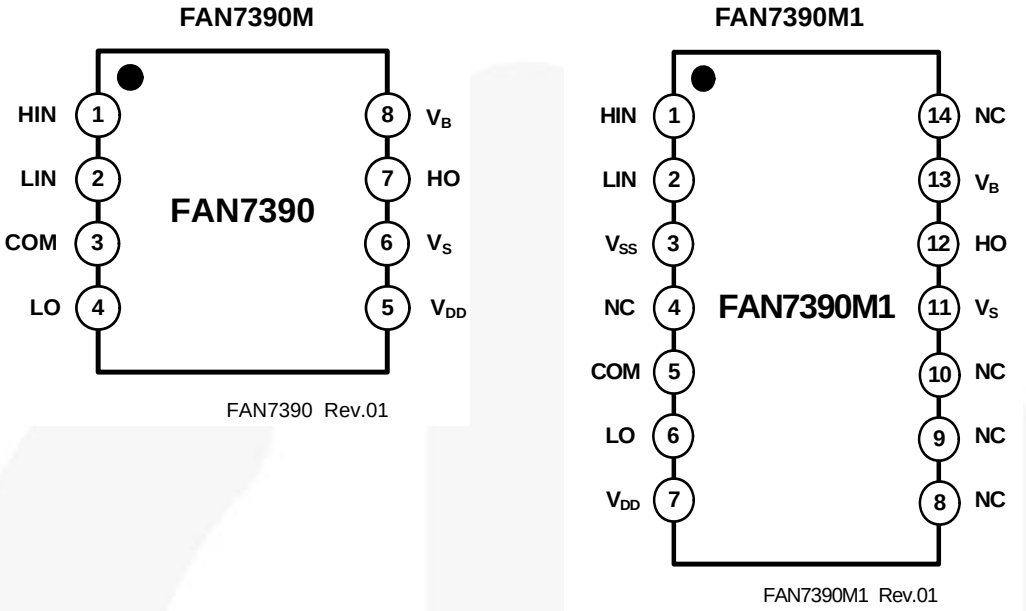

图 5. 引脚分配 （顶视图 / 俯视图）

引脚说明

8-Pin	14-Pin	名称	说明
1	1	HIN	高端栅极驱动器输出的逻辑输入
2	2	LIN	低端栅极驱动器输出的逻辑输入
	3	V_{SS}	逻辑地 （仅适用于 FAN7390M1）
3	5	COM	低端栅极返回
4	6	LO	低端栅极输出
5	7	V_{DD}	低端和逻辑电路的电源电压
6	11	V_S	高端浮动电源电压返回
7	12	HO	高端驱动输出
8	13	V_B	高端浮动电源
	4, 8, 9, 10, 14	NC	未连接

绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，过度暴露在高于推荐的工作条件下，会影响器件的可靠性。绝对最大额定值仅是应力规格值。除非另有说明， T_A=25°C。

符号	特性	最小值	最大值	单位
V_S	高端浮动电源偏置电压	V_B-25	V_B+0.3	V
V_B	高端浮动电源电压	-0.3	625.0	V
V_{HO}	高端浮动输出电压 HO	V_S-0.3	V_B+0.3	V
V_{DD}	低端和固定逻辑电源电压	-0.3	25.0	V
V_{LO}	低端输出电压 LO	-0.3	V_{DD}+0.3	V
V_{IN}	逻辑输入电压 (HIN, LIN)	V_{SS}-0.3	V_{DD}+0.3	V
V_{SS}	逻辑地 （仅适用于 FAN7390M1）	V_{DD}-25	V_{DD}+0.3	V
dV_S/dt	允许的偏置电压转换速率		50	V/ns
P_D[(1)(2)(3)]	功耗	8-SOP	0.625	W
		14-SOP	1.000	
θ_{JA}	结至环境热阻	8-SOP	200	°C/W
		14-SOP	110	
T_J	结温		+150	°C
T_{STG}	存储温度		+150	°C

注意：

1. 安装到 76.2 x 114.3 x 1.6mm PCB 板 (FR-4 环氧玻璃材料)。
2. 参考以下标准：
   JESD51-2: 集成电路热测试方法环境条件 - 自然对流
   JESD51-3: 含铅表面贴装封装的低有效导热系数测试板
3. 在任何情况下，都不要超过 P_D。

推荐工作条件

推荐的操作条件表定义了器件的真实工作条件。指定推荐的工作条件，以确保器件的最佳性能达到数据表中的规格。飞兆不建议超出额定或依照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
V_B	高端浮动电源电压	V_S+10	V_S+22	V
V_S	高端浮动电源偏置电压	6-V_{DD}	600	V
V_{HO}	高端输出电压	V_S	V_B	V
V_{DD}	低端和逻辑电源电压	10	22	V
V_{LO}	低端输出电压	COM	V_{DD}	V
V_{IN}	逻辑输入电压 (HIN, LIN)	V_{SS}	V_{DD}	V
T_A	操作环境温度	-40	+125	°C

电气特性

V_{BIAS} (V_{DD}，V_{BS})=15.0V，V_S=V_{SS}=COM，T_A=25×C，除非另有说明 V_{IL}、V_{IH} 和 I_{IN} 参数以 V_{SS}/COM 作为基准，适用于各自的输入信号 HIN 和 LIN。 V_O 和 I_O 参数以 COM 和 V_S 作为基准，适用于各自的输出信号 HO 和 LO。

符号	特性	测试条件	最小值	典型值	最大值	单位
电源部分 （V_{DD} 和 V_{BS}）						
V_{DDUV+} V_{BSUV+}	V_{DD} 和 V_{BS} 电源欠压正向阈值		8.0	8.8	9.8	V
V_{DDUV-} V_{BSUV-}	V_{DD} 和 V_{BS} 电源欠压负向阈值		7.4	8.3	9.0	
V_{DDUVH} V_{BSUVH}	V_{DD} 和 V_{BS} 电源欠压锁定滞洄电压			0.5		
I_{LK}	偏置漏电流	V_B=V_S=600V			50	µA
I_{QBS}	V_{BS} 静态电源电流	V_{IN}=0V 或 5V		45	80	
I_{QDD}	V_{DD} 电源静态电流	V_{IN}=0V 或 5V		75	110	
I_{PBS}	V_{BS} 电源静态电流	f_{IN}=20kHz， rms 值		530	640	µA
I_{PDD}	V_{DD} 电源工作电流	f_{IN}=20kHz， rms 值		530	640	
逻辑输入部分 (HIN, LIN)						
V_{IH}	逻辑 "1" 输入电压		2.5			V
V_{IL}	逻辑 "0" 输入电压				1.2	
I_{IN+}	逻辑 "1" 输入偏置电流	V_{IN}=5V		25	50	µA
I_{IN-}	逻辑 "0" 输入偏置电流	V_{IN}=0V		1.0	2.0	
R_{IN}	输入下拉电阻		100	200		KΩ
栅极驱动器输出部分 （HO, LO）						
V_{OH}	高电平输出电压， V_{BIAS}-V_O	无负载			1.0	V
V_{OL}	低电平输出电压， V_O	无负载			35	mV
I_{O+}	输出高电平短路脉冲电流 (4)	V_O=0V, V_{IN}=5V with PW<10µs	3.5	4.5		A
I_{O-}	输出低电平短路脉冲电流 (4)	V_O=15V, V_{IN}=0V with PW<10µs	3.5	4.5		
V_S	当 HIN 信号传输至 HO 时，容许 V_S 引脚负电压			-9.8	-7.0	V
V_{SS}-COM	V_{SS}-COM/COM-V_{SS} 电压持久性		-7.0		7.0	V

注意：

4. 参数由设计者提供。

动态电气特性

V_{BIAS} (V_{DD}， V_{BS})=15.0V， V_S=V_{SS}=COM=0V， C_L=1000pF 且 T_A=25×C，除非另有说明。

符号	特性	测试条件	最小值	典型值	最大值	单位
t_{on}	导通传输延时	V_S=0V		140	200	ns
t_{off}	关断传输延时	V_S=0V		140	200	
MT	延时匹配， HS 与 LS 导通 / 关断			0	50	
t_r	导通上升时间			25	50	
t_f	关断下降时间			20	45	

典型特性

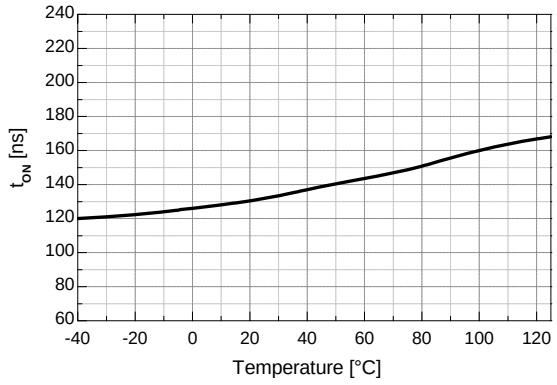

图 6. 开通传输延时与温度的关系

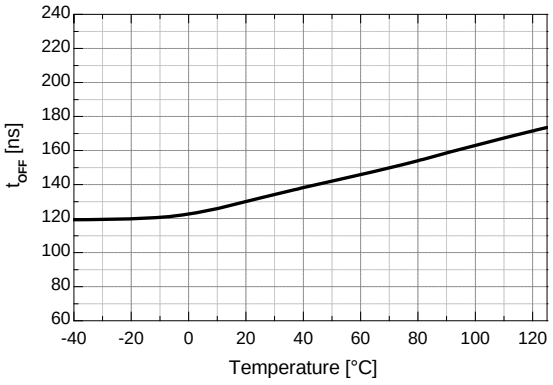

图 7. 关断传输延时与温度的关系

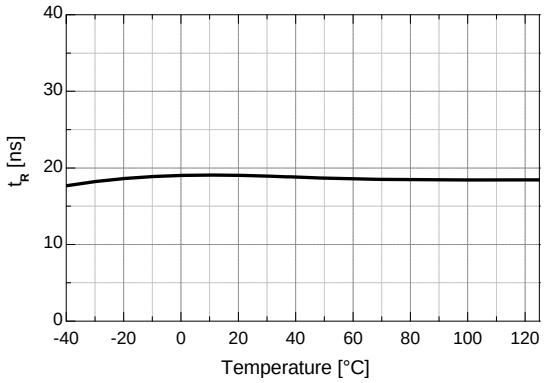

图 8. 导通上升时间与温度的关系

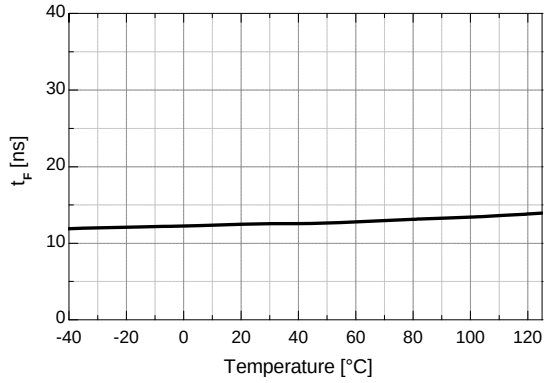

图 9. 导通下降时间与温度的关系

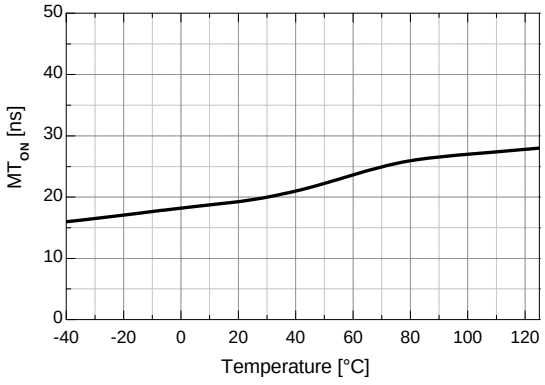

图 10. 导通延时匹配与温度的关系

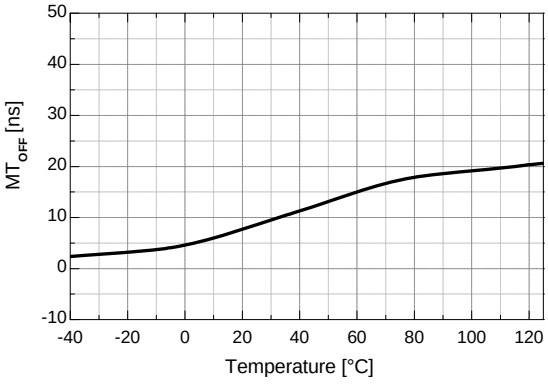

图 11. 关断延时匹配与温度的关系

典型特性 （续）

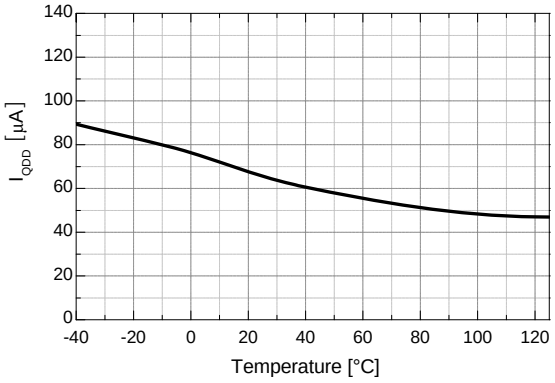

图 12. 静态 V_{DD} 电源电流与温度的关系

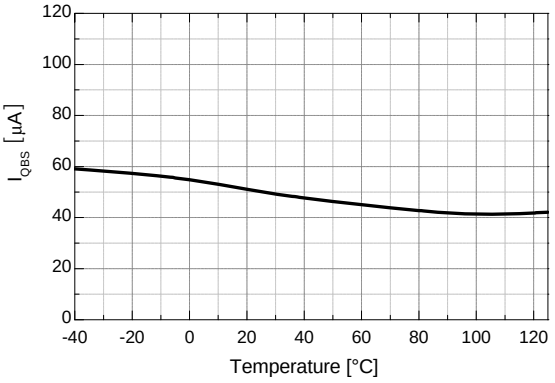

图 13. 静态 V_{BS} 电源电流与温度的关系

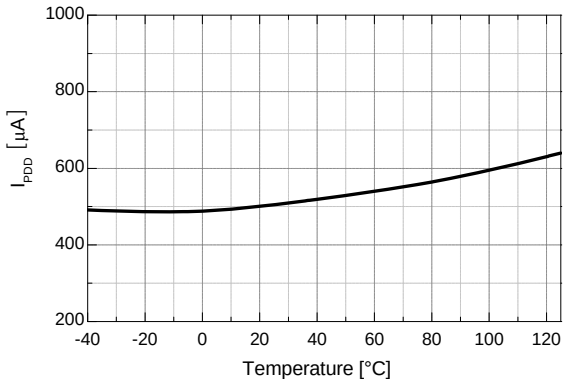

图 14. 工作时 V_{DD} 电源电流与温度的关系

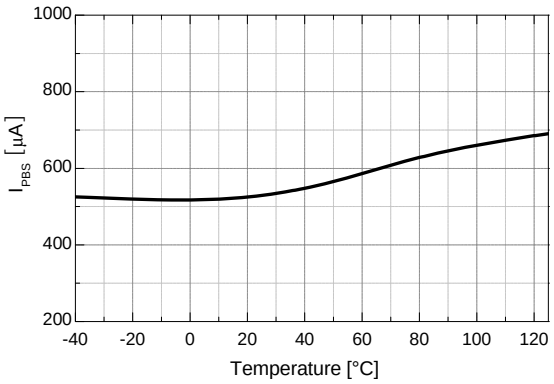

图 15. 工作时 V_{BS} 电源电流与温度的关系

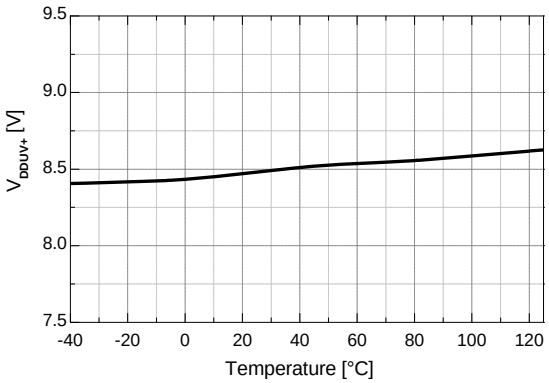

图 16. V_{DD} UVLO+ 与温度的关系

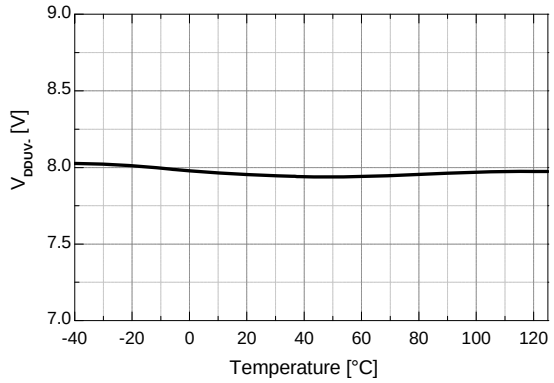

图 17. V_{DD} UVLO- 与温度的关系

典型特性（续）

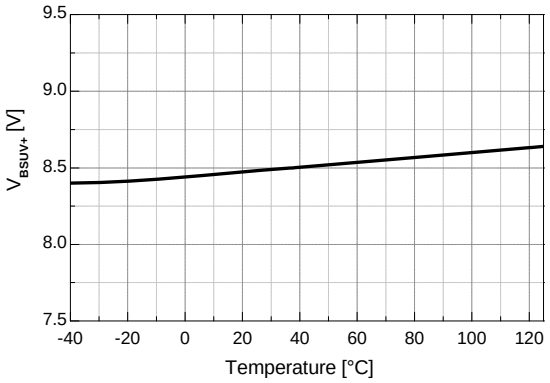

图 18. V_{BS} UVLO+ 与温度的关系

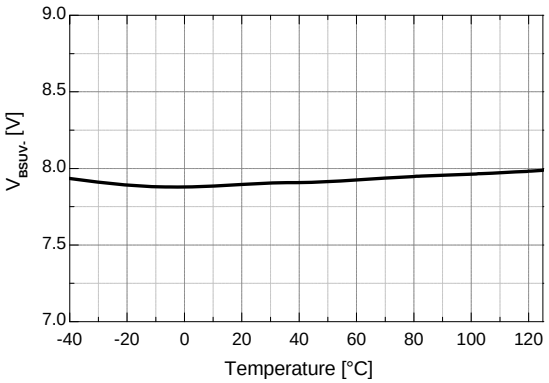

图 19. V_{BS} UVLO- 与温度的关系

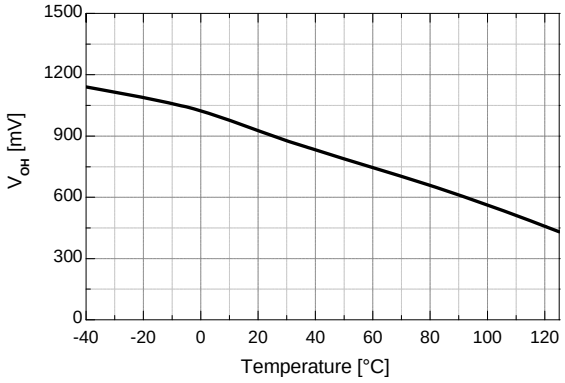

图 20. 高电平输出电压与温度的关系

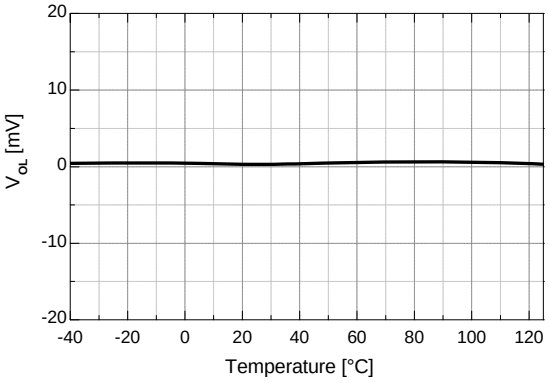

图 21. 低电平输出电压与温度的关系

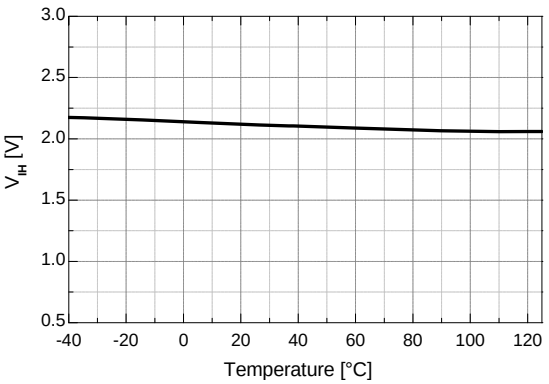

图 22. 逻辑高输入电压与温度的关系

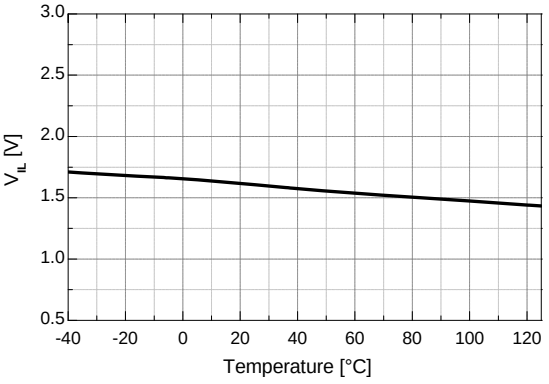

图 23. 低输入电压与温度的关系

典型特性（续）

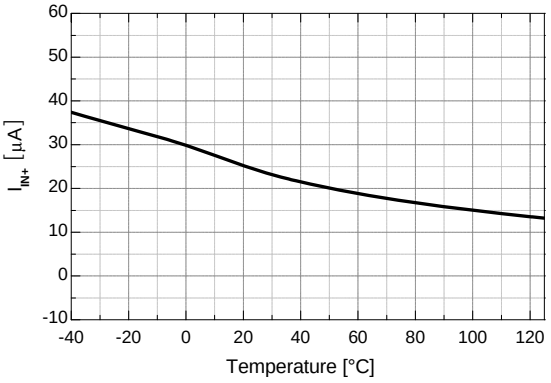

图 24. 逻辑输入高偏置电流与温度的关系

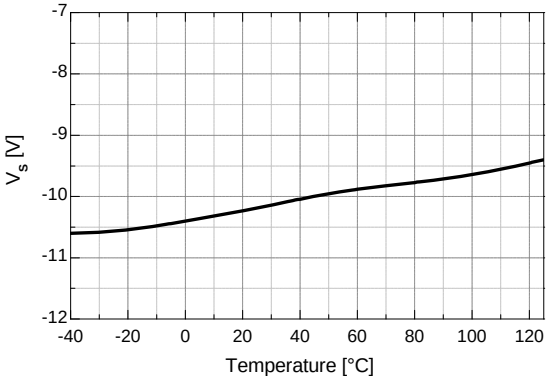

图 25. 容许的负 V_S 电压与温度的关系

开关时间定义

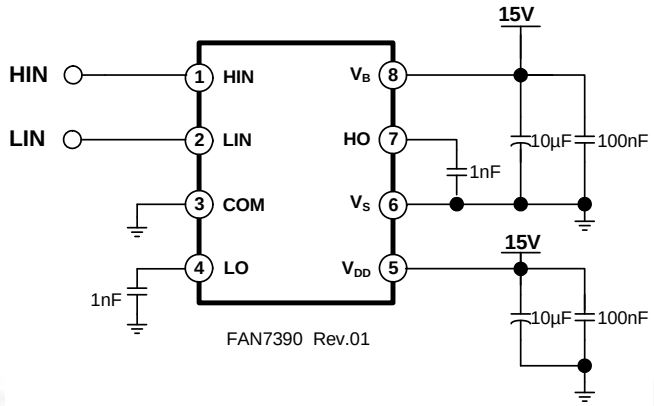

图 26. 开关时间测试电路 （参考 8-SOP）

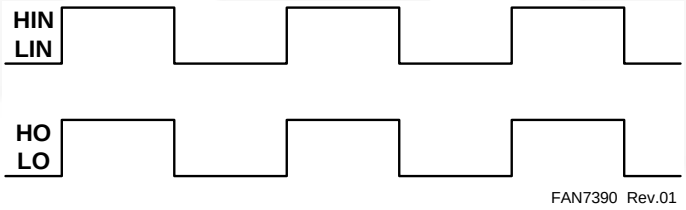

图 27. 输入 / 输出时序图

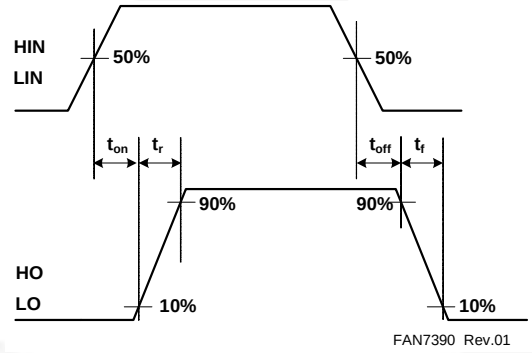

图 28. 开关时间波形定义

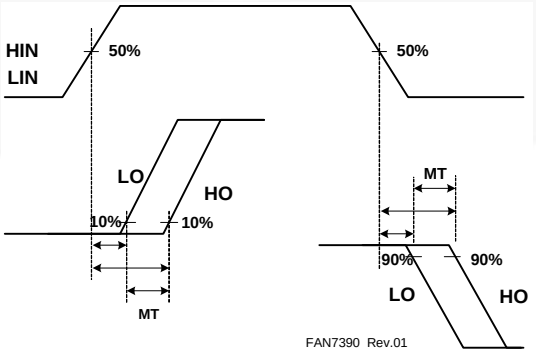

图 29. 开关匹配波形定义

物理尺寸

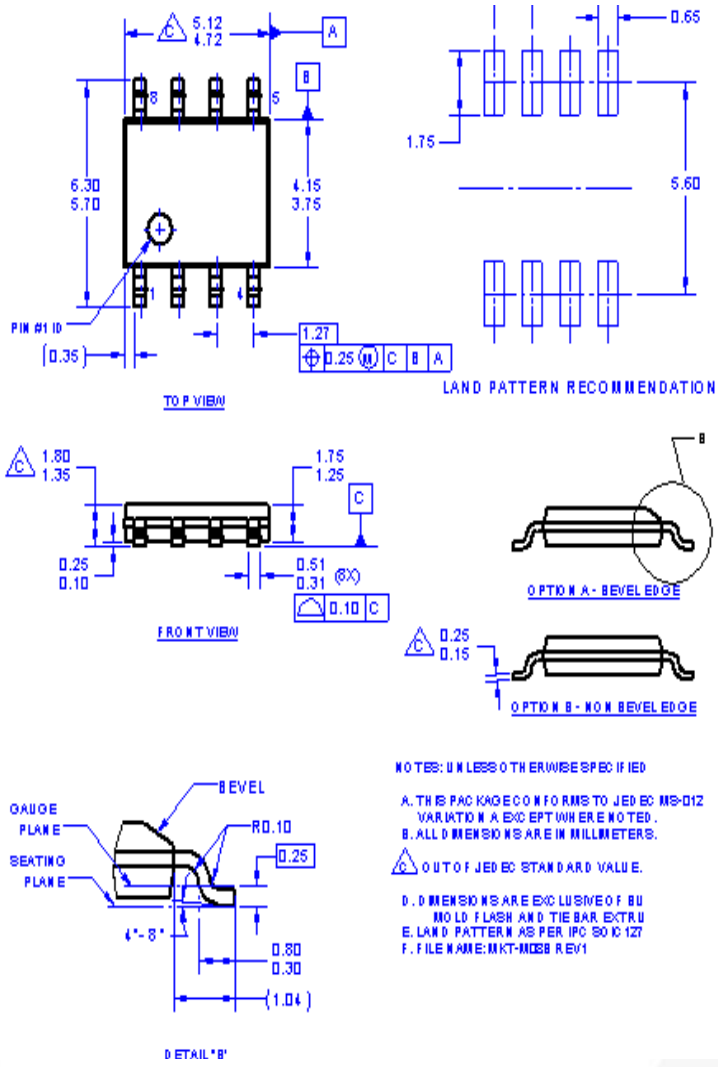

图 30. 8- 引脚小尺寸封装 (SOP)

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物理尺寸 (续)

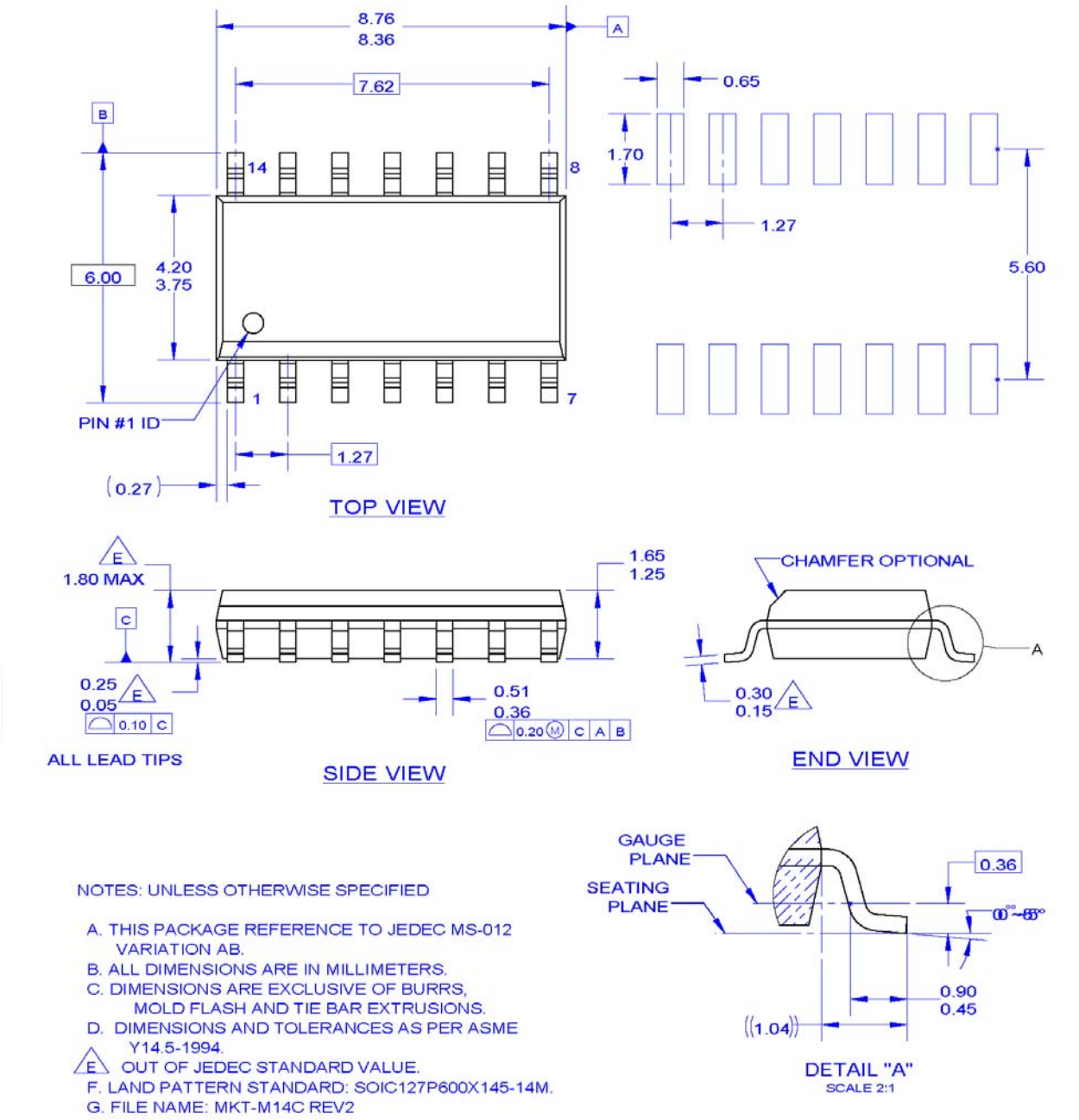

图 31. 14 引脚小尺寸封装 (SOP)

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