



# ECH8502

## Bipolar Transistor (-50V, (-)30A, Low V<sub>CE(sat)</sub>) Complementary Dual ECH8

ON Semiconductor®

<http://onsemi.com>

### Features

- Composite type, facilitating high-density mounting
- Low collector-to-emitter saturation voltage
- Halogen free compliance
- Mounting height 0.9mm
- NPN : V<sub>CE(sat)</sub>=0.08V(typ.)@I<sub>C</sub>=2.5A
- PNP : V<sub>CE(sat)</sub>= -0.12V(typ.)@I<sub>C</sub>= -2.5A

### Specifications ( ) : PNP

#### Absolute Maximum Ratings at Ta=25°C

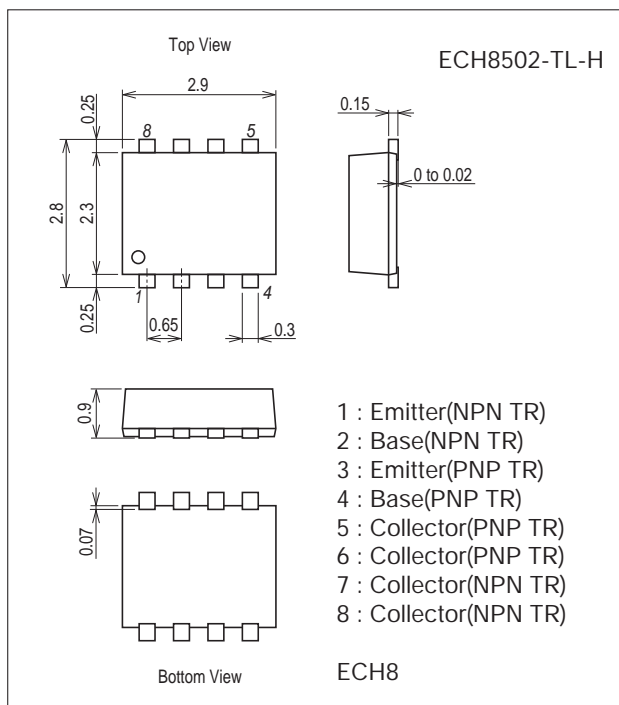
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V <sub>CBO</sub>		(-50)100	V
Collector-to-Emitter Voltage	V <sub>CEO</sub>		(-)50	V
Emitter-to-Base Voltage	V <sub>EBO</sub>		(-)6	V
Collector Current	I <sub>C</sub>		(-)5	A
Collector Current (Pulse)	I <sub>CP</sub>	PW≤1μs, duty cycle≤1%	(-)30	A
Base Current	I <sub>B</sub>		(-)600	mA
Collector Dissipation	P <sub>C</sub>	When mounted on ceramic substrate (900mm <sup>2</sup> ×0.8mm) 1unit	1.3	W
Total Dissipation	P <sub>T</sub>	When mounted on ceramic substrate (900mm <sup>2</sup> ×0.8mm)	1.6	W
Junction Temperature	T <sub>J</sub>		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Package Dimensions

unit : mm (typ)

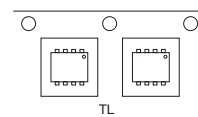
7011A-007



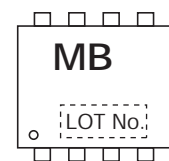
### Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

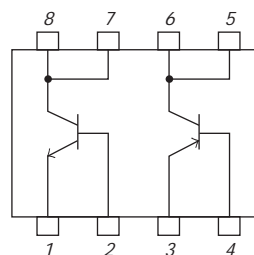
### Packing Type : TL



### Marking



### Electrical Connection



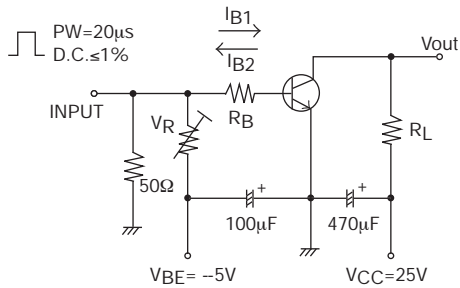
# ECH8502

## Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	$I_{CBO}$	$V_{CB}=(-)50V, I_E=0A$			(-)0.1	$\mu A$
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=(-)4V, I_C=0A$			(-)0.1	$\mu A$
DC Current Gain	$h_{FE}$	$V_{CE}=(-)2V, I_C=(-)500mA$	200		560	
Gain-Bandwidth Product	$f_T$	$V_{CE}=(-)10V, I_C=(-)500mA$		(260)290		MHz
Output Capacitance	$C_{ob}$	$V_{CB}=(-)10V, f=1MHz$		(45)25		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)2.5A, I_B=(-)125mA$		(-120)80	(-200)120	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=(-)2.5A, I_B=(-)125mA$		(-)0.85	(-)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0A$	(-50)100			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)1mA, R_{BE}=\infty$	(-)50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=(-)10\mu A, I_C=0A$	(-)6			V
Turn-On Time	$t_{on}$	See specified Test Circuit.		(30)30		ns
Storage Time	$t_{stg}$			(180)280		ns
Fall Time	$t_f$			(20)25		ns

Note : The specifications shown above are for each individual transistor.

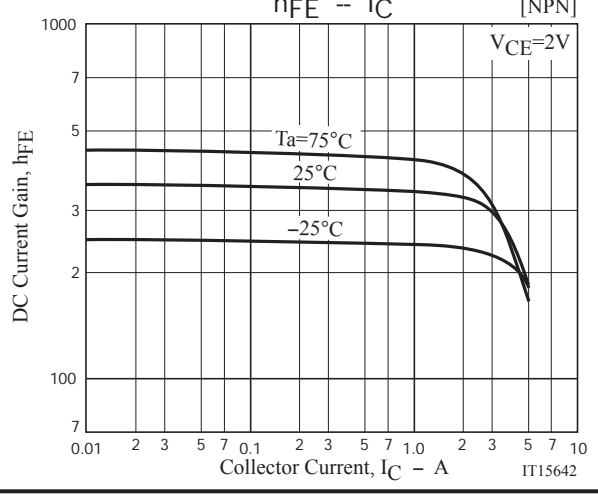
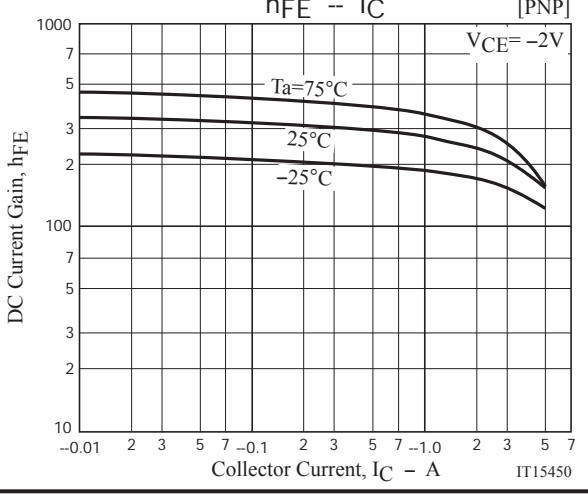
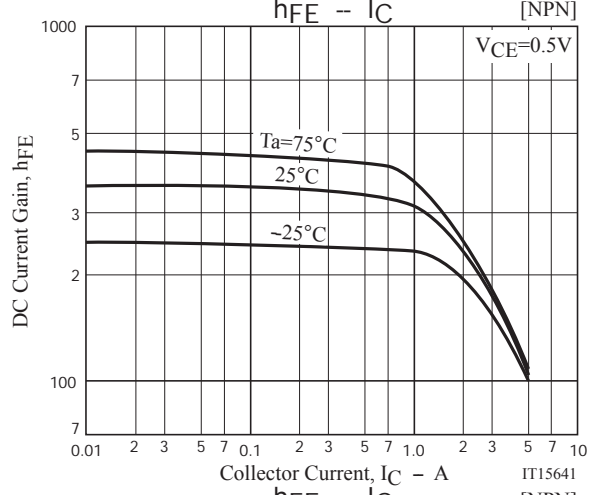
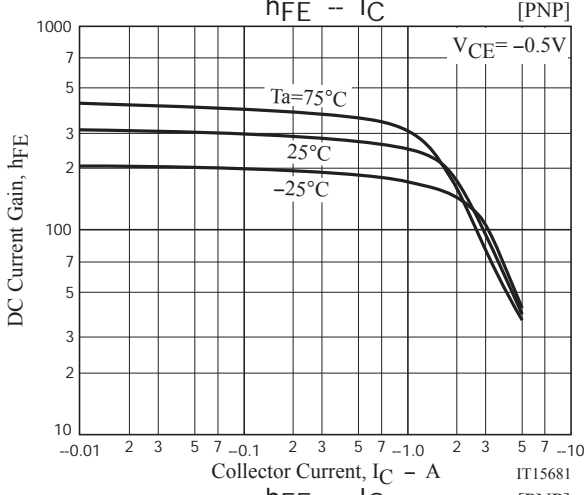
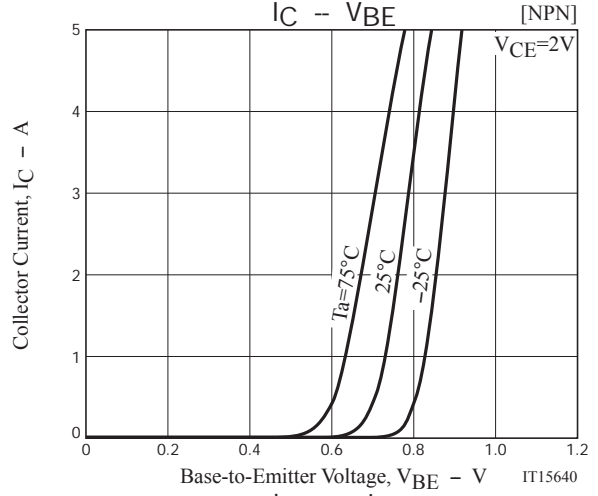
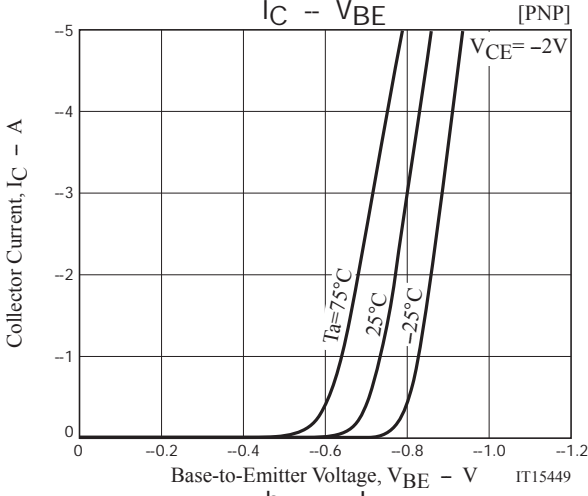
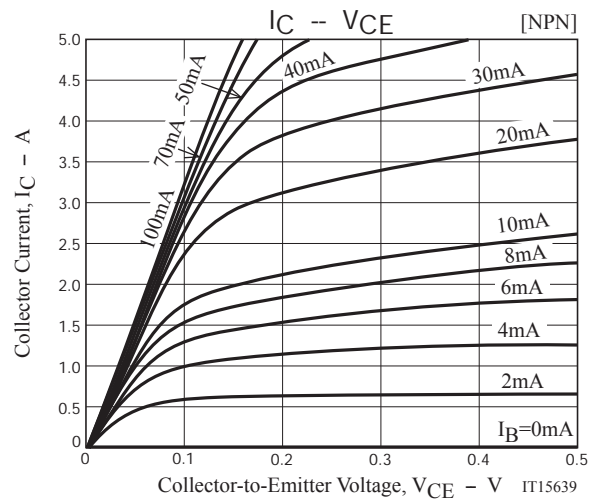
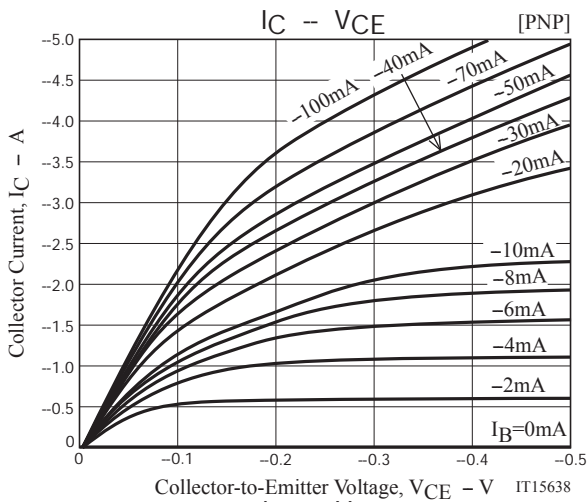
## Switching Time Test Circuit

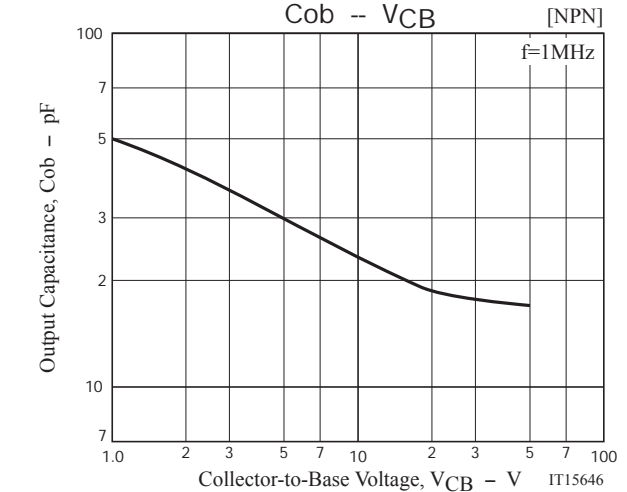
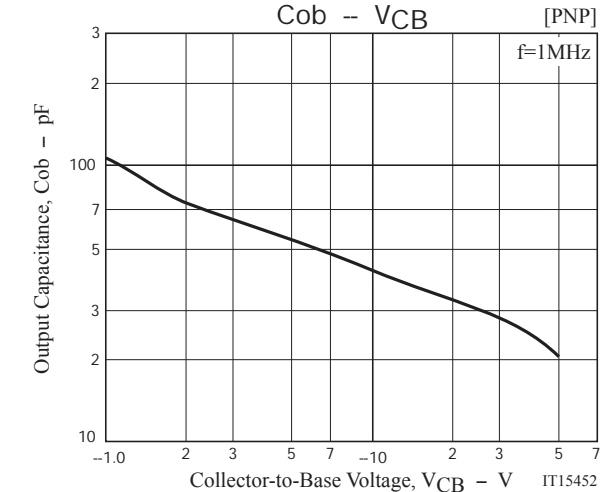
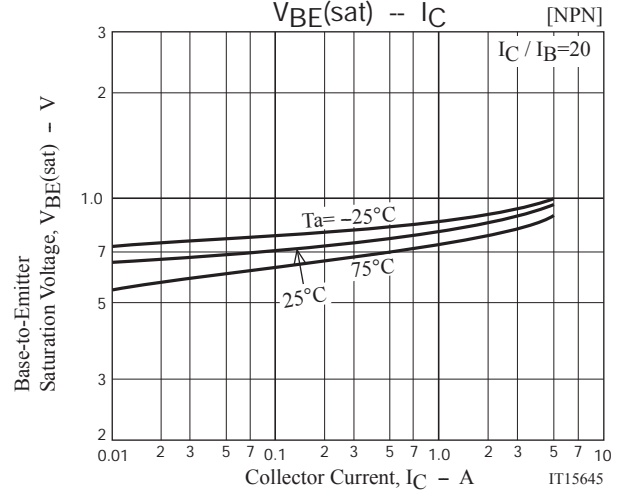
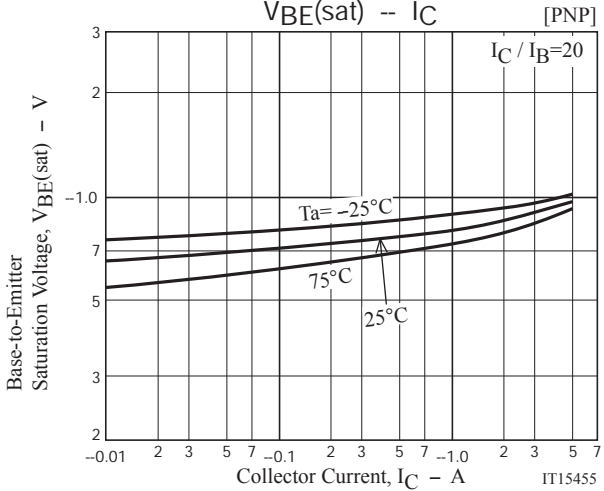
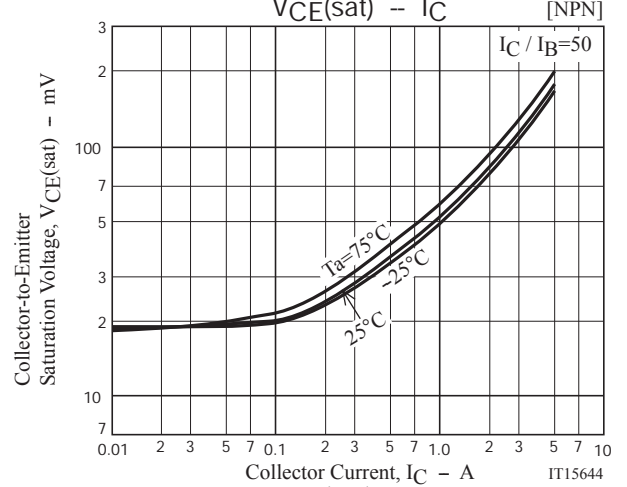
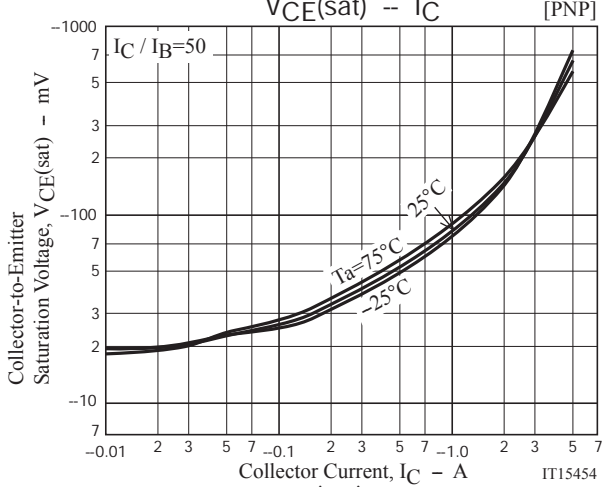
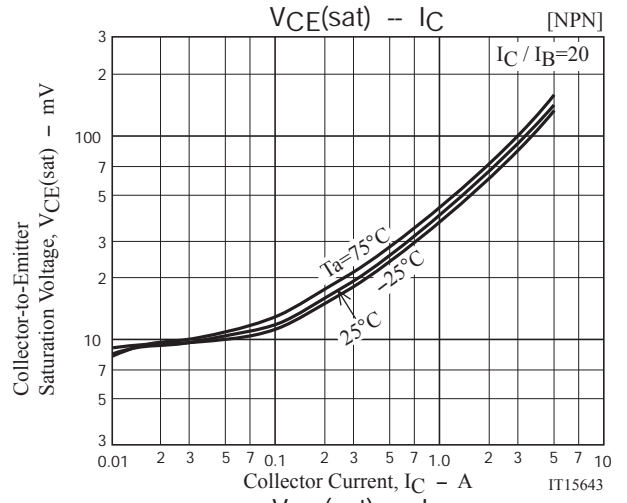
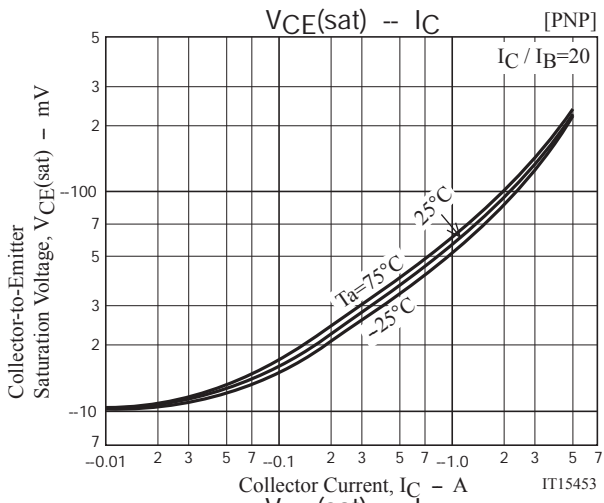


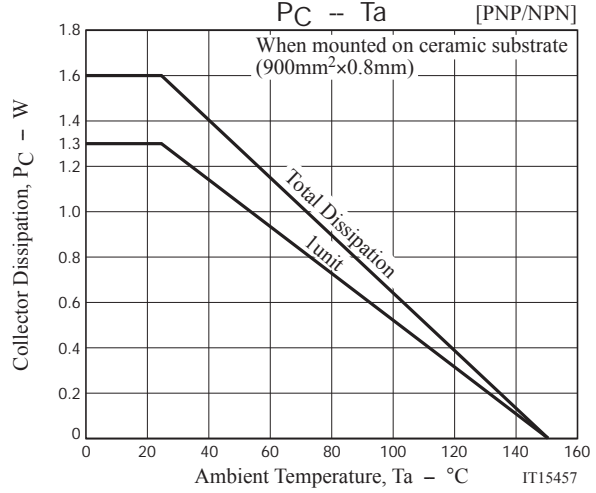
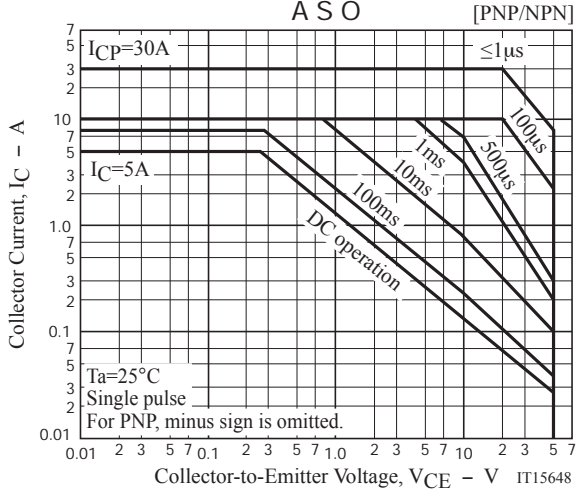
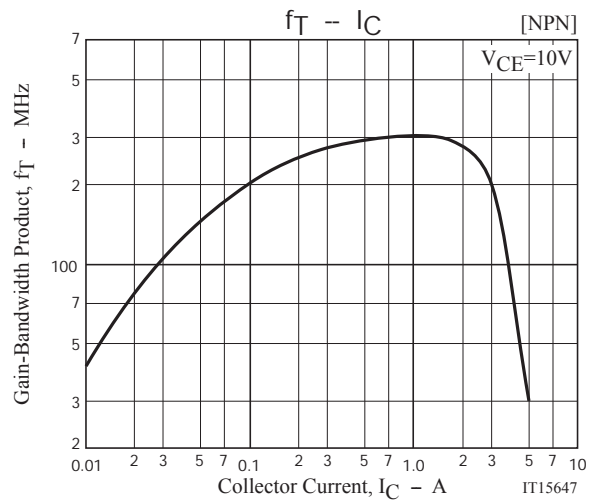
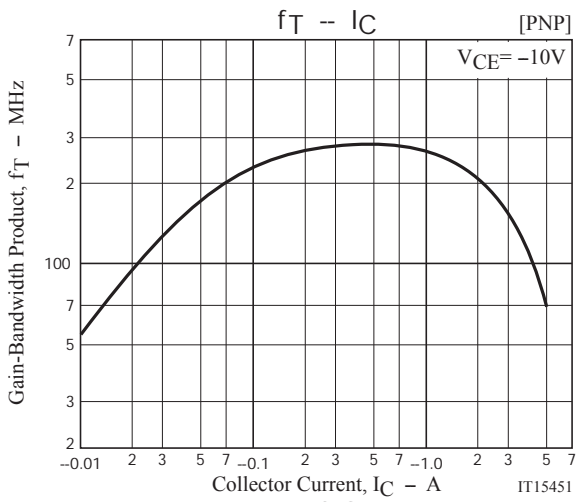
$I_C = 20I_{B1} = -20I_{B2} = 2.5A$   
 (For PNP, the polarity is reversed.)

## Ordering Information

Device	Package	Shipping	memo
ECH8502-TL-H	ECH8	3,000pcs./reel	Pb Free and Halogen Free







Embossed Taping Specification

ECH8502-TL-H

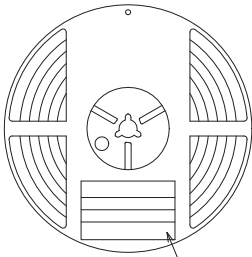
1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
ECH8	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Reel label, Inner box label  
(unit :mm)

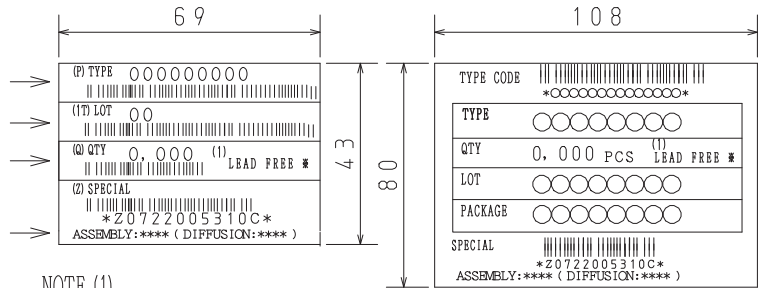
Outer box label  
It is a label at the time of factory shipments.  
The form of a label may change in physical distribution process.

Packing method



Reel label

Type No.  
LOT No.  
Quantity  
Origin



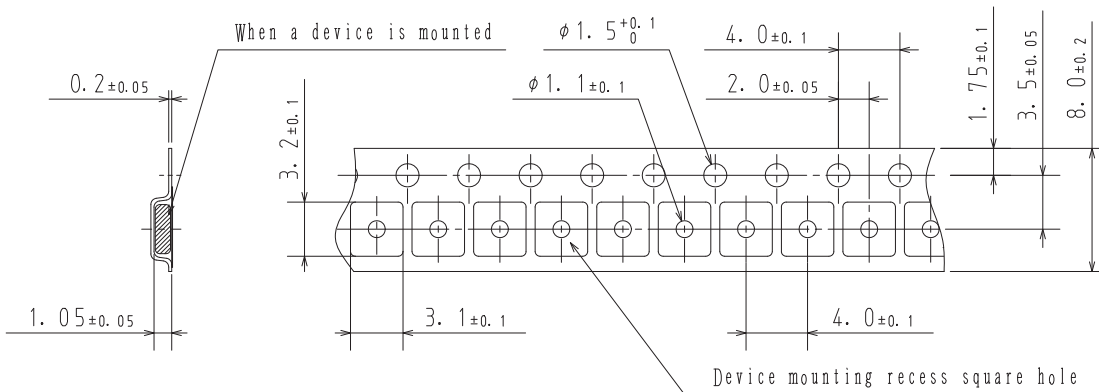
NOTE (1)

The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

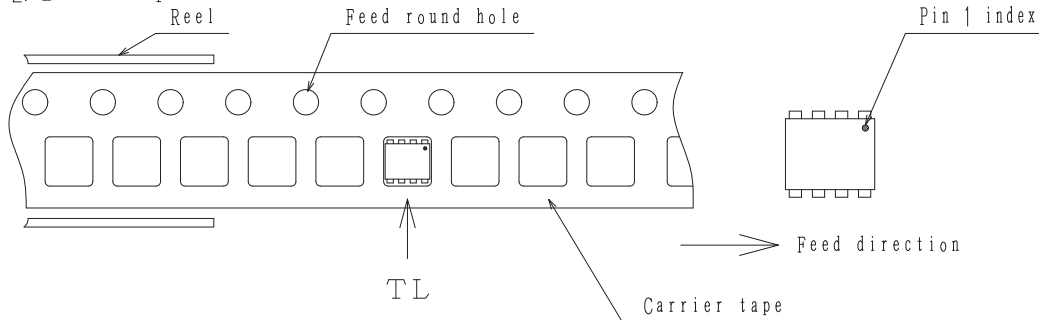
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



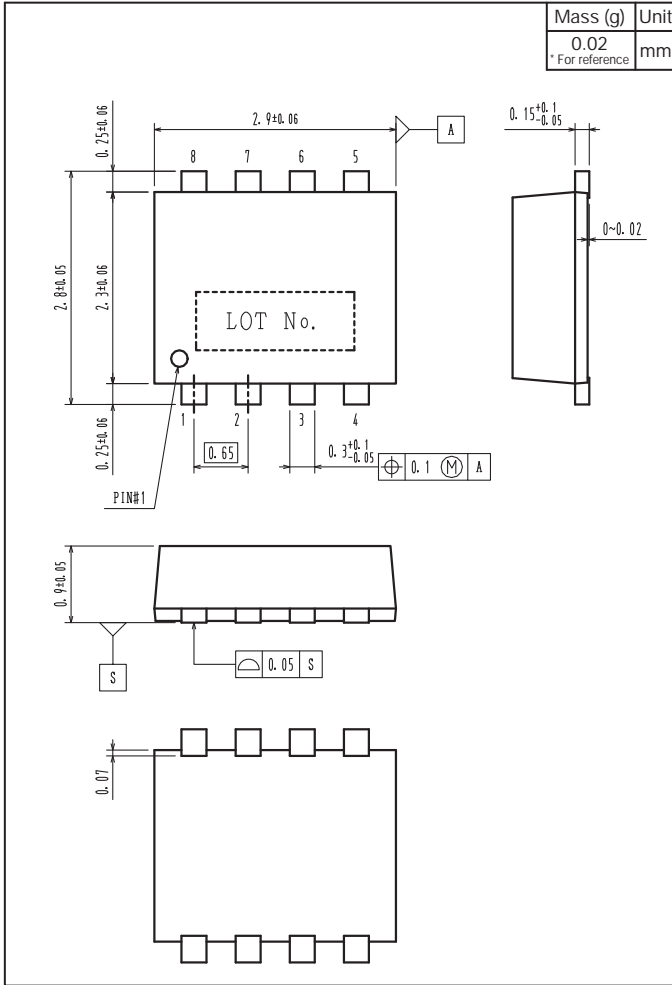
2-2. Device placement direction



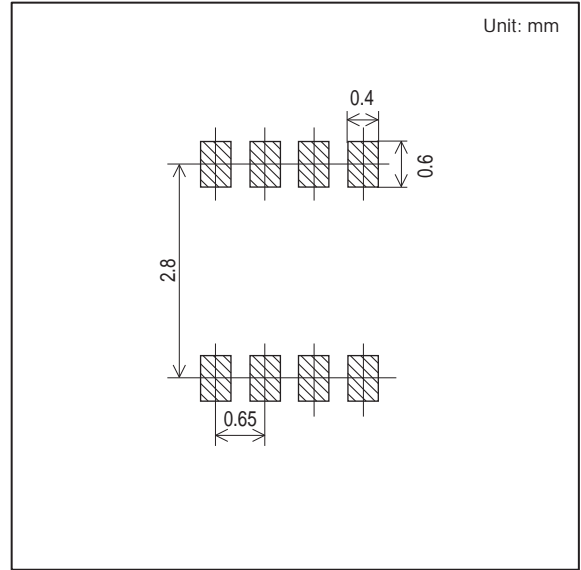
Those with pin 1 index on the feed hole side.....TL

# ECH8502

## Outline Drawing ECH8502-TL-H



## Land Pattern Example



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