2-Port PSE Controller for PoE Systems

Features

- IEEE 802.3AF-2003 and 802.3AT-2009 compliant
- Single DC power supply voltage input (45~57V)
- Wide temperature range: -40℃~+85℃
- Supplies 2 independent power ports
- Built-in power FETs
- Continuous system monitoring for every port
- Independent system parameters setting for every port
- Thermal monitoring and protection
- Built-in 3.3V regulators for external devices
- Built-in Power on Reset
- Configurations: (1) 30W x 2 ports
- Built-in LEDs control
- Built-in EEPROM interface for dumb application
- Package and operation temperature
  48 Pin(7mmx7mm) MQFN, -40~85℃

Application

- 2 port PSE

General Description

IP802 is a 2-port PSE (Power Sourcing Equipment) controller IC for PoE (Power over Ethernet) systems. It integrates power, analog and logic circuits into a single chip, and can be used for Midcap and Endpoint PSE applications.

IP802 meets all IEEE 802.3AF-2003 requirements, such as multi-point resistor detection, PD classification, DC Disconnect, and Back-off for Midcap. It also meets all IEEE 802.3AT-2009 requirements, such as two-event classification and supply maximum 36W per port.

IP802 comprises internal temperature monitoring and thermal protection to protect against junction overheating. The 3.3V regulator is built-in to support external devices. Multiple IP802s can integrate to build a 2 x N ports PSE system, and I^2C bus uses to collect PD power status from each IP802 to support global power managements.

Multiple IP802s can build a cost effective PHY level PSE system to support PD classification and power management without a host. With a management host, a networked LLDP (Link Layer Discovery Protocol) based multiple IP802s PSE system can be built. Based on LLDP (part of IEEE Std 802.3AT-2009), dynamic power management between PSE and PD can be maintained in real time for power efficiency.

Management switch host has options to communicate IP802s via I^2C bus for PSE management activities. Opt couplers can be implemented to provide electrical isolations between the host and IP802s for signal communication.

Table of Contents

List of Figures

List of Tables

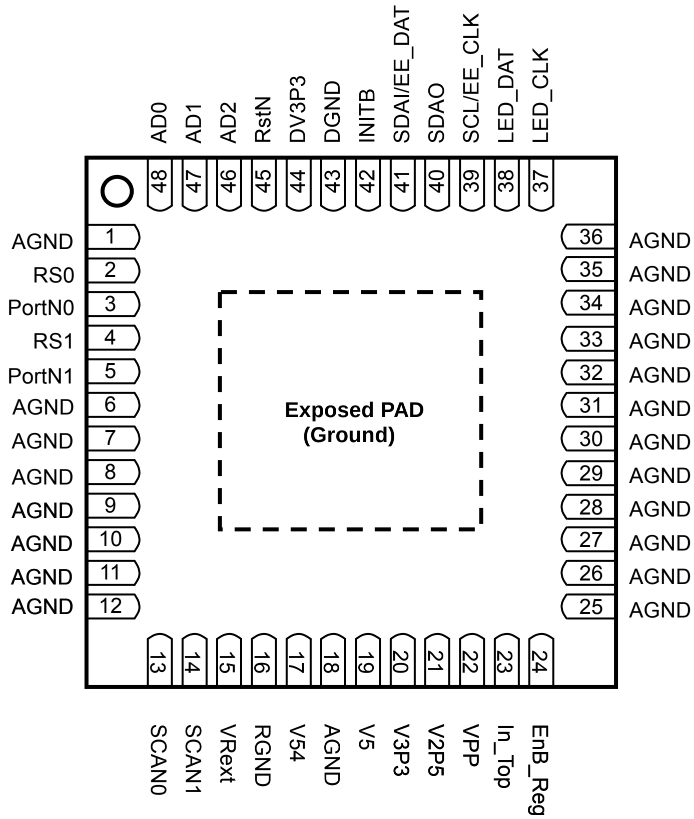
Revision History

Revision #	Date	Change Description
IP802-DS-R01	2017/03/28	Initial release

1 Pin diagram

1.1 IP802 Pin diagram (MQFN48)

(7mm X 7mm Top view)



Exposed pad is system GND, must be soldered to PCB ground plane

Figure 1 Pin Diagram

2 IP802 application diagram

2.1 Dumb & Smart device application

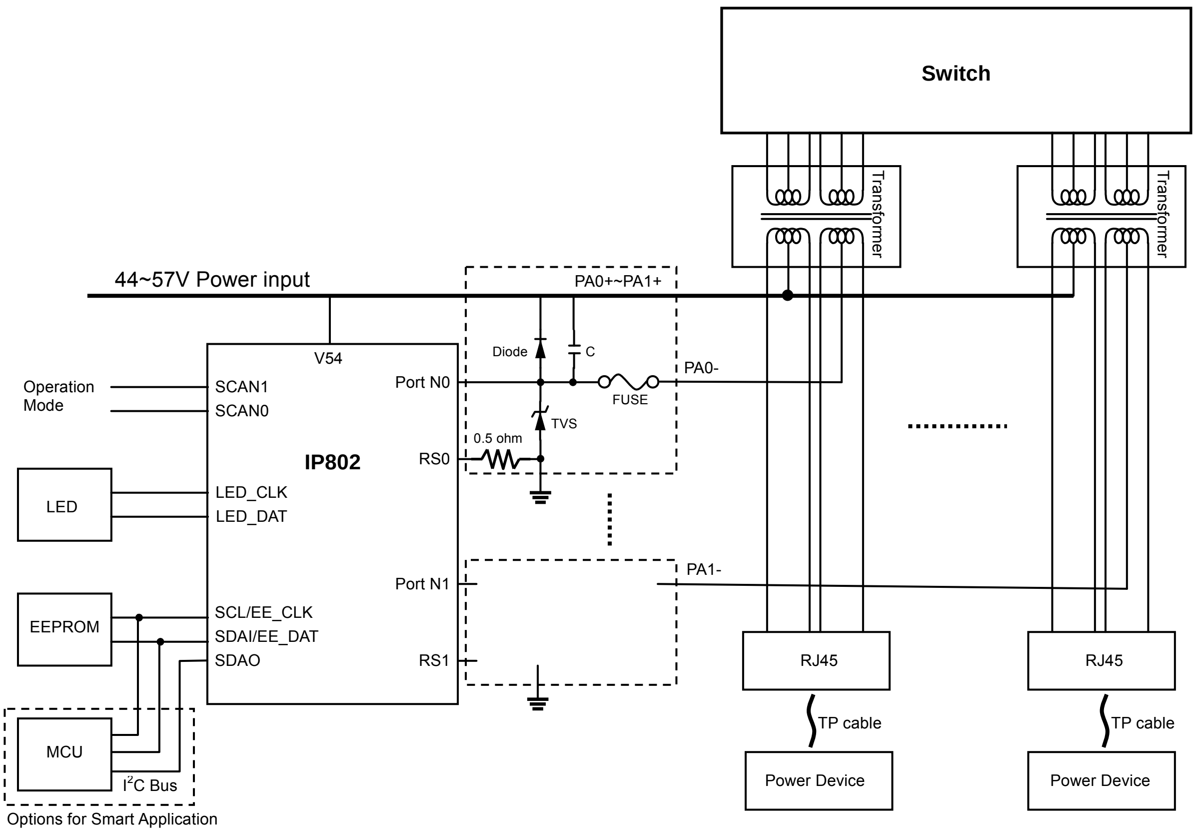


Figure 2 Application Diagram

Application	MCU	EEPROM	IP802 Mode setting	Reference
Smart	V	X	Manual mode	Section 5.3
Dumb	X	V: update default value X: use default value	Auto mode	Section 5.4

V: necessary; X: unnecessary

3 Block diagram

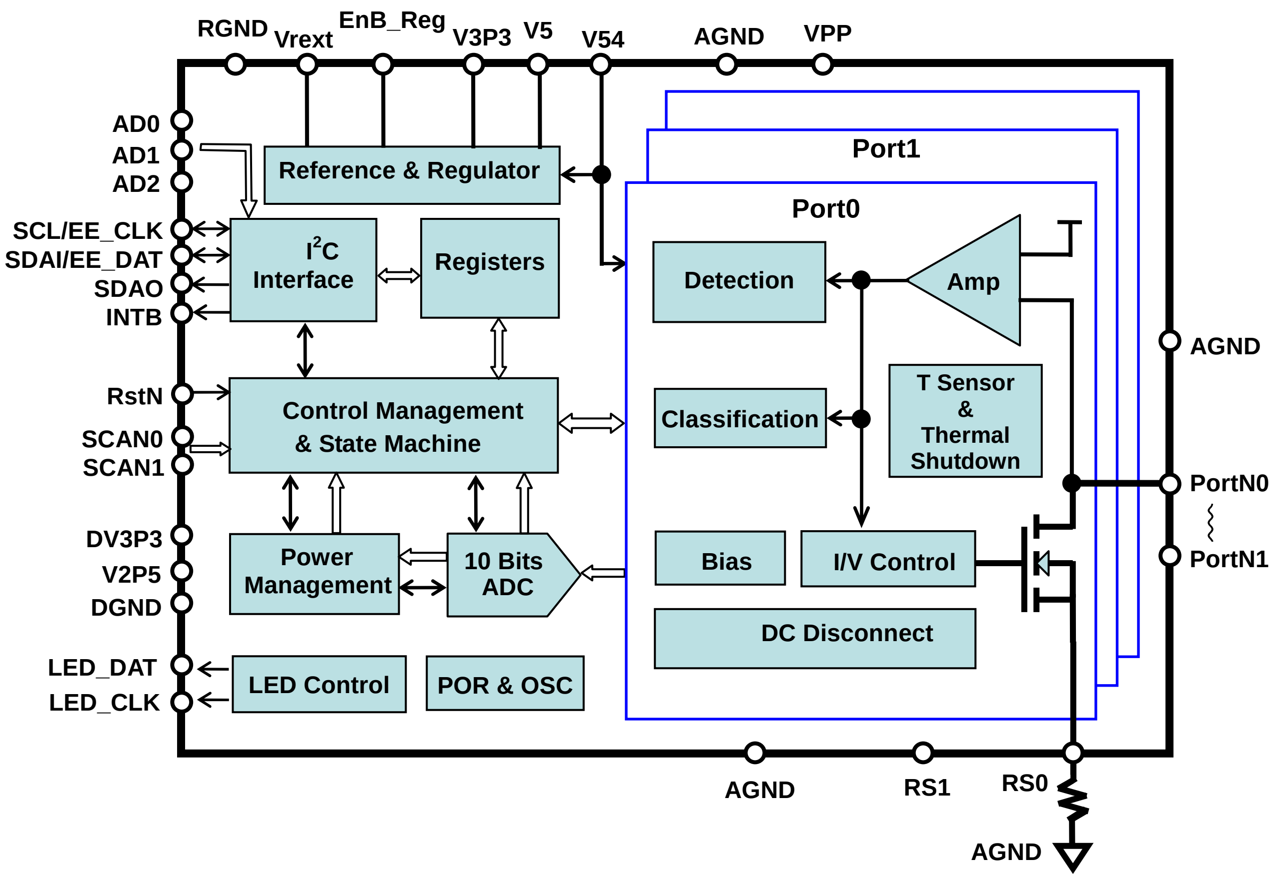


Figure 3 Block Diagram

3.1 Blocks Description

The blocks of IP802 include global blocks for and per port blocks as below:

Global blocks for 2 ports:
- Reference & Regulator
- I^2C Interface
- Registers
- Control Management & State Machine
- Power Management
- 10 Bits ADC
- POR & OSC

Per port blocks for individual port:
- Detection
- Classification
- I/V Control & Fold-back
- Amp
- DC Disconnect
- T sensor & Thermal Shutdown
- Bias
- Power MOSFET

3.1.1 Global Blocks

- **Reference & Regulator:**

The Reference & Regulator generates 2.5V, 3.3V and 5V power for internal use and 3.3V power also can supply typical 6mA current on V3P3 pin for external devices if EnB_Reg pin is connected to GND. If EnB_Reg is conncted to 3.3V, the internal 3.3V regulator is disabled and V3P3 pin should be connected to an external 3.3V power source.

It also generates 1.25V voltage on VREXT pin, which is connected to ground through an external 62KΩ resistor, to generate internal bias current.

- **Registers**:

The "Registers" provides the 8 bits data for Ilim, Icut programming registers, and all other needing registers per port

- **Control Management & State Machine:**

This block provides all the control procedures to perform PoE function. The "State Machine" implements as specified in the IEEE802.3AF/AT.

- **Power Management:**

The "Power Management" provides power management method to meet PD power requirement, or not to power PD if power is not enough.

- **10 Bits ADC:**

The 10 Bits ADC used to convert analog signals into digital bus for Control Management, State Machine, and Power Management for request.

- **POR & OSC:**

The POR generates an internal power on reset signal when V54 is power on. The POR also monitors V3P3, DV3P3, V5, & V54 voltage level. If these voltages level are below specific thresholds, a reset signal generates and resets IP802.

The OSC is an internal oscillator to generate 8MHz clock for IP802 timing source.

- **I^2C Interface:**

A host (master) can communicates with multiple IP802 (slave) via I^2C Interface (SCL/EE_CLK, SDAO, SDAI/EE_DAT) to collect PD power status to support global power managements and all control requirements.

3.1.2 Per Port Block

- **Detection:**

The IP802 uses 4 points detection method to discover PD. It shall accepted resistance as a valid “AF/AT PD” between 19KΩand 26.5KΩ, with a paralleled capacitance small than 0.15uF.

It shall rejects resistance with paralleled capacitance as an invalid “AF/AT PD” small than 15KΩ, larger than 33KΩ, or capacitance larger than 10uF.

The specification is as specified in the IEEE802.3AF/AT.

- **Classification:**

The “Classification” is to distinguish the requested power of PD as specified in the IEEE802.3AF/AT.
In IEEE 802.3AF, classification is 1-event method.
In IEEE 802.3AT, classification is 2-event method.

- **I/V Control:**

The “I/V Control” is to control the slew rate during “detection, classification, inrush, short circuit, power off … and so on”, as specified in IEEE802.3AF/AT

When short circuit event occurs, the “I/V control” will reduce the port current instantaneously to protect the power MOSFET from damages.

- **Amp:**

The “AMP” is used to convert the differential voltage between V54 and PortNx into single end voltage. This voltage will be fed into the “Detection, Classification, I/V Control” blocks to perform the IEEE8023AF/AT specifications.

- **DC Disconnect:**

The IP802 supports DC Disconnect function according to IEEE 802.3AF-2003 & IEEE 802.3AT-2009 requirement.

This DC Disconnect continuously monitors port current after port inrush time, and disconnects port current when port current is below 7.5mA (typical) for more than 360ms (typical) .Please refer to Tmpdo in table 8 for detail information.

- **T sensor & Thermal Shutdown:**

The “T sensor” senses the temperature of each port, and will shutdown the port current as temperature beyond 150℃. When temperature goes down to 129℃, the port will start again.

- **Bias:**

The “Bias” provides the current & voltage bias for all ports according to control signals.

4 Pin description

Type	Description	Type	Description
P	Power or Ground	O	Output
I	Input	OD	Open drain
IL	Input latched upon reset	NC	No connection in internal

Table 1 Pin description

Pin no.	Label	Type	Description
	EPAD	P	Exposed pad, it should be connected to AGND.
1	AGND	P	Analog ground
2	RS0	I	Port0 current sensing voltage input It should be connected to AGND through a 0.5Ω±1% resistor.
3	PortN0	I	Port0 negative feeding voltage input.
4	RS1	I	Port1 current sensing voltage input It should be connected to AGND through a 0.5Ω±1% resistor.
5	PortN1	I	Port1 negative feeding voltage input.
6	AGND	P	Analog ground
7	AGND	P	Analog ground
8	AGND	P	Analog ground
9	AGND	P	Analog ground
10	AGND	P	Analog ground
11	AGND	P	Analog ground
12	AGND	P	Analog ground
13	SCAN0	I	Operation mode, please refer to section 5.2 table 2 for more detail information.
14	SCAN1	I	Operation mode, please refer to section 5.2 table 2 for more detail information. It should be connected to AGND for normal operation.
15	Vrext	O	Connecting to RGND through a 62KΩ±1% resistor, it is for internal bias only.
16	RGND	P	Low noise analog reference ground, it should be connected to AGND.
17	V54	P	Main power supply input for chip A 4.7uF capacitor should be added between V54 and AGND.
18	AGND	P	Analog ground
19	V5	P	Internal 5V generation for internal use only. A 4.7uF capacitor should be added between V5 and AGND.
20	V3P3	P	When EnB_Reg is connected to AGND, the built-in 3.3v regulator is active, and besides IP802 itself, V3P3 can provide 3.3v (6mA) for external device. When EnB_Reg is connected to 3.3v, V3P3 should be connected to an external power 3.3V (6mA minimum) for IP802. A 4.7uF capacitor should be added between V3P3 and AGND.
21	V2P5	P	Internal 2.5V for internal use only Adding an 1uF capacitor between V2P5 and AGND
22	VPP	P	Connecting to V5 for EFuse power

(Continued)

Pin no.	Label	Type	Description
23	In_Top	P	It should be connected to RGND for normal operation.
24	EnB_Reg	I	Enable/Disable the internal 3.3V regulator Please refer to pin description of V3P3.
25	AGND	P	Analog ground
26	AGND	P	Analog ground
27	AGND	P	Analog ground
28	AGND	P	Analog ground
29	AGND	P	Analog ground
30	AGND	P	Analog ground
31	AGND	P	Analog ground
32	AGND	P	Analog ground
33	AGND	P	Analog ground
34	AGND	P	Analog ground
35	AGND	P	Analog ground
36	AGND	P	Analog ground
37	LED_CLK	OD	Serial LED clock output, please refer to section 5.9 LED interface.
38	LED_DAT	OD	Serial LED data output
39	SCL/EE_CLK	I/OD	In manual mode, this pin is I^2C clock input. In auto mode, this pin is clock out to EEPROM.
40	SDAO	OD	I^2C serial data output
41	SDAI/EE_DAT	I/OD	In manual mode, this pin is I^2C serial data input. In auto mode, this pin is data input from EEPROM.
42	INTB	OD	Interrupt output and low active
43	DGND	P	Digital ground, it should be connected to AGND.
44	DV3P3	P	Digital power 3.3V A 4.7uF capacitor should be added between DV3P3 and DGND and DV3P3 should be connected to V3P3.
45	RstN	I	It is a low active signal to reset IP802.
46	AD2	IL	I^2C device address bus AD2, please refer to section 5.3&5.9
47	AD1	IL	I^2C device address bus AD1
48	AD0	IL	I^2C device address bus AD0

5 Functional Description

5.1 System Reset

System reset occurs in either of the following conditions:

1. Reset triggered by the built-in power-on-reset circuit

IP802 generates an internal power on reset signal when V54 is power on. It didn't leave reset state until V54 reaching V54_UVL. After reset, IP802 still keeps on monitoring voltage level of V3P3, DV3P3, and V54. If the voltage level of V54 (V3P3) is below V54_UVL(V3P3_UVL),or over V54_OVL (V3P3_OVL), IP802 enters reset state. Please refer to section 7.3 for detail specification of V54_UVL, and V3P3_UVL. It is note that there are two values for one parameter because of hysteresis.

2. Reset triggered by the reset pin (RstN)

3. Reset triggered by the Software

➢ **System Control Register @ 0x02 of Page 1**

Bit #	R/W	Default	Description
7:1	R	0	**Reserved.**
0	R/W	0	**Software Reset**. Writing 1 to this bit initiates a system reset. After system reset, this bit is automatically cleared. Writing 0 has no effects. Reading this bit always returns 0.

5.2 Operation Modes & System Configuration

IP802 operates in four possible modes, namely the **Auto Mode**, **Manual Mode**, **Diagnostic Mode**, and **Scan Mode**. The mode in which the chip operates in is determined by the two pins **SCAN<1:0>** at system reset.

- **Auto Mode** means the chip is operating in a stand alone fashion, i.e. without the need for software intervention. The state machine does the detection, classification, power configuration, and system event monitoring automatically. The system events and status will be recorded in the corresponding registers, however, no interrupt will be generated and I^2C bus in this mode could not be used.
  IP802 detects voltage of power supply automatically to determine whether it should support AF or AT standard. If V54 is greater than 50 volts, IP802 supports AT standard (PSE type 2), otherwise IP802 supports AF standard (PSE type 1). The detection result is stored in the **AF/AT Mode Register**.
  Avoid setting the wrong AF/AT mode, IP802 reset time must be 0.5S or more waiting power supply voltage to stable.
  If there is an EEPROM, the contents of the EEPROM are loaded into the register file as initial values. Please refer to the section 5.4 for the description of the syntax of the contents of the EEPROM.

- **Manual Mode** means the chip will not be working, that is all ports are disabled, until the software has (1) enabled the port by writing 0x01 to the **Port Power Control Register**, and (2) written 1 to the **Start** bit of the **System Control Register**; at that time, the state machine start doing the detection, classification, power configuration, and system event monitoring as does in auto mode. The interrupt output pin will be active if the interrupt masks are turned off by software and predefined events occur. The ports can be disabled (power turned off and no further detection activity) by writing 0x00 to the **Port Power Control Register**. If the operation mode is either in manual mode or diagnostic mode, the host CPU can read register 0 (I^2C LSB Device Address Register) to make sure that IP802 has done the system start up procedure

- **Diagnostic Mode**, as its name suggests, is not for normal operation. It is used in field diagnosis and mass production test. In this mode, the state machine will be working in a step-by-step fashion, in which the state machine will stop at each detection, classification, and power configuration step and can be controlled by software to advance to the next step. The port current, voltage, or temperature measured by the ADC can be read in each steps. Another use of diagnostic mode is to program the E-Fuse during mass production.

- **Scan Mode** is also not for normal operation. It is used to execute the scan test through the scan in, scan out, and scan enable pins. The state machine will not be working in this mode.

Mode / Pin setting	Auto Mode			Manual Mode			Diagnostic Mode	Scan Mode
	LED Master	LED Slave	LED Disable	LED Master	LED Slave	LED Disable		
SCAN0	0	0	0	1	1	1	0	1
SCAN1	0	0	0	0	0	0	1	1
AD2	1	0	X	1	0	X	X	X
LED_CLK	1	1	0	1	1	0	0	X
LED_DAT	1	1	0	1	1	0	X	X

Please refer to Section 5.11 for LED mode setting.

Table 2 Mode Setting

A summary of available functions in different modes

Function	Auto mode	Manual mode	Diagnostic mode	Reference
Auto start detection,classfiction, and power up	V	-	-	Section 5.2
Program to detection, classfiction, and power up	-	V	-	Section 5.2
Stepbystepdetection classfiction, and power up	-	-	V	Section 5.2
Access register through I^2C	-	V	V	Section 5.3
Load EEPROM	V	V	V	Section 5.4
LED master & slave	V	V	-	Section 5.9

Table 3 Available functions in Operation modes

- **System Configuration Register @ 0x01 of Page 1**

Bit #	R/W	Default	Description
7:6	R	N/A	**Operation Modes**. At system reset, these bits latch the input pins **SCAN<1:0>** to determine the operation mode. 00b: Auto Mode. 01b: Manual Mode. 10b: Diagnostic Mode. 11b: Scan Mode.
5	R	0	Reserved.
4	R/W	0	**Alternative Indicator**. 0: Alternative A. 1: Alternative B.
3:0	R	0	Reserved.

AF/AT Mode Register @ 0x25 of Page 0

Bit #	R/W	Default	Description
1:0	R/W	0x00	**AF/AT Mode**. The 2 bits represent the AF/AT mode of the 2 ports, where bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc. 0 = AF mode. 1 = AT mode. In auto mode, IP802 will detect the supply voltage to determine AF/AT mode and automatically update this register. In manual mode or diagnostic mode, this register should be written by host CPU. Note: When Host Defined Power Limit (HDPL) is used, please refer to Host Defined Power Limit (HDPL) application note.

5.3 I^2C Slave Interface

Through the I^2C slave interface of IP802, host CPU can access the register file in IP802. It consists of SCL, SDAO and SDAI pins, where SCL is Clock, SDAO is Serial Data Output and SDAI is Serial Data Input. It should be note that SDAO and SDAI could be connected to implement a bidirectional data pin. This I^2C interface supports the 7-bit addressing mode of the I^2C standard. The clock speed can be up to 1 Mbit/sec.

There can be up to eight IP802 chips on one I^2C bus, the LSB 3 bits of the I^2C address can be assigned with the address pin AD2~AD0. The MSB 4 bits of the I^2C address are fixed at **1010b**.

The following diagram is the register read/write cycles of the I^2C bus.

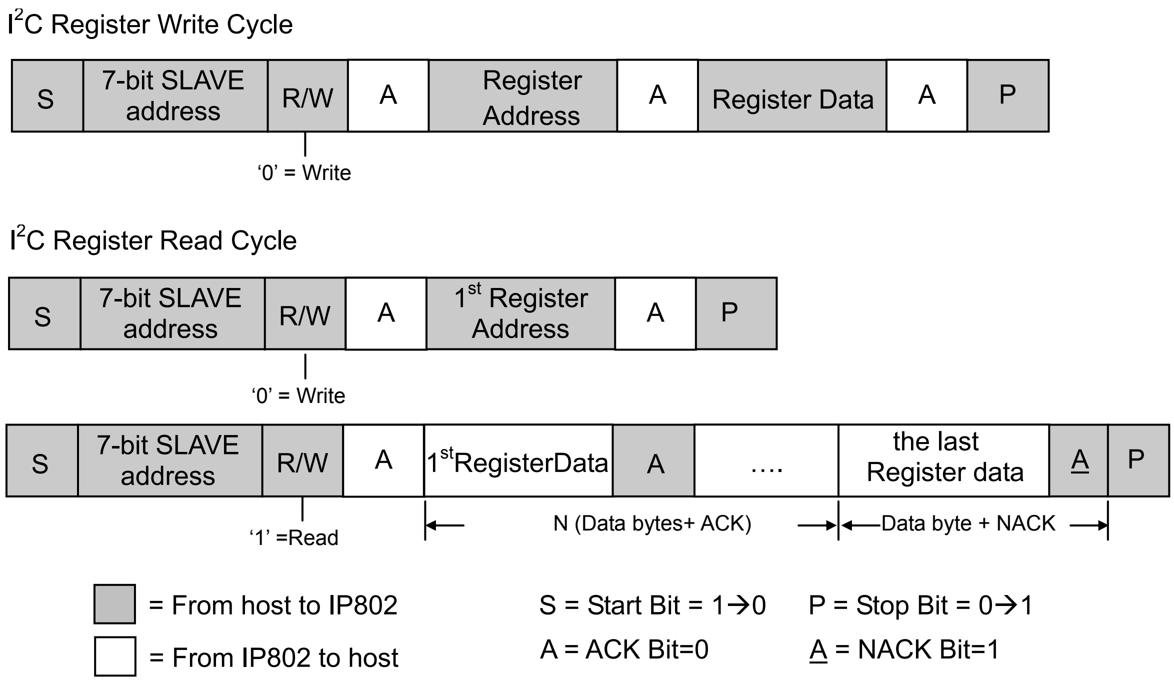


Figure 4 I^2C bus read/write cycles diagram

Following the 7-bit slave address and read/write bit, the 1st data byte received by IP802 is always interpreted as the register address to be accessed, thus named the address byte.

In a write cycle, following the address byte, there is only one byte, which contains the register data to be written. IP802 replies an ACK to the host whenever it receives a data byte. After writing this byte, the host should terminate the write cycle by sending a STOP bit.

In a read cycle, the host writes only one byte, which contains the initial address of registers to be read, to the IP802 firstly. Then the host needs to start another I^2C cycle with its read/write bit set to 1. IP802 will continue to send out the next data and increase the address by one automatically whenever the host acknowledges a data byte with an ACK, If the calculated register address is valid (within valid address range). The host can terminates a read cycle by sending a NACK following by a STOP bit. If the address of the data to be sent back falls out of valid register address range, IP802 always returns 00h.

- **I^2C Device Address Register @ 0x00 of Both Pages**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6	R/W	0	**Register Page**. This bit specifies the page number of the register to be accessed through the I^2C interface. 0: page 0, 1: page 1
5:3	R	0	Reserved.
2:0	R	000b	**I^2C Device LSB Address**. Unique device address to identify this chip on the I^2C bus. This address is latched in from the input pins AD2~AD0.

The highest I^2C clock speed supported is 1MHz. However, in order to prevent abnormal activity on the I^2C bus from hanging IP802, the I^2C interface implements a time out mechanism. Host CPU can stop the I^2C clock when it's low and resume the clock within 7 mini-seconds. If the clock does not resume within 7 mini-seconds, the I^2C interface will abort the current I^2C cycle and wait for the next START condition.

5.4 EEPROM controller

When IP802 operates in auto mode, the register file can be loaded with some initial value from external EEPROM (24xx series EEPROM, Maximum support to 24C16). IP802 reads the EEPROM starting from address 0, parses the contents of the EEPROM command blocks, checks for integrity of the contents, and then writes the designated registers. This process continues until there is either no more data or the integrity check fails. EEPROM is necessary only if user wants to modify the default value of registers in auto mode.

The format of the EEPROM follows:

BYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Command		# of Data Bytes					X
1	Starting Register Address							
2	Data Byte 1							
3	Data Byte 2							
…	…							
1 + N	Data Byte N							
2 + N	Checksum Byte							
3 + N	Next command block							

Figure 5 EEPROM Format

Where:

- **Command**: 10b = valid command, other values are invalid command and will stop the EEPROM loading process.
- **# Of Data Bytes**: the number of data bytes in this command block. 0 = 1 byte, 1 = 2 bytes, etc.
- **Starting Register Address**: the starting register address to be loaded by the following data bytes.
- **Data Bytes**: the data bytes to be loaded in to specified registers.
- **Checksum Byte**: the checksum byte is the checksum of all previous bytes in the command block. The checksum is calculated by adding all the previous bytes with the carry bit (if any) adding back to the sum. If the checksum fails, the system start up procedure fails and the system halt.

5.5 PSE State Machine

IP802 has 2 ports and each port is mainly controlled by a state machine to perform the detection, classification, and powering up procedures. As the eight state machines run in parallel, they contend for ADC 1 in the detection and classification procedures. Thus an arbiter is needed to grant the access rights among the eight state machines.

Furthermore, to limit the chip inrush current, a maximum of two ports are allowed to start their classification procedures simultaneously. And only one port is allowed to turn on power at a time. After successful detection, classification, and power configuration, the port power is turned on.

The state machine is also designed to respond to abnormal power events, such as overload, short circuit, and overheat (thermal shutdown); basically port power will be turned off when such event happens. It takes time to cool off the device after power is turned off, so the state machine will delay a certain amount of time before starting next detection procedure for the port.

- **Port 0~1 Power Control Registers @ 0x98~0x99 of Page 1**

Bit #	R/W	Default	Description
7:2	R	0x00	**Reserved.**
1:0	R/W	0x0	**PSE Enable.** **00b** = **PSE port disabled**. The port is disabled, port power is turned off, and the PSE state machine returns to the IDLE state. **01b** = **PSE port enabled**. The port is enabled, and the PSE state machine starts the detection process if the port is not in error condition and the **Start State Machine** bit in the **State Machine Control Register** is set to be 1. **10b** = **PSE port force power on**. The port is forced to turn power on without going through the normal detection, classification, and power configuration processes. This is used for testing purpose, not for normal operation. **11b** = **PSE port enabled (skip detection process)**. The port is enabled, and the PSE state machine skips the detection process and starts the classification process directly. This is only used for testing purpose and not for normal operation.

- **Port 0~1 State Machine Control Registers @ 0x90~0x91 of Page 1**

Bit #	R/W	Default	Description
7	R/W	0	**Start State Machine**. When in manual mode or diagnostic mode, writing 1 to this bit will start the state machine (from IDLE state) if the port is enabled.
6	R/W	0	**Step State Machine**. When in diagnostic mode, writing 1 to this bit will advance the state machine to the next state, after which this bit will be cleared by hardware. Writing 0 has no effect. Note that not every state can be stepped; Basically, only those states directly related to the detection and classification procedures can be stepped.
5	R	0	Reserved.
4:0	R	0	**Current State of the State Machine.** Current state of the state machine. 0 = DISABLED 1 = TEST_MODE 2 = TEST_ERROR 3 = IDLE 4 = START_DETECTION 5 = DETECT_EVAL 6 = SINATURE_INVALID

Bit #	R/W	Default	Description
			7 = BACKOFF 8 = START_CLASSIFICATION (AF Mode) 1-EVENT_CLASS (AT Mode) 9 = CLASS_EV1 (AT Mode) 10 = MARK_EV1 (AT Mode) 11 = CLASS_EV2 (AT Mode) 12 = MARK_EV2 (AT Mode) 13 = CLASSIFICATION_EVAL 14 = POWER_DENIED 15 = POWER_UP 16 = POWER_ON 17 = SET_PARAMETERS (AT Mode) 18 = DLL_ENABLE (AT Mode) 19 = ERROR_DELAY (AT Mode) ERROR_DELAY_SHORT (AF Mode) 20 = ERROR_DELAY_OVER (AF Mode)

- **Port 0~1 Detected Signature Registers @ 0x68~0x69 of Page 0**

Bit #	R/W	Default	Description
7:3	R	0x0	Reserved.
1:0	R	0	**Detected Signature**. 00b = R_{BAD}. 01b = R_{GOOD}. 10b = R_{OPEN}.

- **Port 0~1 Invalid Signature Counter Registers @ 0xB0~0xB1 of Page 1**

Bit #	R/W	Default	Description
3:0	R	0	**Invalid Signature Counter**. When an invalid signature is detected in the detection process, this counter is increased by 1.

- **Port 0~1 Classification Event Number Registers @ 0xA0 of Page 1**

Bit #	R/W	Default	Description
3:2	R/W	2	**Number of Classification Events for Port 1**. Valid value range is from 0 to 2. The value 3 will be regarded as 2. If the value is 0, no classification is executed, and the PD is always deemed class 0 device. This register can be written to by host CPU. However, according to IEEE802.3 standard, if the port is in AF mode, only one classification event is executed, and in AT mode, there will be two classification events. So, this register will be automatically updated when the AF/AT Mode Register is updated.
1:0	R/W	2	**Number of Classification Events for Port 0**.

- **PSE Skip Event 2 Register @ 0xA2 of Page 1**

Bit #	R/W	Default	Description
1:0	R/W	0xFF	**Skip the Second Classification Event.** Bit 0 corresponds to port 0, bit 1 corresponds to port 1, etc. 0 = do not skip event 2, 1 = skip event 2.

- **Port 0~1 Detected PD Class Registers @ 0x88 of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6:4	R	5	**Detected PD Class of Port 1**. 0 = Class 0 1 = Class 1 2 = Class 2 3 = Class 3 4 = Class 4 5 = Unknown
3	R	0	Reserved.
2:0	R	5	**Detected PD Class of Port 0.**

- **Port I_{CLASS} Registers @ 0x78~0x7B of Page 0**

Bit #	R/W	Default	Description
7:6	R	0	Reserved.
5:0	R	0	**Port I_{CLASS} MSB**. The current detected in classification. The MSB 10 bits are integer and the LSB 4 bits are fractional. Unit is in mAmp.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0x00	**Port I_{CLASS} LSB.**

- **Port PD Requested Power Registers @ 0x90~0x93 of Page 0**

Bit #	R/W	Default	Description
7:0	R	0x00	**PD Requested Power of Port.** The power requested by a PD that passes detection and classification. The MSB 6 bits are the integer part, and the LSB 2 bits are the fractional part. Unit is in Watts.

5.6 Power Manager

Power manager is responsible for two tasks: **power configuration** and **power monitoring**. Power configuration is the task to allocate power to the ports requesting for power. Power monitoring is the task to monitor power conditions (current, voltage, and temperature). When invalid conditions occur, proper actions will be taken to prevent hazardous consequences.

5.6.1 Power Trunks

Before doing power configuration, the total available power must be determined first. IP802 supports two trunks of power, where each power trunk has its own set of parameters to facilitate the calculation of total available power.

- **Trunk Power Limit** is the maximum power supply capacity allocated to the power trunk.

- **Trunk 0 Power Limit Register @ 0x40~0x41 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved**.
2:0	R/W	1	**Trunk 0 Power Limit (MSB)**.
Bit #	**R/W**	**Default**	**Description**
7:0	R/W	0x2C	**Trunk 0 Power Limit (LSB)**. Trunk Power Limit specifies the upper limit of the power supply. Default is 300 Watts.

- **Trunk 1 Power Limit Register @ 0x42~0x43 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved. 0x42**
2:0	R/W	1	**Trunk 1 Power Limit (MSB). 0x42**
7:0	R/W	0x2C	**Trunk 1 Power Limit (LSB). 0x43** Default is 300 Watts.

- **Trunk Select Register @ 0x69 of Page 1**

Bit #	R/W	Default	Description
7:3	R	0	**Reserved**.
1:0	R/W	0	**Trunk Select**. Writing to this register will switch power trunk. Note that whenever the parameters of the power trunk currently in use are updated, this Trunk Select Register must also be written to make the newly updated parameters in effect. 0 = Trunk 0, 1 = Trunk 1.

5.6.2 Power Configuration

Power manager is responsible to allocate powers to the ports that pass the detection and classification process. To do so, several parameters must be specified or be calculated in advance:

1) Maximun Trunk Power (specified in register 0x40~0x43, page1).
2) Power configuration Mode (specified in register 0x10, page1).

- **Power configuration Mode** specifies the way to determine the requested port power of the power device (**RPP** of **Power configuration Mode Register**) in the power configuration process.

- **Requested Port Power** is determined in the power configuration process according to **RPP** of power configuration mode.

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- **Power configuration Mode Register 0 @ 0x10 of Page 1**

Bit #	R/W	Default	Description
7:5	R/W	0	Reserved
4:3	R/W	1	**Requested port power (RPP)** specifies ways to determine the port power requested by the power device in the power configuration process 0 = Host Defined Power Limit (HDPL) specified in Host Defined Power Limit registers 1 = Class defined power limit (CDPL) specified in Class Defined Power Limit registers. Note: When Host Defined Power Limit (HDPL) is used, please refer to Host Defined Power Limit (HDPL) application note.
2:0	R	0	Reserved.

- **Class 0 Defined Power Limit Registers @ 0x12 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 0 Port Power Limit (C0DPL)**. The maximum allowable port power for class 0 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W.

- **Class 1 Defined Power Limit Registers @ 0x13 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x10	**Class 1 Port Power Limit (C1DPL)**. The maximum allowable port power for class 1 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x10 = 4.0W.

- **Class 2 Defined Power Limit Registers @ 0x14 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x1c	**Class 2 Port Power Limit (C2DPL)**. The maximum allowable port power for class 2 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x1c = 7.0W.

- **Class 3 Defined Power Limit Registers @ 0x15 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 3 Port Power Limit (C3DPL)**. The maximum allowable port power for class 3 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W.

- **Class 4 Type 1 Power Limit Registers @ 0x16 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x3e	**Class 4 Port Power Limit Type 1 (C4DPL_TYPE1).** The maximum allowable port power for class 4 type 1 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x3e = 15.5W (i.e. Type 1 device, I_{CABLE} = 0.35A, $V_{PORT\_PSE\_MIN}$ = 44V)

- **Class 4 Type 2 Power Limit Registers @ 0x17 of Page 1**

Bit #	R/W	Default	Description
7:0	R/W	0x78	**Class 4 Port Power Limit Type 2 (C4DPL_TYPE2).** The maximum allowable port power for type 2 class 4 devices if RPP is set to be 1. Bit 7~2 specifies the integral part of the power limit, whereas bit 1~0 specifies the fractional part of the power limit value. Default is 0x78 = 30.0W (i.e. Type 1 device, I_{CABLE} = 0.60A, $V_{PORT\_PSE\_MIN}$ = 50V)

5.6.3 Port Polling

Besides power configuration, power manager is also responsible for the monitoring of port current (I), port voltage (V), and port temperature (T). When either of IVT is out of its valid range, power manager will take prompt actions to prevent the system from hazardous consequences.

Power manager do the monitoring by periodically polling the IVT of each port. The poll period can be specified in the **IVT Poll Register**.

- **Force Poll Register @ 0xE2 of Page 0**

Bit #	R/W	Default	Description
1:0	R/W	0	**Force Poll**. Writing 1 to a bit will force an IVT poll on the corresponding port. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc. When the polling completes, the bit will be cleared automatically.

- **IVT Poll Register @ 0xE3 of Page 0**

Bit #	R/W	Default	Description
7	R	0	Reserved.
6	R/W	1	**Check Port Voltage**. 0 = do not check port voltage. 1= check port voltage after polling.
5	R/W	0	**Auto Poll**. Enable automatically polling of IVT of powered ports. In auto mode, this bit will be set to 1 automatically after system reset.
4:0	R/W	10	**Poll Period**. Number of 8ms between each poll to the port IVT. Minimum value is 10. Thus, by default, the poll period is 10 * 8 = 80 ms.

- **Port 0~1 Current Registers @ 0xA0~0xA3 of Page 0**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Port Current**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port Current**. The port current. MSB 10 bits are the integer part and LSB 2 bits are the fractional part. The unit is mA.

- **Port 0~1 Voltage Registers @ 0xB0~0xB3 of Page 0**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Port Voltage**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port Voltage**. The MSB 8 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Volts. This value is updated every time the port is polled. Note that the true port voltage is (**Supply Voltage - Port Voltage**). Please refer to Supply Voltage Registers.

- **Port 0~1 Temperature Registers @ 0xC0~0xC3 of Page 0**

Bit #	R/W	Default	Description
7:5	R	0	Reserved.
4:0	R	0	**Port Temperature**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Port Temperature**. The MSB 9 bits are the integer part and the LSB 4 bits are the fractional part. The unit is Celsius. This value is updated every time the port is polled.

- **Supply Voltage Registers @ 0xE0~0xE1 of Page 0**

Bit #	R/W	Default	Description
7:4	R	0	Reserved.
3:0	R	0	**Supply Voltage**.
Bit #	**R/W**	**Default**	**Description**
7:0	R	0	**Supply Voltage**. The supply voltage in Volts. The MSB 8 bits are the integer part, where the LSB 4 bits are the fractional part.

5.6.4 Power Event Handling

After the IVTs are polled and recorded, the power manager checks the polled values against predefined valid ranges. If the polled values drop out of the predefined valid range, power events are recorded and handled. The power events triggered by power manager **Port Temperature Limit Event**.

When a power event occurs, if its corresponding power event handle bit is 1, the port power is turned off. If IP802 is in manual mode or diagnostic mode, and the power event's corresponding status mask bit is 1, an interrupt will be issued to the host CPU.

- **Port Temperature Limit Event (Bit 7).** After the port is polled and if the port temperature is above the value specified in **Port Temperature Limit Register**, a **Port Temperature Limit Event** occurs.

- **Port Temperature Limit Registers @ 0x24~0x25 of Page 1**

Bit #	R/W	Default	Description
7:5	R	0	Reserved.
4:0	R	0x9	**Port Temperature Limit.**
Bit #	**R/W**	**Default**	**Description**
7:0	R	0x60	**Port Temperature Limit**. The port temperature limit in Celsius, over which a port temperature limit event will be reported. The 9 MSB bits are the integer part, and the 4 LSB bits are the fraction part. Default 0x960 = 150°C.

5.7 Real time Monitor Power Event

Power events described in previous sections are discovered only when the ports are polled. The analog monitor can continuously watch over and report time-critical power events so that the power manager can take prompt actions. Power events from analog monitor include thermal shutdown event, severe short circuit event (I > 1Amp), MPS error event (DC Disconnect), overload event ($I > I_{CUT}$), and short circuit event ($I > I_{LIM}$).

- **Thermal Shutdown Event** is the event where the port temperature is over the pre-defined thermal shutdown threshold. The port power is turned off and the port is eligible for detection only after the port is cooled off (temperature drops below the threshold).
- **Severe Short Circuit Event** is the event where the port current is over 1 Amp. Immediate action must be taken to eliminate such event. The power manager responds to this event by temporarily turn off port power.
- **DC Disconnect Event** is the event the port cannot maintain its power signature (MPS). If the event lasts for specified period of time (**Event High Count Register**), this will be considered an **MPS error event** and the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Overload (I_{CUT}) Event** is the event where port current is greater than I_{CUT}. If the event lasts for specified period of time (**Event High Count Register**), this will be considered an **overload event**. When an overload condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.
- **Short Circuit (I_{LIM}) Event** is the event where port current is greater than I_{LIM}. This event should be sampled by the power manager to determine if a **short circuit event** has occurred either during the power up process or after the port being powered up. When a short circuit condition is determined, the port power will be turned off. After the power is turned off the port start another detection process after about 1.6 seconds.

A summary of power off conditions

Condition	description	Power off moment	Reference Section
Power Trunk< budget	Power Trunk not enough power to port used	Power up sequence	5.6.1
Port temp > limit	Port temperature Event	IVT polling	5.6.4
Port temp > thermal	Thermal Shutdown Event	Real-time monitor	5.7
Port I > 1A	Severe Short Circuit Event	Real-time monitor	5.7
Port unplug UTP	DC Disconnect Event	Real-time monitor	5.7
Port I > Ilim	short circuit event	Real-time monitor	5.7
Port I > Icut	Overload (I_{CUT}) Event	Real-time monitor	5.7

Table 4 Port power off conditions

5.8 Port Status and Interrupt

Port state and power events are recorded in the registers. In manual mode and diagnostic mode, these statuses can generate interrupts to host CPU for further processing.

- **Port Power Event Handle Register @ 0x81 of Page 1**

Bit #	R/W	Default	Description
7	R/W	1	**Port Temperature Limit Event Handle**. 0 = Do not turn off power when the event occurs. 1 = Turn off power when the event occurs.
6:0	R/W	0x1F	Not used.

- **Port 0~1 Power Event Register @ 0x70~0x71 of Page 1**

Bit #	R/W	Default	Description
7	W1C	0	**Port Temperature Limit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
6:5	W1C	0	Not used.
4	W1C	0	**Port Thermal Shutdown Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
3	W1C	0	**Port Severe Short Circuit Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
2	W1C	0	**Port MPS Error (DC Disconnect) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
1	W1C	0	**Port Short Circuit Limit (I_{LIM}) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.
0	W1C	0	**Port Overload (I_{CUT}) Event**. In manual or diagnostic mode, write 1 to clear the bit. Writing 0 to this bit has no effect.

- **Port 0~1 Power Event Mask Register @ 0x78~0x79 of Page 1**

Bit #	R/W	Default	Description
7	R/W	1	**Port Temperature Limit Event Mask**. In manual mode or diagnostic mode, when mask bit is 0, no interrupt will be issued for this event.
6:5	R/W	1	Not used.
4	R/W	1	**Port Thermal Shutdown Event Mask**.
3	R/W	1	**Port Severe Short Circuit Event Mask**.
2	R/W	1	**Port MPS Error (DC Disconnect) Event Mask**.
1	R/W	1	**Port Short Circuit (I_{LIM}) Event Mask**.
0	R/W	1	**Port Overload (I_{CUT}) Event Mask**.

- **Port Interrupt Register @ 0x80 of Page 1**

Bit #	R/W	Default	Description
7:2	R	0	Not used.
1	R	0	**Port 1 Interrupt**. Port 1 has interrupt.
0	R	0	**Port 0 Interrupt**. Port 0 has interrupt.

- **Port Power Status Register @ 0x82 of Page 1**

Bit #	R/W	Default	Description
1:0	R	0x00	**Power Status of the Ports**. 0 = power off. 1 = power on. Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

- **Port MPS Present Status Register @ 0x83 of Page 1**

Bit #	R/W	Default	Description
1:0	R	0x00	**MPS Status of the Ports**. 0 = MPS not present. 1 = MPS present Bit 0 corresponds to port 0, and bit 1 corresponds to port 1, etc.

- **Port 0~1 Invalid Signature Counter Registers @ 0xB0~0xB1 of Page 1**

Bit #	R/W	Default	Description
3:0	R	0	**Invalid Signature Counter.** Number of times the port encounters an “Invalid Signature” in detection process.

- **Port 0~1 Power Denied Counter Registers @ 0xB8~0xB9 of Page 1**

Bit #	R/W	Default	Description
3:0	R	0	**Power Denied Counter.** Number of times the port encounters a “Power Denied” in classification process.

5.9 LED Interface

In auto mode or manual mode, the LED interface can hook up with an IP403 (Serial-to-Parallel LED driver) to display the port status. A port status LED is lit up when IP802 allocates power to the port

LED interface is enabled by pulling up LED_DAT pin with a resister. One IP802 can handle 2 LEDs and up to three IP802s can share one IP403, where one IP802 serves as the master to drive LED_CLK and the others are slaves. AD2 pin defines IP802 to be a master or a slave. The index counter in all IP802s counts from 0 to 55 repeatly with LED_CLK after reset and the value of index counter in all IP802 are identical. An IP802 will send out 2-bit LED information on LED_DAT when its index counter reaches start index defined in start index register (0x0B). The detail is illustrated in the LED start index register (0x0B) and figure 7.

If there is only one IP802, user can replace IP403 with a 74LV164 to display port status for cost saving. IP802 should be configured as a master.

LED Configuration Register @ 0x08 of Page 1

Bit #	R/W	Default	Description
7	R/W	0/1	**LED Interface Enable**. Enable the LED interface. 0 = disable, 1 = enable. The default value of this bit is latched from LED_DAT pin.
6:5	R	0	**Reserved**.
4	R/W	1	**LED Order**. The order in which 2-bit LED information is shifted out. 0 = Port 0, Port1, 1 = Port1, Port0 .
3	R/W	0	**LED Active Level**. 0 = light up a LED by driving logic low 1 = light up a LED by driving logic high
2	R/W	1	**LED Initial Level**. The initial level of the LED. After reset, the LED will be driven to this initial value.
1	R/W	1	**LED Clock Rate**. Clock rate of the LED clock. 0 = LED clock is 512k Hz 1 = LED clock is 1M Hz
0	R/W	0/1	**LED Master**. 0 = slave. IP802 receives LED clock on LED_CLK pin. 1 = master. IP802 drives LED_CLK pin. The default value of this bit is latched from AD2 pin.

- **LED Start Index Register @ 0x0B of Page 1**

<table>
<tr><th>Bit #</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7:6</td><td>R</td><td>0</td><td>Reserved.</td></tr>
<tr><td>5:0</td><td>R/W</td><td></td><td>LED Start Index.

There are 3 default values can be selected with I²C address pin AD2 ~ AD0. It is benefit to implement a multiple (no more than 3) IP802 LED display without software programming.
<table>
<tr><th>AD2~AD0</th><th>default value of bit [5:0]</th></tr>
<tr><td>1,x,x (master)</td><td>0x30h (48d)</td></tr>
<tr><td>0,0,0(slave)</td><td>0x28h (40d)</td></tr>
<tr><td>0,0,1(slave)</td><td>0x20h (32d)</td></tr>
<tr><td>0,1,0(slave)</td><td>0x18h (24d)</td></tr>
<tr><td>0,1,1(slave)</td><td>0x10h (16d)</td></tr>
</table>

The following table demostrates the LED applications for 1~3 IP802.
<table>
<tr><th>3 x IP802</th><th>Master</th><th>Slave1</th><th>Slave2</th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>0x20h</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>0,0,0</td><td>0,0,1</td></tr>
<tr><th>2 x IP802</th><th>Master</th><th>Slave1</th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>0x28h</td><td>--</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>0,0,0</td><td>--</td></tr>
<tr><th>1 x IP802</th><th>Master</th><th></th><th></th></tr>
<tr><td>Start index</td><td>0x30h</td><td>--</td><td>--</td></tr>
<tr><td>AD2~AD0</td><td>1,x,x</td><td>--</td><td>--</td></tr>
</table>

In manual mode, because AD0~AD2 is used for I²C address at the same time, the default setting of LED start index may be incorrect. User has to correct the LED start index by writing this register to make sure that IP802 can send out LED status correctly.

There is an alternative for LED implementation if there is a MCU in the system. The MCU reads the port status of IP802 through I²C and write the LED information to IP403, where IP403 works as a GPIO controller not a serial-to-parallel LED driver. Because LED is handled by MCU itself, the start index in IP802 can be ignored.</td></tr>
</table>

6 IP802 Register descriptions

Table 5 Register Page 0 description

Page #	Register Address and Attribute		Register Name	Default Value
I^2C Interface Registers				
0	0x00	R/W	Register Page & I^2C LSB Device Address (I^2C Addr)	(x0xx,xPPP) P: pin setting
Analog Configure and Control Registers				
0	0x01~0x24	R	Reserved (write prohibited)	-
0	0x25	R/W	AF/AT Mode	(0000,0000)
0	0x26	R	Reserved (write prohibited)	-
0	0x27	R/W	Power Down HV Analog Driver	(0000,0000)
0	0x28~0x5E	R	Reserved (write prohibited)	-
0	0x5F	R/W	Inrush Time	(0111,1110)
0	0x60~0x67	R	Reserved (write prohibited)	-
Detection Result				
0	0x68	R	R_{DET} for Port 0	(xxxx,xx00)
0	0x69	R	R_{DET} for Port 1	(xxxx,xx00)
0	0x6A~0x77	R	Reserved (write prohibited)	-
Classification Currents				
0	0x78	R	I_{CLASS} for Port 0 MSB	(xx00,0000)
0	0x79	R	I_{CLASS} for Port 0 LSB	(0000,0000)
0	0x7A	R	I_{CLASS} for Port 1 MSB	(xx00,0000)
0	0x7B	R	I_{CLASS} for Port 1 LSB	(0000,0000)
0	0x7C~0x87	R	Reserved (write prohibited)	-
Classification Results (Detected PD Classes)				
0	0x88	R	Detected PD Class Port 1 & 0	(x101,x101)
0	0x89~0x8F	R	Reserved (write prohibited)	-
PD Requested Powers				
0	0x90	R	PD 0 Requested Power	(0000,0000)
0	0x91	R	PD 1 Requested Power	(0000,0000)
0	0x92~0x9F	R	Reserved (write prohibited)	-
Port Currents				
0	0xA0	R	Port 0 Current MSB	(xxxx,0000)
0	0xA1	R	Port 0 Current LSB	(0000,0000)
0	0xA2	R	Port 1 Current MSB	(xxxx,0000)
0	0xA3	R	Port 1 Current LSB	(0000,0000)
0	0xA4~0xAF	R	Reserved (write prohibited)	-
Port Voltages				
0	0xB0	R	Port 0 Voltage MSB	(xxxx,0000)
0	0xB1	R	Port 0 Voltage LSB	(0000,0000)
0	0xB2	R	Port 1 Voltage MSB	(xxxx,0000)
0	0xB3	R	Port 1 Voltage LSB	(0000,0000)
0	0xB4~0xBF	R	Reserved (write prohibited)	-
Port Temperatures				
0	0xC0	R	Port 0 Temp. MSB	(xxx0,0000)
0	0xC1	R	Port 0 Temp. LSB	(0000,0000)
0	0xC2	R	Port 1 Temp. MSB	(xxx0,0000)
0	0xC3	R	Port 1 Temp. LSB	(0000,0000)
0	0xC4~0xDF	R	Reserved (write prohibited)	-
Supply Voltage				

Page #	Register Address and Attribute		Register Name	Default Value
0	0xE0	R	Supply Voltage MSB	(xxxx,0000)
0	0xE1	R	Supply Voltage LSB	(0000,0000)
IVT Poll Control				
0	0xE2	R/W	Force IVT Poll	(0000,0000)
0	0xE3	R/W	IVT Poll Control	(x101,1110)
0	0xE4 ~ 0xFF	R	Reserved (write prohibited)	-

Table 6 Register Page 1 description

Page #	Register Address and Attribute		Register Name	Default Value (Binary)
Register Page & I2C Interface Registers				
1	0x00	R/W	Register Page & I2C LSB Device Address (I2C Addr)	(x1xx,xPPP) P:pin setting
System Configuration & Control Registers				
1	0x01	R/W	System Configuration	(PPx0,xxxx) P:pin setting
1	0x02	R/W	System Control	(xxxx,xxx0)
1	0x03~0x07	R	Reserved (write prohibited)	-
LED Control & Configuration				
1	0x08	R/W	LED Control	(Pxx1,011P) P:PinSetting
1	0x09~0x0A	R	Reserved (write prohibited)	-
1	0x0B	R/W	LED Start Index	(PPPP,PPPP) P:PinSetting
1	0x0C~0x0F	R	Reserved (write prohibited)	-
Power Configuration				
1	0x10	R/W	Power Configuration Mode (PAM)	(0000,1000)
1	0x11	R	Reserved (write prohibited)	
1	0x12	R/W	Class 0 Port Power Limit	(0011,1110)
1	0x13	R/W	Class 1 Port Power Limit	(0001,0000)
1	0x14	R/W	Class 2 Port Power Limit	(0001,1100)
1	0x15	R/W	Class 3 Port Power Limit	(0011,1110)
1	0x16	R/W	Class 4 Port Power Limit Type 1	(0011,1110)
1	0x17	R/W	Class 4 Port Power Limit Type 2	(0111,1000)
1	0x18~0x23	R	Reserved (write prohibited)	-
1	0x24	R/W	Port Temp. Limit MSB	(xxx0,1001)
1	0x25	R/W	Port Temp. Limit LSB	(0110,0000)
1	0x26~0x3F	R	Reserved (write prohibited)	-
Power Trunk Control & Configuration				
1	0x40	R/W	Trunk 0 Power Limit MSB	(xxxx,x000)
1	0x41	R/W	Trunk 0 Power Limit LSB	(1111,1010)
1	0x42	R/W	Trunk 1 Power Limit MSB	(xxxx,x000)
1	0x43	R/W	Trunk 1 Power Limit LSB	(1111,1010)
1	0x44~0x68	R	Reserved (write prohibited)	-
1	0x69	R/W	Trunk Select	(xxxx,xx00)
1	0x6A~0x6F	R	Reserved (write prohibited)	-
Port Status				
1	0x70	R/W1C	Port 0 Status	(0000,0000)
1	0x71	R/W1C	Port 1 Status	(0000,0000)
1	0x72~0x77	R	Reserved (write prohibited)	-
1	0x78	R/W	Port 0 Status Mask	(1111,1111)
1	0x79	R/W	Port 1 Status Mask	(1111,1111)
1	0x7A~0x7F	R	Reserved (write prohibited)	-
1	0x80	R	Port Interrupt Status	(0000,0000)
1	0x81	R/W	Power Event Handle	(111x,xxxx)
1	0x82	R	Port Power Status	(0000,0000)
1	0x83	R	MPS Present Status	(0000,0000)
1	0x84~0x8F	R	Reserved (write prohibited)	-

Page #	Register Address and Attribute		Register Name	Default Value (Binary)
State Machine Control & Status				
1	0x90	R/W	Port 0 State Machine State	(00x0,0000)
1	0x91	R/W	Port 1 State Machine State	(00x0,0000)
1	0x92~0x97	R	Reserved (write prohibited)	-
1	0x98	R/W	Port 0 Power Control	(xxxx,xx00)
1	0x99	R/W	Port 1 Power Control	(xxxx,xx00)
1	0x9A~0x9F	R	Reserved (write prohibited)	-
1	0xA0	R/W	Port 1-0 Classification Event Number	(xxxx,1010)
1	0xA1	R	Reserved (write prohibited)	-
1	0xA2	R/W	PSE Skip Event 2	(xxxx,xx11)
1	0XA3~0xAF	R	Reserved (write prohibited)	-
Counter Registers				
1	0xB0	R	Port 0 Invalid Signature Count	(0000,0000)
1	0xB1	R	Port 1 Invalid Signature Count	(0000,0000)
1	0XB2~0xB7	R	Reserved (write prohibited)	-
1	0xB8	R	Port 0 Power Denied Count	(0000,0000)
1	0xB9	R	Port 1 Power Denied Count	(0000,0000)
1	0xBA~0xFF	R	Reserved (write prohibited)	-

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

(Note: Beyond these ratings can cause damage to the device)

Table 7 Electrical Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Supply Voltage	V54 – AGND	-0.3		+80	V
PortN0~PortN1	PortNn– AGND @n=0~1	-0.3		+80	V
RS0~RS1	RSn – AGND @n=0~1	-0.3		+5.5	V
V5	V5 – AGND	-0.3		+5.5	V
All other Pins	All other Pin – (AGND, or DGND)	-0.3		+3.6	V
RGND, AGND	DGND – AGND	-0.3		+0.3	V
Maximum Junction Temperature				150	℃
Storage Temperature Range		-65		150	℃
Lead Temperature	Soldering 10 seconds			300	℃
ESD at all Pins	HBM	±2			KV

7.2 Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
Ta	Ambient temperature	-40		+85	℃
V54	V54 – AGND @ AF	45	48	57	V
	V54 – AGND @ AT	51	54	57	V

7.3 Electrical Characteristics for Analog I/O Pins

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V54	Power Supply voltage	45V~57V @AF	45		57	V
		51V~57V @AT	51		57	V
I54	V54 operating current	All ports on @w/o peripheral load current & port load current		12	18	mA
V3P3	V3P3 voltage	External Capacitance=4.7uF @short V3P3 and DV3P3	3.10	3.30	3.46	V
Iout_v3p3	EnB_Reg=low	V3P3 providing to peripheral device @short V3P3 and DV3P3			6	mA
Iin_v3p3	EnB_Reg=high	External 3.3V provides to V3P3 @short V3P3 and DV3P3	6			mA
V5	Internal use only	External Capacitance=4.7uF	5	5.25	5.5	V
V2P5	Internal use only	External Capacitance=1uF	2.37	2.5	2.62	V
V54_UVL	V54 under voltage lockout	Increasing V54 – AGND		30		V
		Decreasing V54 – AGND		27		V
V54_OVL	V54 overvoltage lockout	Increasing V54 – AGND		63		V
		Decreasing V54 – AGND		60		V
V3P3_UVL	V3P3 under voltage lockout	Increasing V3P3 – AGND V3P3 – AGND @short V3P3 and DV3P3		2.8		V
V3P3_OVL	V3P3 overvoltage lockout	Decreasing V3P3 – AGND V3P3 – AGND @short V3P3 and DV3P3		1.9.		V

7.4 IEEE802.3 AF/AT Mode Parameters

Table 8 IEEE802.3 AF/AT Mode Parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Tovlrec	Auto-recovery time	From overload shutdown to next detection		1.6		s
Tudlrec	Auto-recovery time	From Imin_off shutdown to next detection		1.6		s
Tbackoff	Back-off time	Midspan mode detection back-off time		2.5		s
Iinrush	Inrush current	For t=50ms Cload=180uF max.	400	425	450	mA
Iport	Port output current	Continuous port output current after startup period AF	10		375	mA
		AT	10		640	mA
Pport	Port output power	Continuous port output power after startup period @ AF	0.57		15.4	W
		Continuous port output power after startup period @ AT	0.57		30	W
Imin_off	Port off	Must disconnect for t greater than Tmpdo	0		5	mA
Imin_onoff	Port off or on	May or may not disconnect for greater than Tmpdo	5	7.5	10	mA
Tmpdo	PD Maintenance power signature dropout time limit	AF/AT	300	350	400	ms
Tmps	PD Maintenance power signature time for validity	Port current pulse width to reset disconnect timer		49		ms
Icut	Over load current (default)	AF	350	375	400	mA
		AT	600	640	664	mA
Tcut	Over load time	Iport > Icut, AF/AT	50	62.5	75	ms
Ilim	Current limit	AF	400	425	450	mA
		AT	800	860	920	mA
Tlim	Current limit time	Iport = Ilim, AF/AT	50	62.5	75	ms
Toff	Turn off time	From VportN to V54-2.8V			500	ms
Ron	Port on resistance	Iport≦640mA, & Ta=25℃		0.3		Ω
Ioff_port	PortN leakage current	V54=54V , Ta=25℃, Port off			10	uA

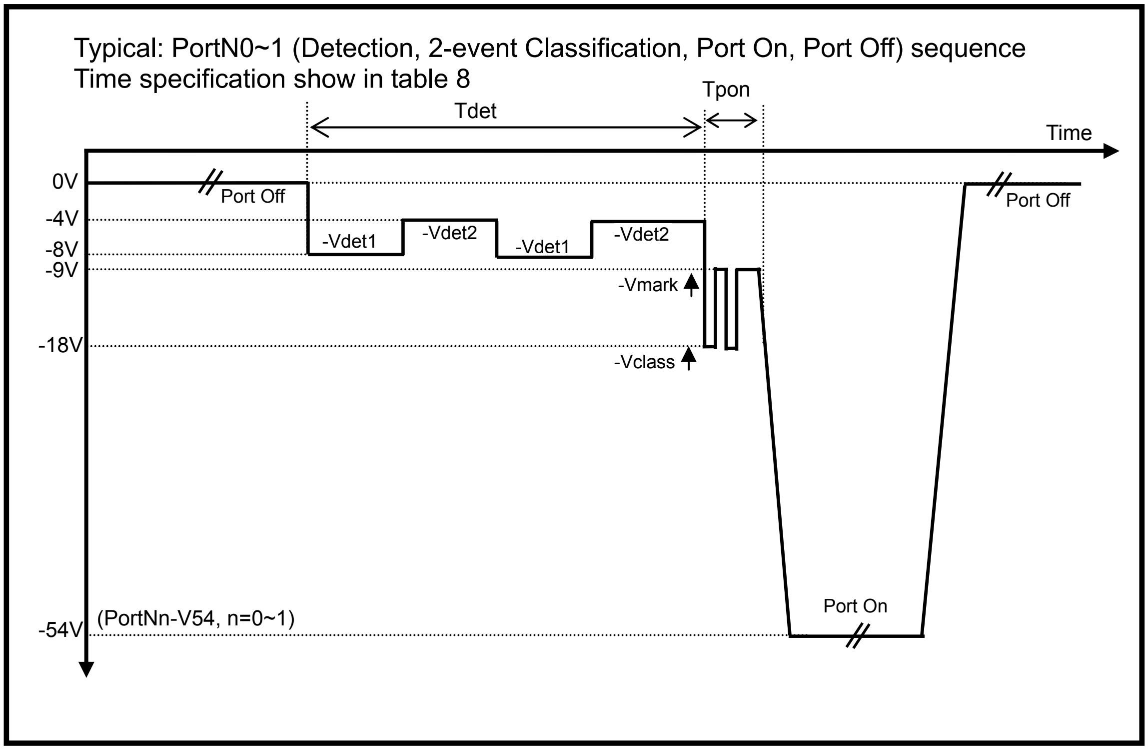


Figure 6 Typical Power up Sequence

IEEE802.3 AF/AT Mode Parameters: (continued)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Detection						
Vdet1	Detection voltage @first point	V54 – PortNn, (n=0~1) @Rdet=25KΩ	2.8	8	10	V
Vdet2	Detection voltage @second point	V54 – PortNn, (n=0~1) @Rdet=25KΩ	2.8	4	10	V
Idetlim	Detection current limit	V54=PortNn, (n=0~1)			5	mA
Tdet	Time to complete detection of a PD	AF/AT		326	500	ms
Vdet_oc	Detection port open circuit voltage	V54 – PortNn, (n=0~1) @Port open circuit			30	V
Rdet_min	Minimum Rdet detection resistance	@Cdet=0.15uF	15	17	19	KΩ
Rdet_max	Maximum Rdet detection resistance	@Cdet=0.15uF	26.5	30	33	KΩ
Rdet_open	Open circuit resistance	Rdet @Cdet=0.15uF	500			KΩ
Cdet_good	Valid Cdet detection capacitance	@Rdet=25KΩ	0		0.15	uF
Cdet_bad	Invalid Cdet detection capacitance	@Rdet=25KΩ	10			uF

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Classification						
Vclass	Classification voltage	V54 – PortNn, (n=0~1) @0mA≦Iclass≦50mA	15.5	18.0	20.5	V
Iclasslim	Classification current limitation	V54=PortNn, (n=0~1)	51		100	mA
Iclass	Classification current	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
		Invalid class	51			
Vmark	Mark voltage	V54 – PortNn, (n=0~1) @0mA≦Imark≦10mA	7	9	10	V
Imarklim	Mark current limitation	V54=PortNn, (n=0~1)	5		100	mA
Tcle	Classification event time	Width for classification event 1 or event 2	6	12	30	ms
Tme1	Mark event 1 time	Width for mark event 1	6	9	12	ms
Tme2	Mark event 2 time	Width for mark event 2	16	22		ms
Tpon	Power turn on time	From end of valid detect to application of power to port		55	400	ms
Temperature Sensor						
Tsd	Thermal shutdown	Internal temperature for thermal shutdown		150		℃
Thy	Thermal shutdown hysteresis	Internal temperature for release thermal shutdown		129		℃

7.5 Digital Electrical Characteristics

Table 9 Digital Electrical Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I²C & EEPROM interface						
VIL	Input low voltage	SCL/EE_CLK,SDAI/EE_DAT@ I²C mode, SCAN0, SCAN1			0.8	V
VIH	Input high voltage	SCL/EE_CLK,SDAI/EE_DAT@I²C mode, SCAN0, SCAN1	2.2			V
VOL	Open drain output low voltage	SCL/EE_CLK,SDAI/EE_DAT@auto mode @ Isink =5mA			0.7	V
VOL	Open drain output low voltage	SDAO,INTB,LED_CLK,LED_DAT @ Isink =5mA			0.7	V
Tscl	SCL/EE_CLK input	I²C input clock			1	MHz
Tee	SCL/EE_CLK output	Output clock for EEPROM			1	MHz
T_{SDAO}	SDAO output Delay		350			ns
T_{SDAOH}	SDAO output Hold		125			ns
T_{SDAI}	SDAI Input Setup		50			ns
T_{SDAIH}	SDAI Input Hold		50			ns
Others						
VIL	Input low voltage	AD0~AD2			0.8	V
VIH	Input high voltage	AD0~AD2	2.2			V

7.6 AC Timing

7.6.1 Power On Sequence and Reset Timing

Description	Min.	Typ.	Max.	Unit
V54_Power on time@ V54 rising time from 0v to 57v		100	-	ms
V54 stable to RstN release	200			ms
Reset to System up time			150	ms

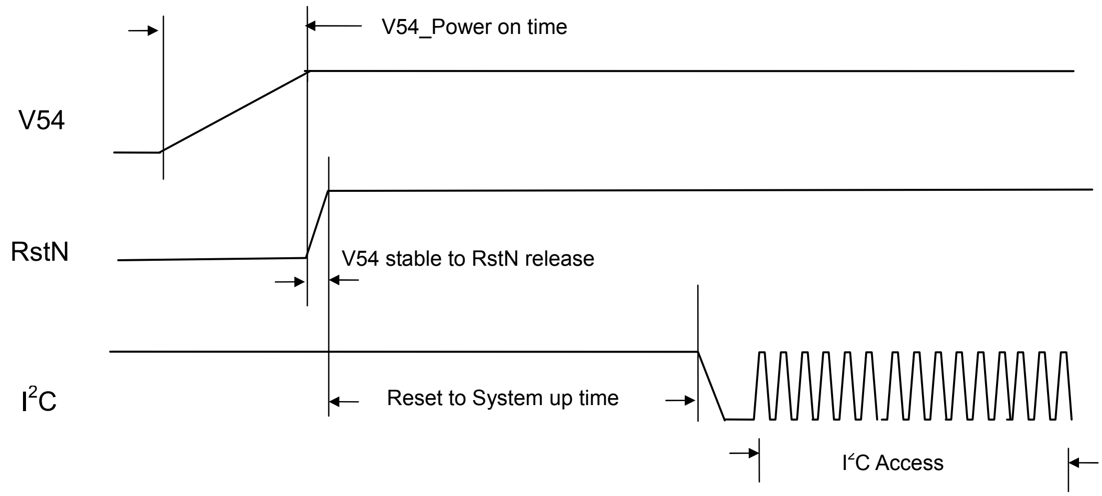


Figure 7 Power on Sequence and Reset Timing Diagram

7.6.2 EEPROM Timing

7.6.2.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns

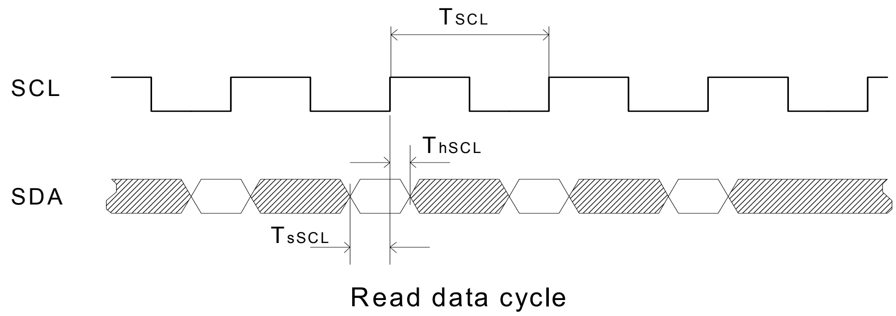


Figure 8 EEPROM Read Cycle Timing Diagram

7.6.2.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns

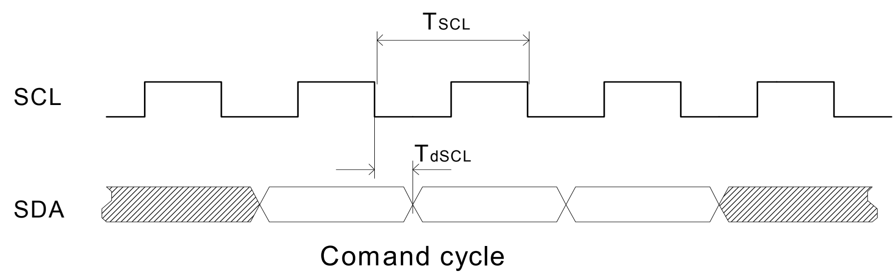


Figure 9 EEPROM Command Cycle Timing Diagram

7.6.3 I²C Timing

7.6.3.1 Data read cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	I²C clock period	1000	-	-	ns
T_{SDAO}	SDAO output delay	-	-	350	ns
T_{SDAOH}	SDAO output hold time of the last data bit	125	-	-	ns

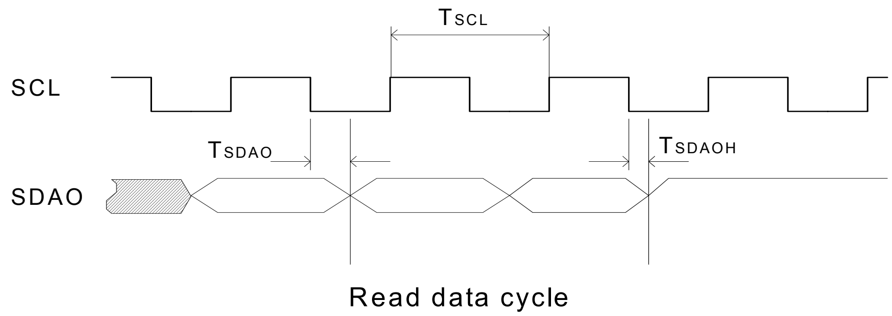


Figure 10 I²C Read Cycle Timing Diagram

7.6.3.2 Command cycle

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	I²C clock period	1000	-	-	ns
T_{SDAI}	SDAI setup time	50	-	-	ns
T_{SDAIH}	SDAI hold time	50	-	-	ns

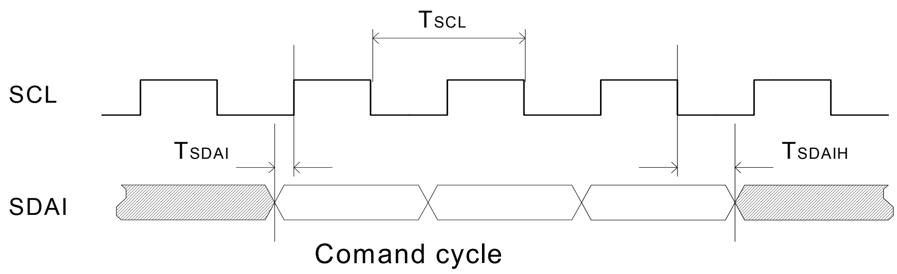


Figure 11 I²C Command Cycle Timing Diagram

7.7 Thermal Data

θ_{JA}	θ_{JC}	Ψ_{JT}	Conditions	Units
21	9.6	0.47	4 Layer PCB	°C/W

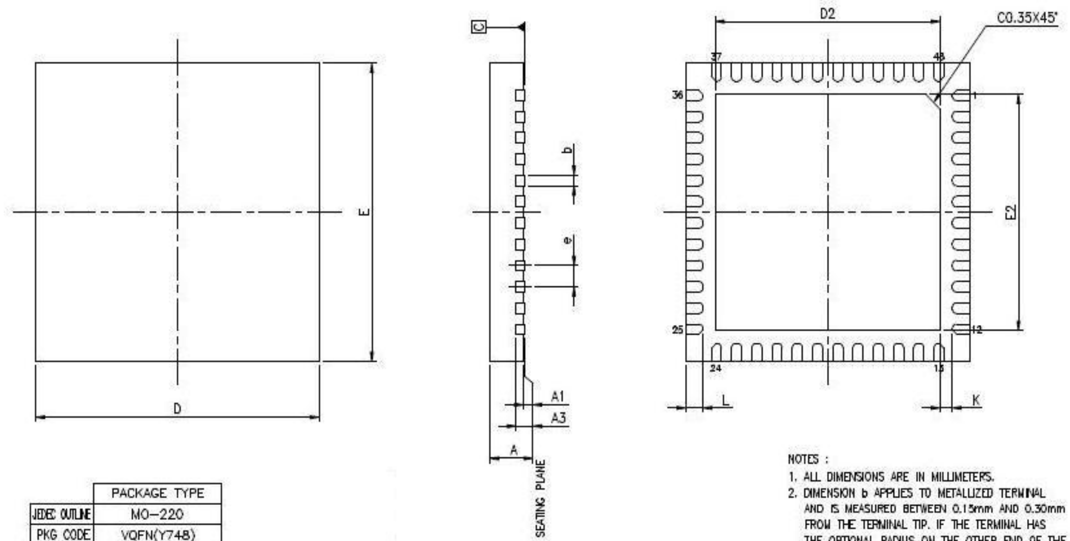
8 Order Information

Table 10 Order Information

Part No.	Package	Operating Temperature	Notice
IP802	48-Lead MQFN	-40°C to 85°C	

9 Package Detail

9.1 48 MQFN Outline Dimensions (in mm)



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y748)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
K	0.20	—	—

	D2			E2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.20	5.30	5.40	5.20	5.30	5.40	0.35	0.40	0.45	V	X	N/A

Figure 12 Package Outline Dimensions

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