# Power MOSFET

## 20 V, 285 mA, P−Channel with ESD Protection, SOT−723

LNTK3043PT5G
S-LNTK3043PT5G

### Features

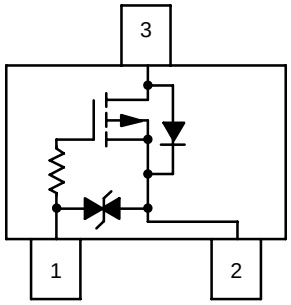
- Enables High Density PCB Manufacturing
- 44% Smaller Footprint than SC−89 and 38% Thinner than SC−89
- Low Voltage Drive Makes this Device Ideal for Portable Equipment
- Low Threshold Levels, $V_{GS(TH)}$ < 1.3 V
- Low Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels Using the Same Basic Topology
- These are Pb−Free Devices
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

### Applications

- Interfacing, Switching
- High Speed Switching
- Cellular Phones, PDAs

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ Max |
|---|---|---|
| 20 V | 1.5 Ω @ 4.5 V | 285 mA |
| | 2.4 Ω @ 2.5 V | |
| | 5.1 Ω @ 1.8 V | |
| | 6.8 Ω @ 1.65 V | |

Top View




1 − Gate
2 − Source
3 − Drain

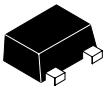
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

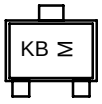
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 20 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±10 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 255 | mA |
| | | $T_A$ = 85°C | | 185 | |
| | t ≤ 5 s | $T_A$ = 25°C | | 285 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 440 | mW |
| | t ≤ 5 s | | | 545 | |
| Continuous Drain Current (Note 2) | Steady State | $T_A$ = 25°C | $I_D$ | 210 | mA |
| | | $T_A$ = 85°C | | 155 | |
| Power Dissipation (Note 2) | | $T_A$ = 25°C | $P_D$ | 310 | mW |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | 400 | mA |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) (Note 2) | | | $I_S$ | 286 | mA |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds) | | | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
2. Surface−mounted on FR4 board using the minimum recommended pad size.

**MARKING DIAGRAM**






**SOT−723**
**CASE 631AA**

KB = Device Code
M = Date Code

**ORDERING INFORMATION**

| Device | Package | Shipping † |
|---|---|---|
| LNTK3043PT5G<br>S-LNTK3043PT5G | SOT−723* | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*These packages are inherently Pb−Free.

## THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 280 | °C/W |
| Junction−to−Ambient – t = 5 s (Note 3) | $R_{\theta JA}$ | 228 | |
| Junction−to−Ambient – Steady State Minimum Pad (Note 4) | $R_{\theta JA}$ | 400 | |

3. Surface−mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)
4. Surface−mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise specified)

| Parameter | Test Condition | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 100 μA | | $V_{(BR)DSS}$ | 20 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $I_D$ = 100 μA, Reference to 25°C | | $V_{(BR)DSS}/T_J$ | | 27 | | mV/°C |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 16 V | $T_J$ = 25°C | $I_{DSS}$ | | | 1 | μA |
| | | $T_J$ = 125°C | | | | 10 | |
| Gate−to−Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = ±5 V | | $I_{GSS}$ | | | 1 | μA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | $V_{GS(TH)}$ | 0.4 | | 1.3 | V |
| Gate Threshold Temperature Coefficient | | | $V_{GS(TH)}/T_J$ | | −2.4 | | mV/°C |
| Drain−to−Source On Resistance | $V_{GS}$ = 4.5V, $I_D$ = 10 mA | | $R_{DS(ON)}$ | | 1.5 | 3.4 | Ω |
| | $V_{GS}$ = 4.5V, $I_D$ = 255 mA | | | | 1.6 | 3.8 | |
| | $V_{GS}$ = 2.5 V, $I_D$ = 1 mA | | | | 2.4 | 4.5 | |
| | $V_{GS}$ = 1.8 V, $I_D$ = 1 mA | | | | 5.1 | 10 | |
| | $V_{GS}$ = 1.65 V, $I_D$ = 1 mA | | | | 6.8 | 15 | |
| Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 100 mA | | $g_{FS}$ | | 0.275 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 10 V | | $C_{ISS}$ | | 11 | | pF |
| Output Capacitance | | | $C_{OSS}$ | | 8.3 | | |
| Reverse Transfer Capacitance | | | $C_{RSS}$ | | 2.7 | | |
| **SWITCHING CHARACTERISTICS, VGS= 4.5 V** (Note 4) | | | | | | | |
| Turn−On Delay Time | $V_{GS}$ = 4.5 V, $V_{DD}$ = 5 V, $I_D$ = 10 mA, $R_G$ = 6 Ω | | $t_{d(ON)}$ | | 13 | | ns |
| Rise Time | | | $t_r$ | | 15 | | |
| Turn−Off Delay Time | | | $t_{d(OFF)}$ | | 94 | | |
| Fall Time | | | $t_f$ | | 55 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{GS}$ = 0 V, $I_S$= 286 mA | $T_J$ = 25°C | $V_{SD}$ | | 0.83 | 1.2 | V |
| | | $T_J$ = 125°C | | | 0.69 | | |
| Reverse Recovery Time | $V_{GS}$ = 0 V, $V_{DD}$ = 20 V, dISD/dt = 100 A/μs, $I_S$ = 286 mA | | $t_{RR}$ | | 9.1 | | ns |
| Charge Time | | | $t_a$ | | 7.1 | | |
| Discharge Time | | | $t_b$ | | 2.0 | | |
| Reverse Recovery Charge | | | $Q_{RR}$ | | 3.7 | | nC |

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

## LNTK3043PT5G , S-LNTK3043PT5G

### TYPICAL PERFORMANCE CURVES

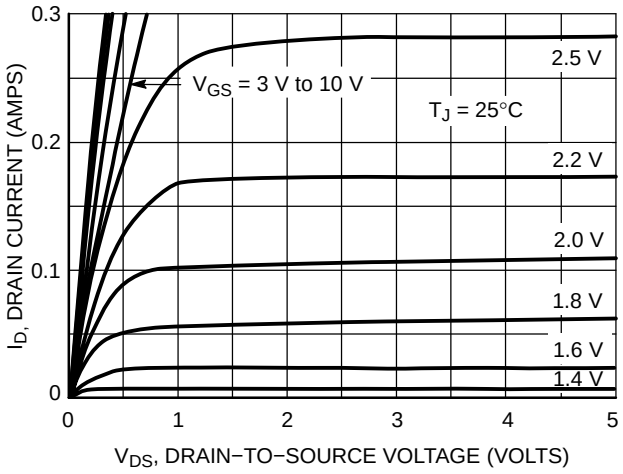



**Figure 1. On−Region Characteristics**

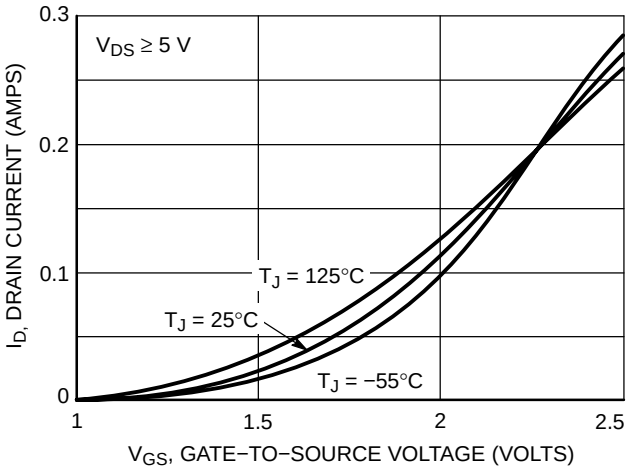



**Figure 2. Transfer Characteristics**

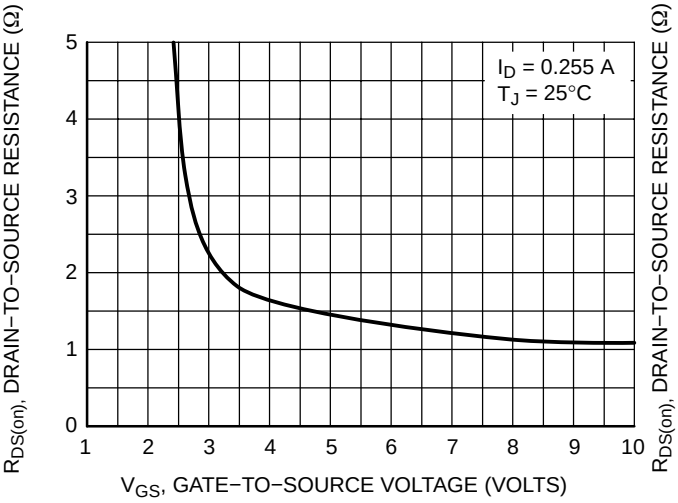



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

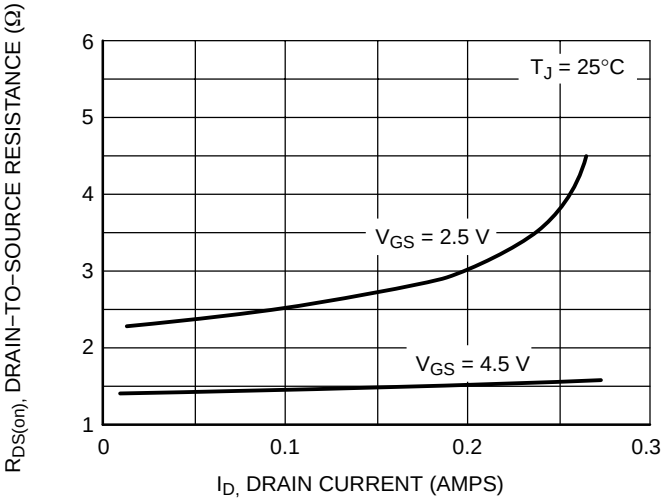



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

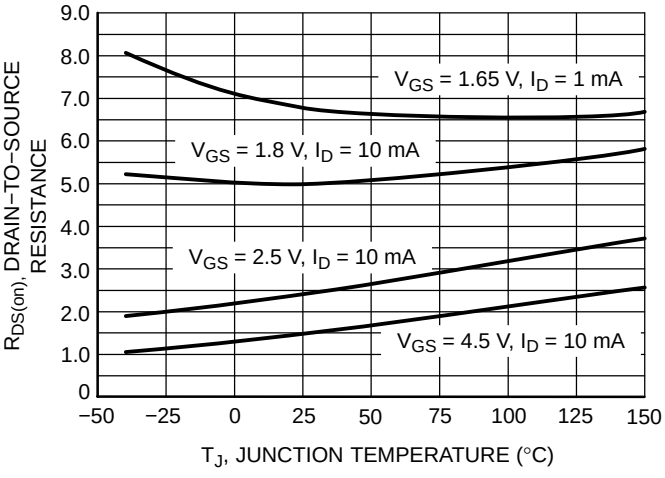



**Figure 5. On−Resistance Variation with Temperature**

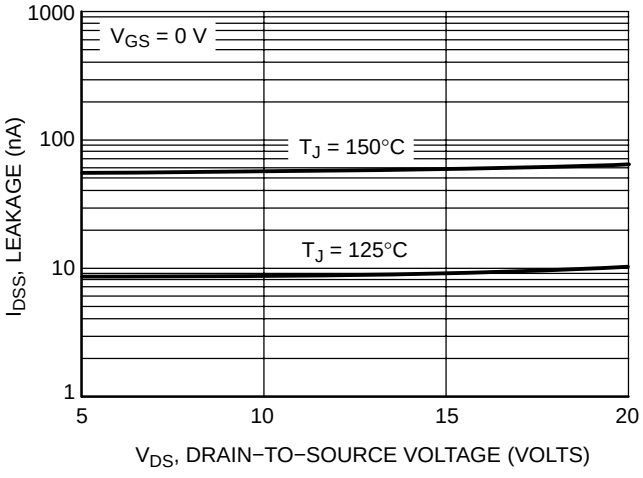



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL PERFORMANCE CURVES

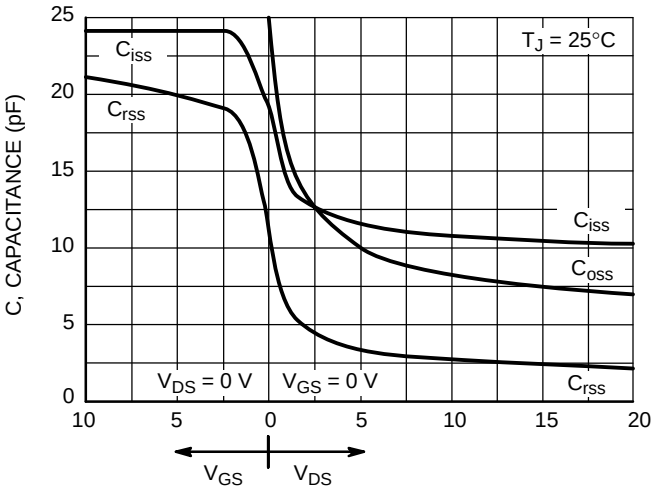



**Figure 7. Capacitance Variation**

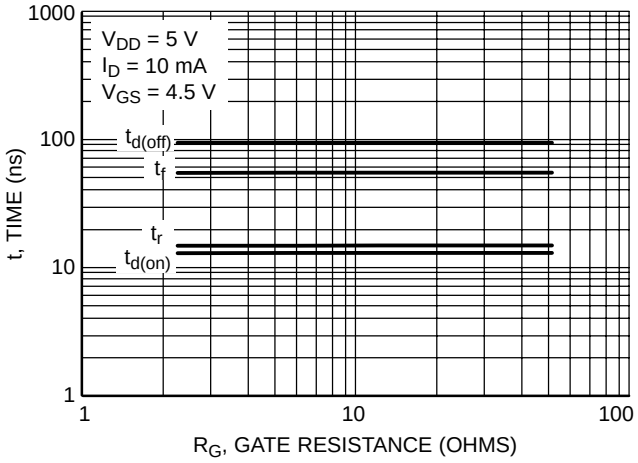



**Figure 8. Resistive Switching Time Variation vs. Gate Resistance**

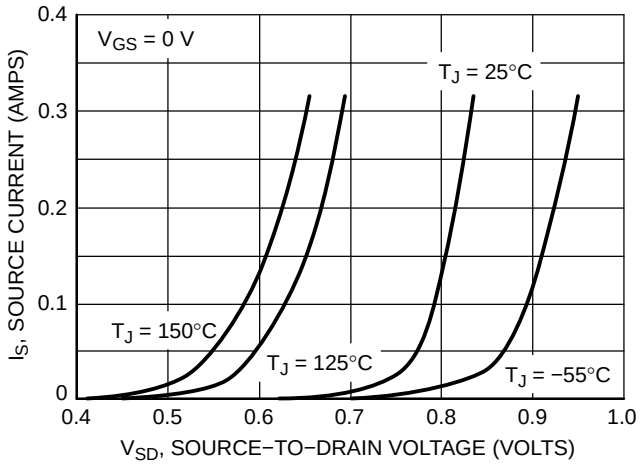
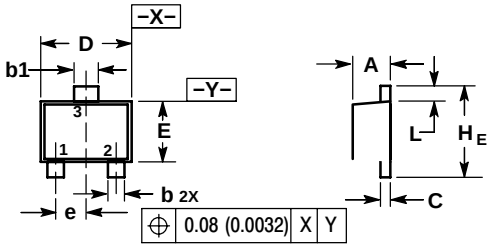



**Figure 9. Diode Forward Voltage vs. Current**

## PACKAGE DIMENSIONS

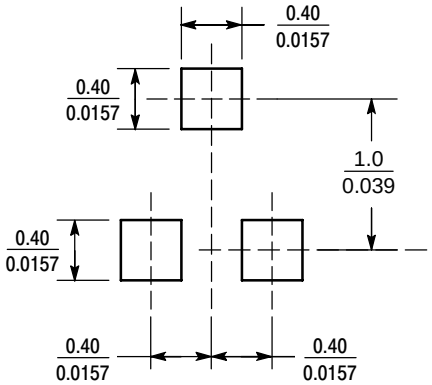
### SOT−723




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| b | 0.15 | 0.21 | 0.27 | 0.0059 | 0.0083 | 0.0106 |
| b1 | 0.25 | 0.31 | 0.37 | 0.010 | 0.012 | 0.015 |
| C | 0.07 | 0.12 | 0.17 | 0.0028 | 0.0047 | 0.0067 |
| D | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| E | 0.75 | 0.80 | 0.85 | 0.03 | 0.032 | 0.034 |
| e | | 0.40 BSC | | | 0.016 BSC | |
| $H_E$ | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| L | 0.15 | 0.20 | 0.25 | 0.0059 | 0.0079 | 0.0098 |

## SOLDERING FOOTPRINT*




SCALE 20:1 (mm / inches)