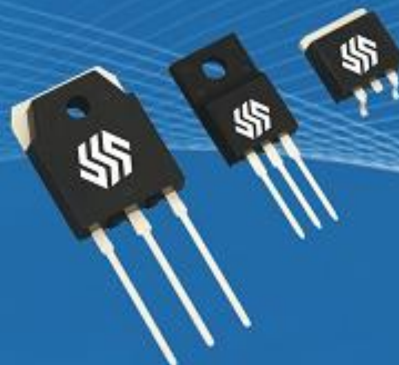
SUPER-SEMI



SUPER-MOSFET

Super Junction Metal Oxide Semiconductor Field Effect Transistor

800V Super Junction Power MOSFET
SS*80R500S

Rev. 1.6
Aug. 2019

www.supersemi.com.cn

September, 2013

SJ-FET

SSF80R500S/SSP80R500S/SSB80R500S/SST80R500S 800V N-Channel MOSFET

Description

SJ-FET is new generation of high voltage MOSFET family that is utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.
This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.
SJ-FET is suitable for various AC/DC power conversion in switching mode operation for higher efficiency.

Features

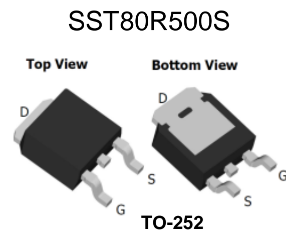
- Multi-Epi process SJ-FET
- 850V @TJ = 150 ℃
- Typ. RDS(on) = 0.48Ω
- Ultra Low Gate Charge (typ. Qg = 13nC)
- 100% avalanche tested

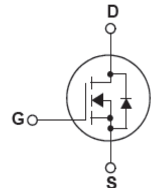
SSF80R500S

SSP80R500S

SSB80R500S

SST80R500S





Absolute Maximum Ratings

Symbol	Parameter	SSP_B_T80R500S	SSF80R500S	Unit
V_{DSS}	Drain-Source Voltage	800		V
I_D	Drain Current -Continuous (TC = 25℃) -Continuous (TC = 100℃)	10.5* 6.7*		A
I_{DM}	Drain Current - Pulsed (Note 1)	30*		A
V_{GSS}	Gate-Source voltage	±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	210		mJ
I_{AR}	Avalanche Current (Note 1)	1.8		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.32		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	15		V/ns
dVds/dt	Drain Source voltage slope (Vds=640V)	50		V/ns
P_D	Power Dissipation (TC = 25℃)	83	31	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		℃

* Drain current limited by maximum junction temperature. Maximum duty cycle D=0.75.

Thermal Characteristics

Symbol	Parameter	SSP_B_T80R500S	SSF80R500S	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	4.0	℃/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	-	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	80	℃/W

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Electrical Characteristics TC = 25℃ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA, T_J = 25℃	800	-	-	V
		V_{GS} = 0V, I_D = 250μA, T_J = 150℃	-	850	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25℃	-	0.6	-	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800V, V_{GS} = 0V -T_J = 150℃	-	- 10	1 -	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 5.5A (TO-220F/TO-220/TO-263)	-	0.48	0.52	Ω
		V_{GS} = 10V, I_D = 5.5A (TO-252)	-	0.51	0.55	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40V, I_D = 11A	-	9	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	630	-	pF
C_{oss}	Output Capacitance		-	180	-	pF
C_{rss}	Reverse Transfer Capacitance		-	11	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400V, I_D = 5.5A, R_G = 25Ω (Note 4)	-	28	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	65	-	ns
t_f	Turn-Off Fall Time		-	19	-	ns
Q_g	Total Gate Charge	V_{DS} = 450V, I_D = 5.5A, V_{GS} = 10V (Note 4)	-	13	-	nC
Q_{gs}	Gate-Source Charge		-	3.4	-	nC
Q_{gd}	Gate-Drain Charge		-	4.9	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	30	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 11A	-	0.9	1.5	V
t_{rr}	Reverse Recovery Time	V_R = 400V, V_{GS} = 0V, I_F = 11A, dI_F/dt = 100A/μs	-	600	-	ns
Q_{rr}	Reverse Recovery Charge		-	7.2	-	μC
I_{rrm}	Peak reverse recovery Current		-	22	-	A

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS}=1.8A, VDD=50V, Starting TJ=25 ℃
3. I_{SD}≤ID, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting TJ = 25 ℃
4. Essentially Independent of Operating Temperature Typical Characteristics

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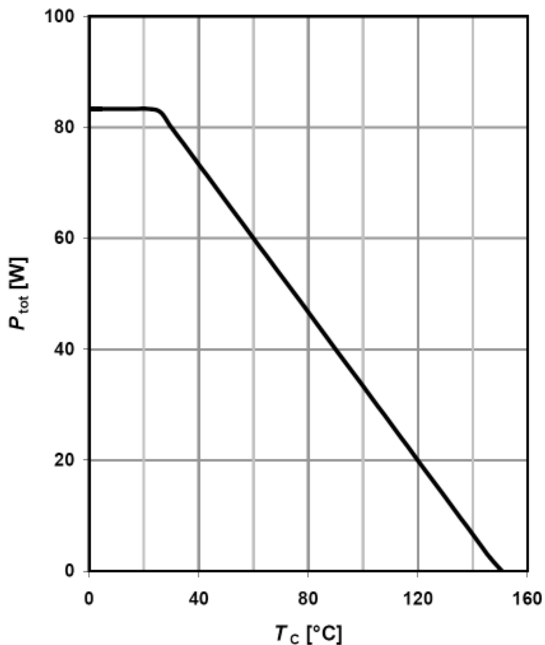
Typical Performance Characteristics

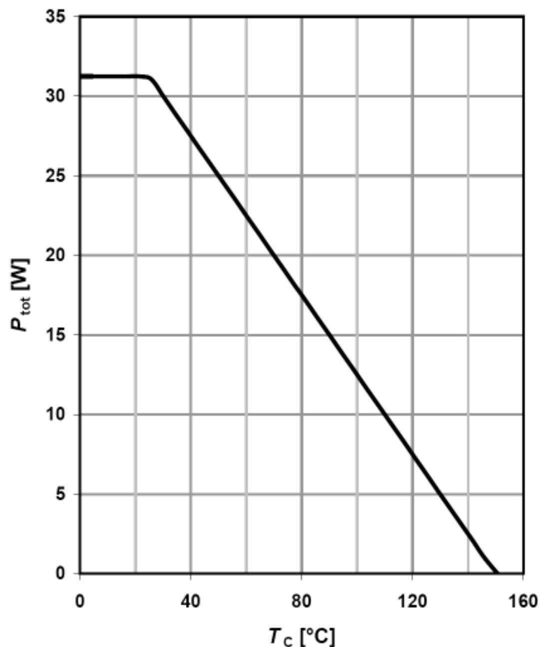
Power dissipation

$P_{tot}=f(T_C)$; TO-220,TO-252,TO-263



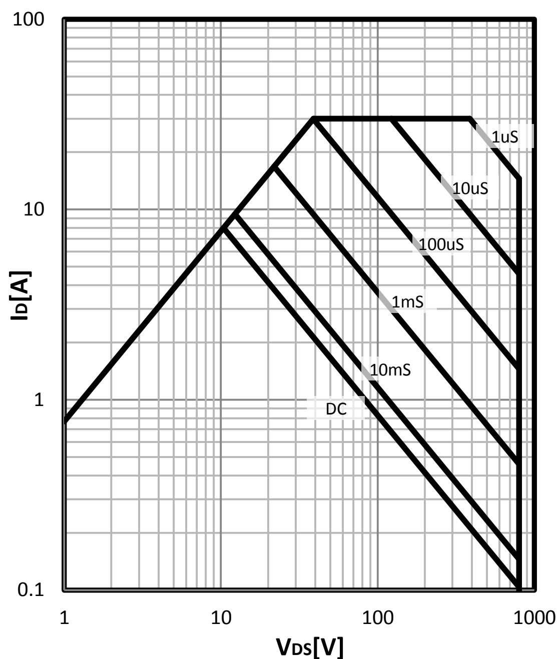
Power dissipation

$P_{tot}=f(T_C)$; TO-220FullPAK



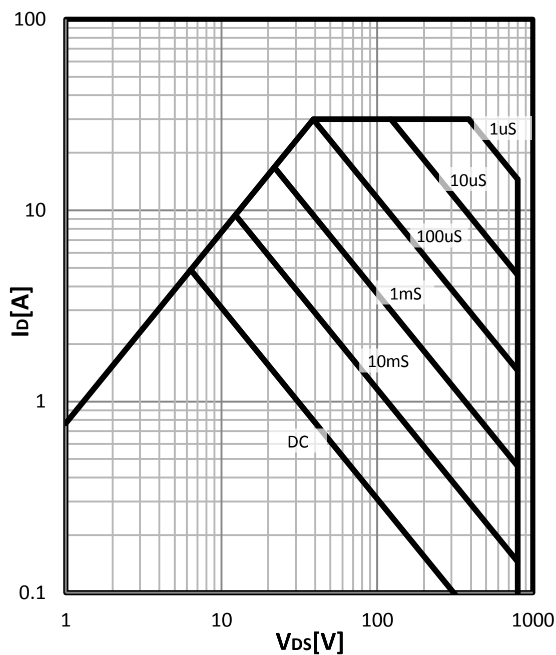
Safe Operating area Tc=25℃

$I_D=f(V_{DS})$; D=0; parameter t_p ; TO-220,TO-252,TO-263



Safe Operating area Tc=25℃

$I_D=f(V_{DS})$; D=0; parameter $t_{p,}$; TO-220FullPAK



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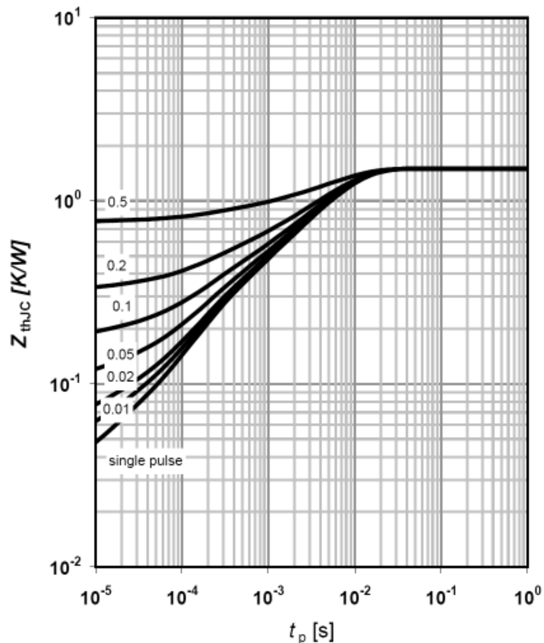
Typical Performance Characteristics

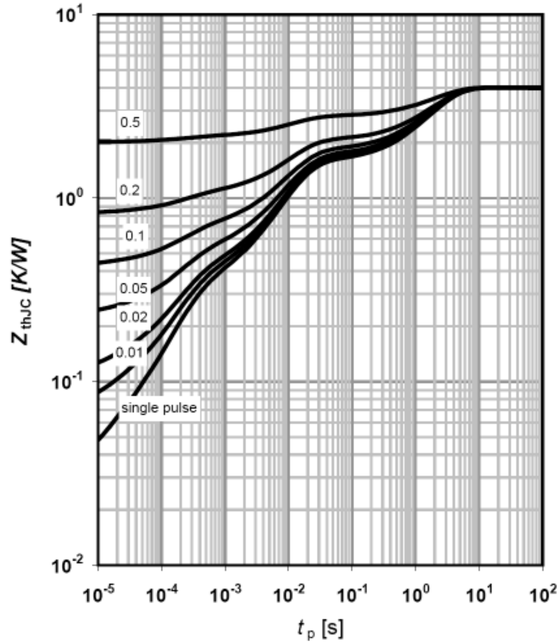
Max. Transient thermal impedance

$Z_{(thJC)}$=f(tp);Parameter: D=t_p/T; TO-220,TO-252,TO-263



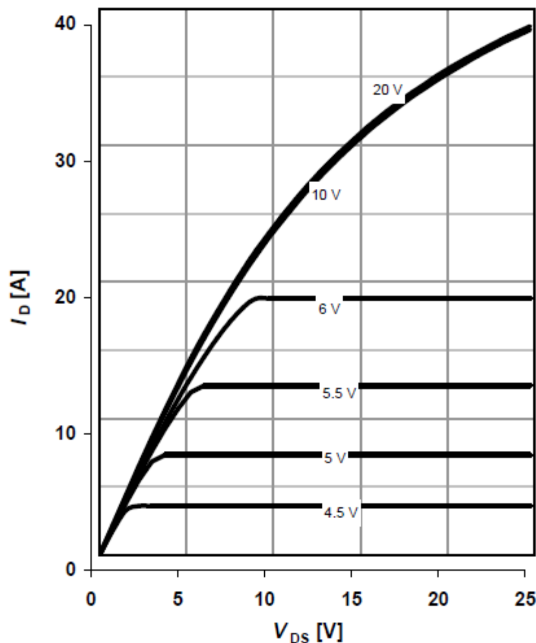
Max. Transient thermal impedance

$Z_{(thJC)}$=f(tp);Parameter: D=t_p/T; TO-220FullPAK



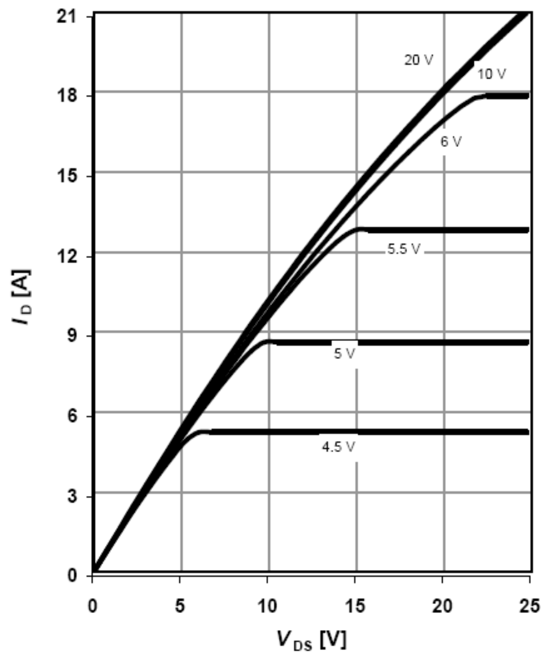
Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C; t_p=10 µs; parameter: V_{GS}



Typ. output characteristics

I_D=f(V_{DS}); T_j=150 °C; t_p=10 µs; parameter: V_{GS}



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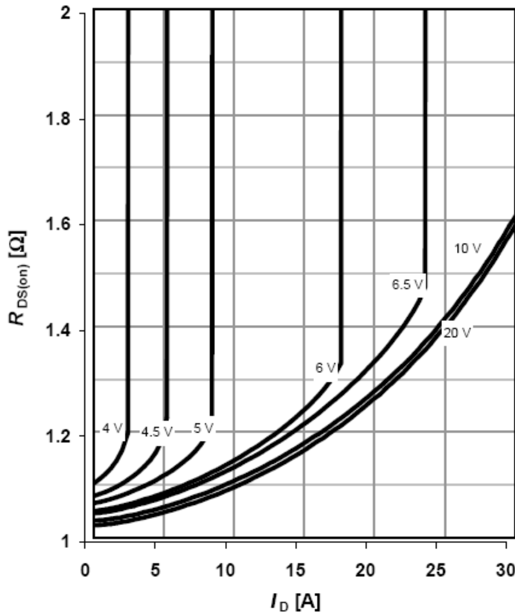
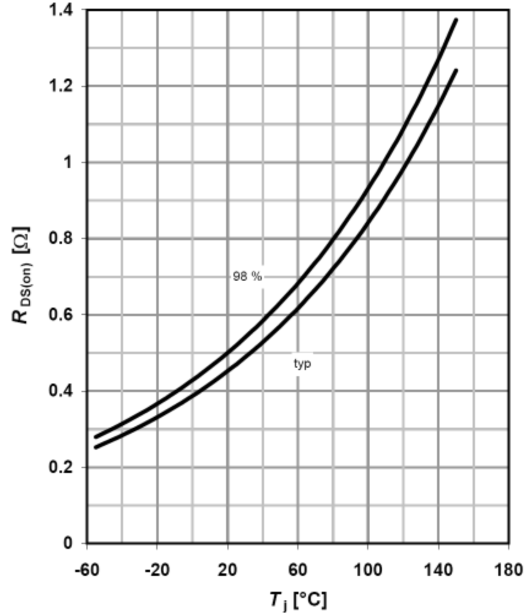
Typ. drain-source on-state resistance

RDS(on)=f(I D); T j=150 °C; parameter: VGS



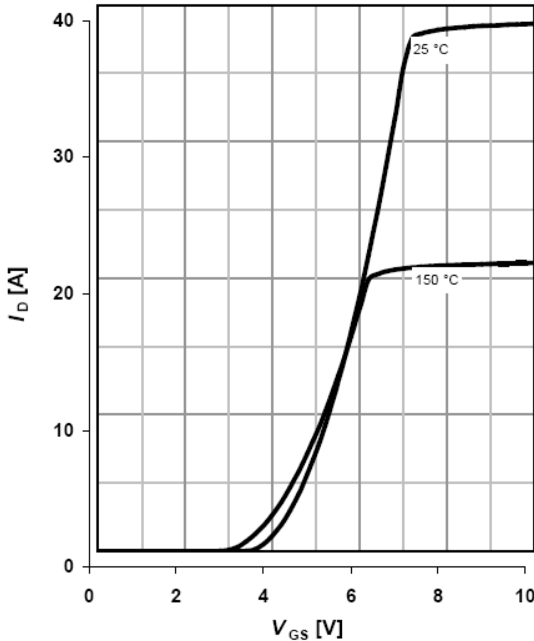
Drain-source on-state resistance

RDS(on)=f(T j); ID=5.5A; VGS=10V



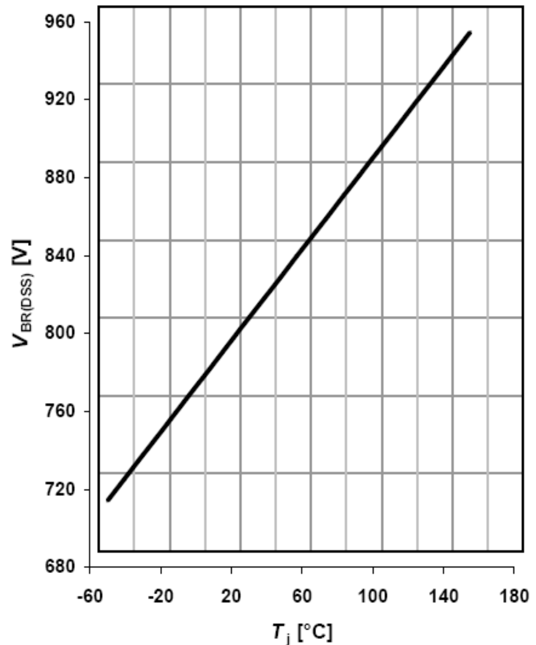
Typ. transfer characteristics

ID=f(VGS); |VDS|>2|ID|RDS(on)max; tp=10μs; parameter: Tj



Drain-source breakdown voltage

VBR(DSS)=f(T j); ID=0.25 mA



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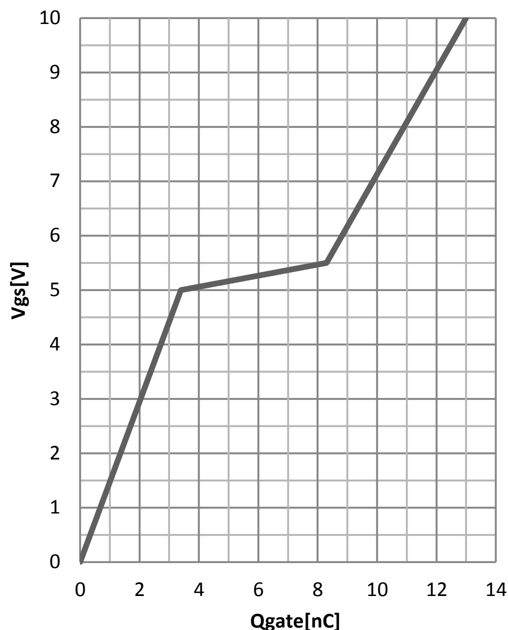
Typical Performance Characteristics

SSF80R500S/SSP80R500S/SSB80R500S/SST80R500S 800VN-Channel MOSFET

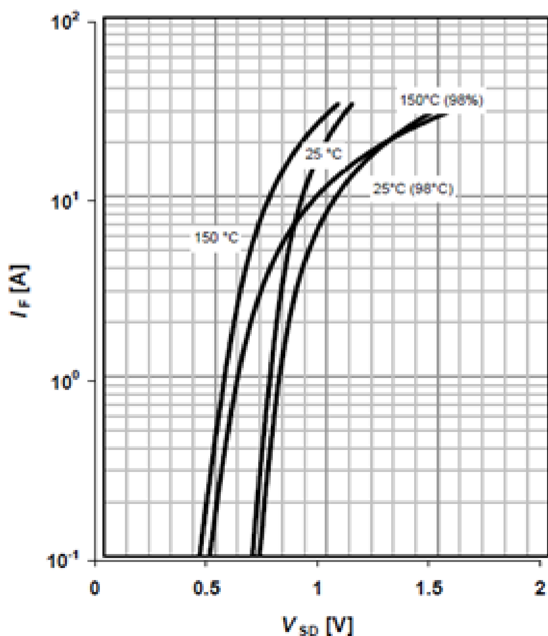
Typ. Gate charge

V_{GS}=f(Q_{gate}); I_D=5.5A pulsed



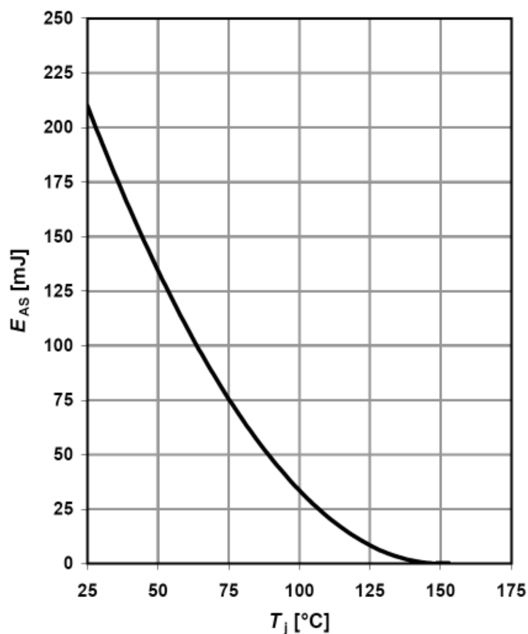
Forward characteristics of reverse diode

I_F=f(V_{DS}); parameter: T_j



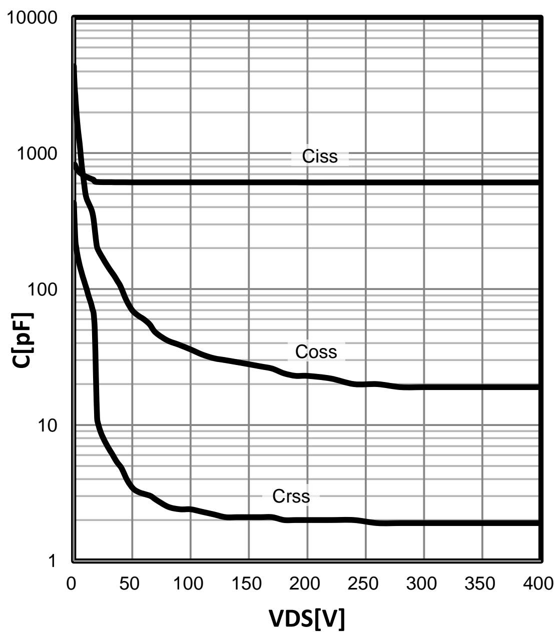
Avalanche energy

E_{AS}=f(T_j); V_{DD}=50V



Typ. Capacitances

C=f(V_{DS}); V_{GS}=0 V; f =1 MHz



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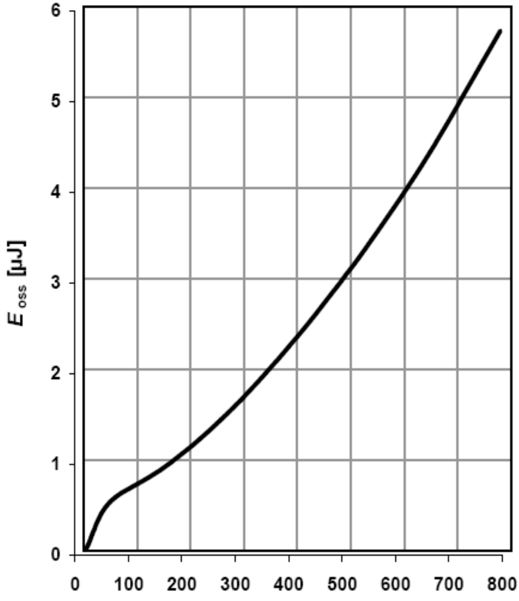
Typical Performance Characteristics

Typ. Coss stored energy

*E*oss= f(*V*DS)



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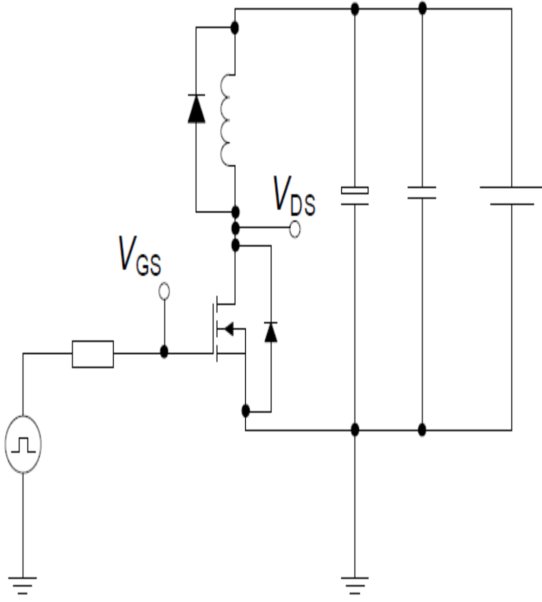
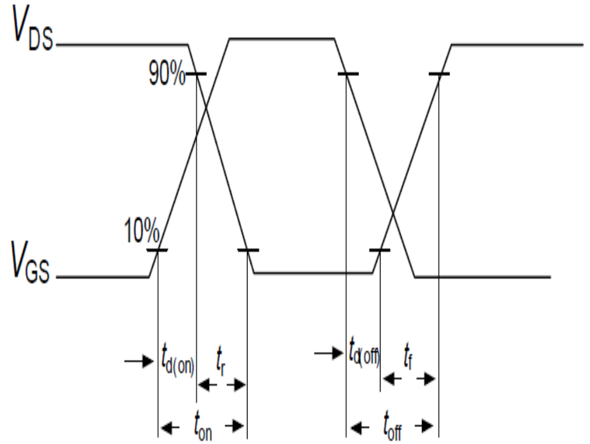
Test circuits

Switching times test circuit and waveform for inductive load

Switching times test circuit for inductive load

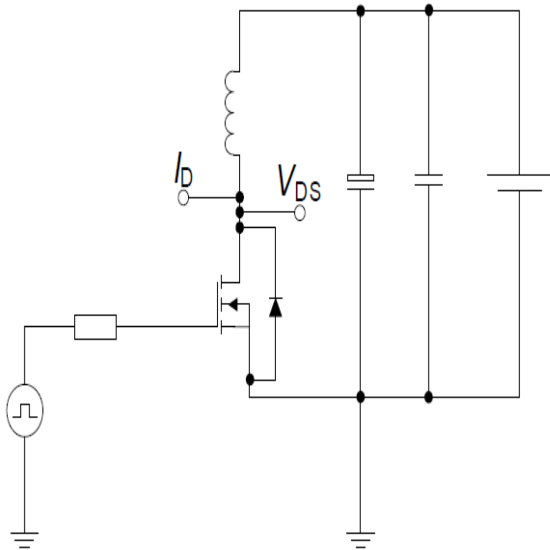


Switching time waveform

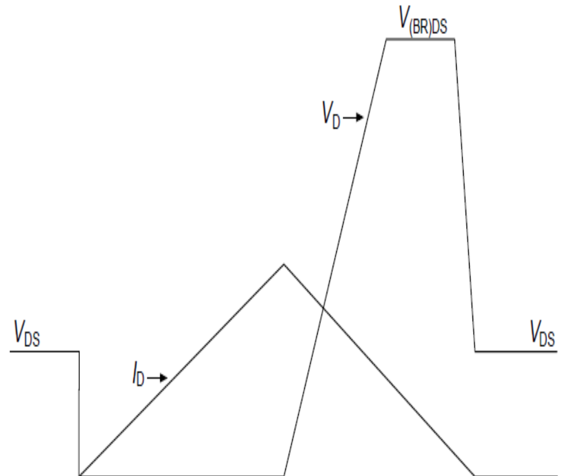


Unclamped inductive load test circuit and waveform

Unclamped inductive load test circuit



Unclamped inductive waveform



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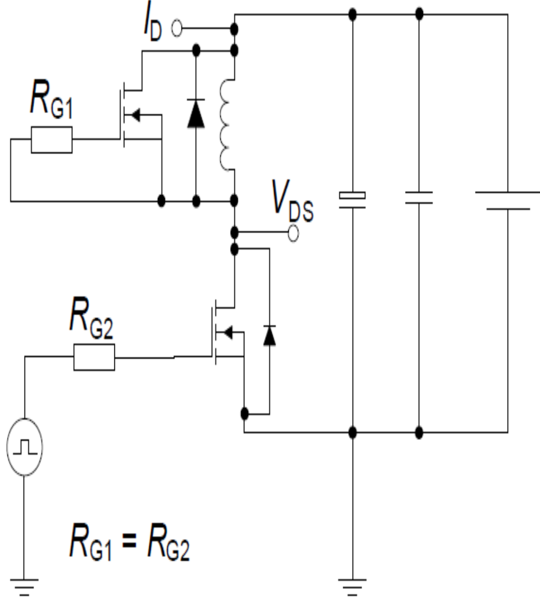
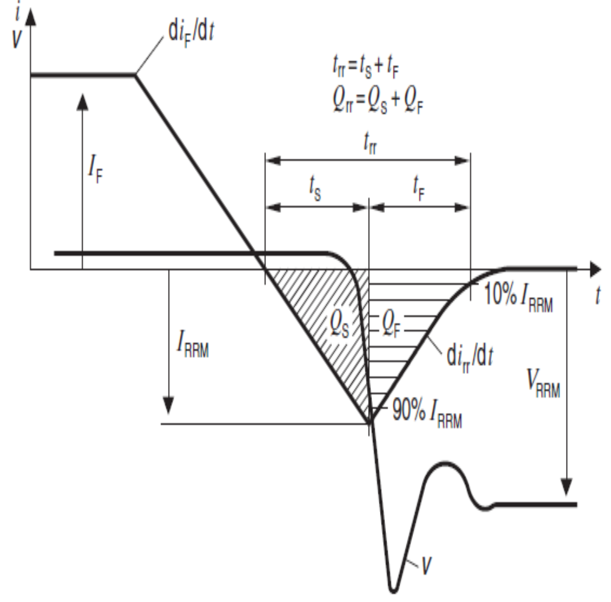
Test circuits

Test circuit and waveform for diode characteristics

Test circuit for diode characteristics

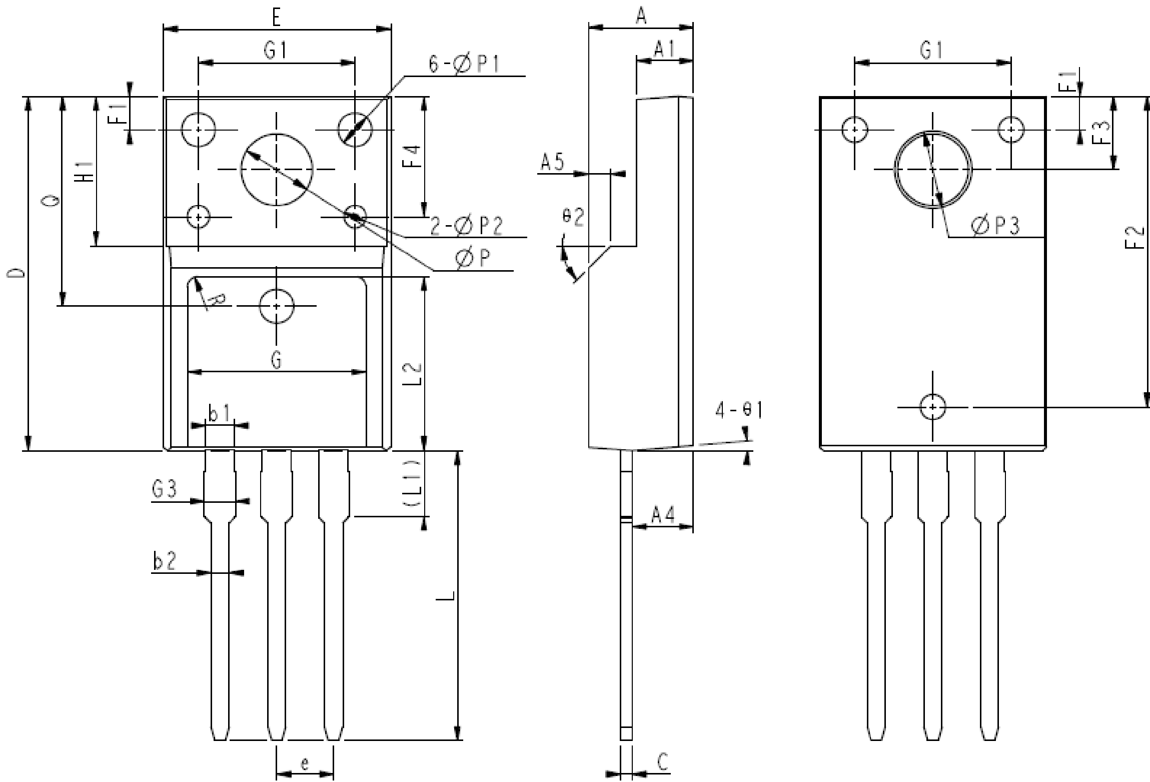


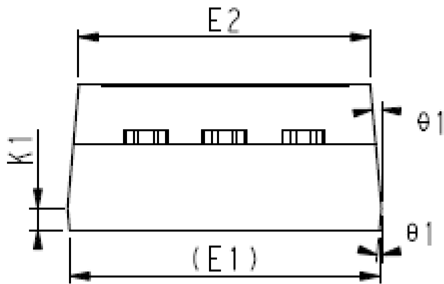
Diode recovery waveform



Package Outline

TO-220 Full PAK





COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
E	10.00	10.16	10.32
E1	9.94	10.04	10.14
E2	9.36	9.46	9.56
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A4	2.66	2.76	2.86
A5		1.00REF	
c	0.45	0.50	0.60
D	15.67	15.87	16.07
Q		9.40REF	
H1		6.70REF	
e		2.54BSC	
ΦP		3.18REF	
L	12.78	12.98	13.18
L1	2.83	2.93	3.03
L2	7.70	7.80	7.90
ΦP1	1.40	1.50	1.60
ΦP2	0.95	1.00	1.05
ΦP3		3.45REF	
θ1	3°	5°	7°
θ2	-	45°	-
F1	1.00	1.50	2.00
F2	13.80	13.90	14.00
F3	3.20	3.30	3.40
F4	5.30	5.40	5.50
G	7.80	8.00	8.20
G1	6.90	7.00	7.10
G3	1.25	1.35	1.45
b1	1.23	1.28	1.38
b2	0.75	0.80	0.90
K1	0.65	0.70	0.75
R		0.50REF	

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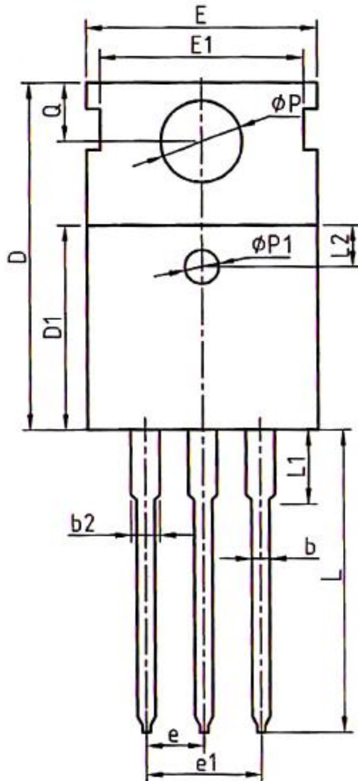
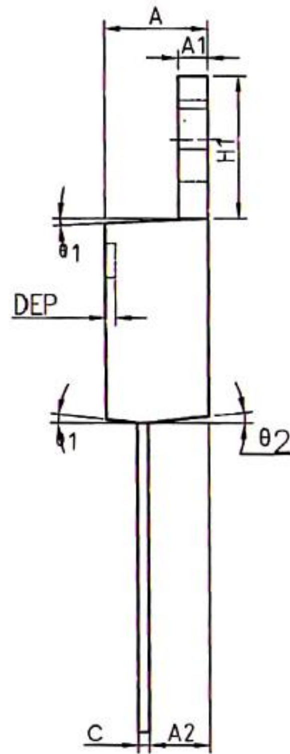
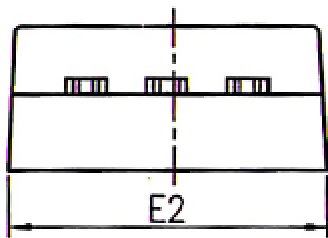
Package Outline

TO-220







COMMON DIMENIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.40	4.57	4.70
A1	1.27	1.30	1.37
A2	2.35	2.40	2.50
b	0.77	0.80	0.90
b2	1.17	1.27	1.36
c	0.48	0.50	0.56
D	15.40	15.60	15.80
D1	9.00	9.10	9.20
DEP	0.05	0.10	0.20
E	9.80	10.00	10.20
E1	–	8.70	–
E2	9.80	10.00	10.20
ØP1	1.40	1.50	1.60
e		2.54BSC	
e1		5.08BSC	
H1	6.40	6.50	6.60
L	12.75	13.50	13.65
L1	–	3.10	3.30
L2		2.50REF	
ØP	3.50	3.60	3.63
Q	2.73	2.80	2.87
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	1°	3°	5°

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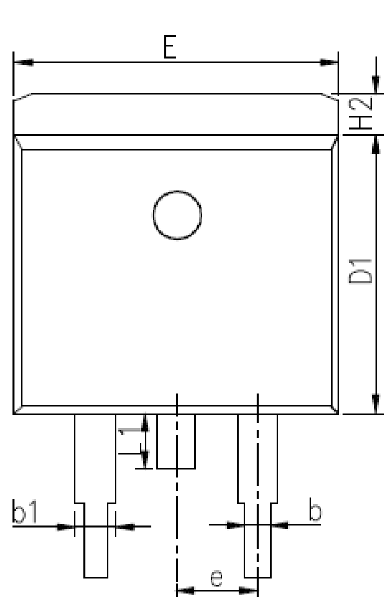
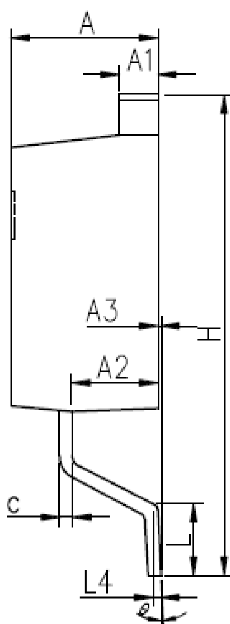
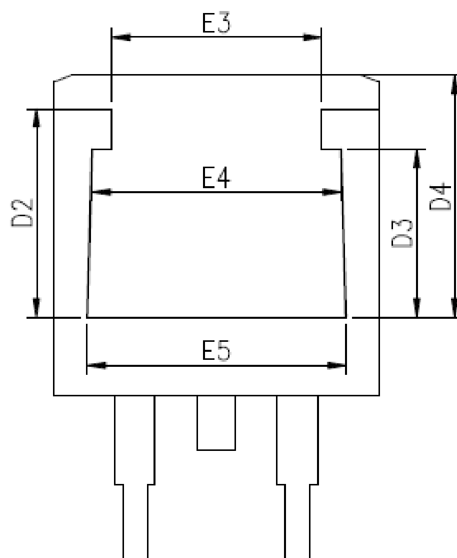
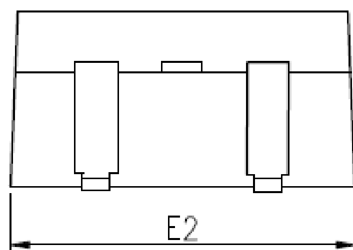
Package Outline

TO-263









COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.27	4.57	4.87
A1	1.22	1.27	1.42
A2	2.39	2.69	2.99
A3	0.00	0.13	0.20
b	0.70	0.81	1.01
b1	1.17	1.27	1.50
c	0.30	0.38	0.53
D1	8.40	8.70	9.00
D2	5.33	6.33	6.63
D3	4.54	5.54	5.84
D4	6.60	7.60	8.00
E	9.88	10.16	10.50
E2	9.80	10.10	10.40
E3	4.94	5.94	6.24
E4	6.67	7.67	7.97
E5	7.06	8.06	8.36
e	2.54 BSC		
H	14.70	15.10	15.50
H2	1.00	1.27	1.50
L	2.00	2.30	2.60
L1	1.35	1.55	1.75
L4	0.25 BSC		
θ	0°	5°	9°

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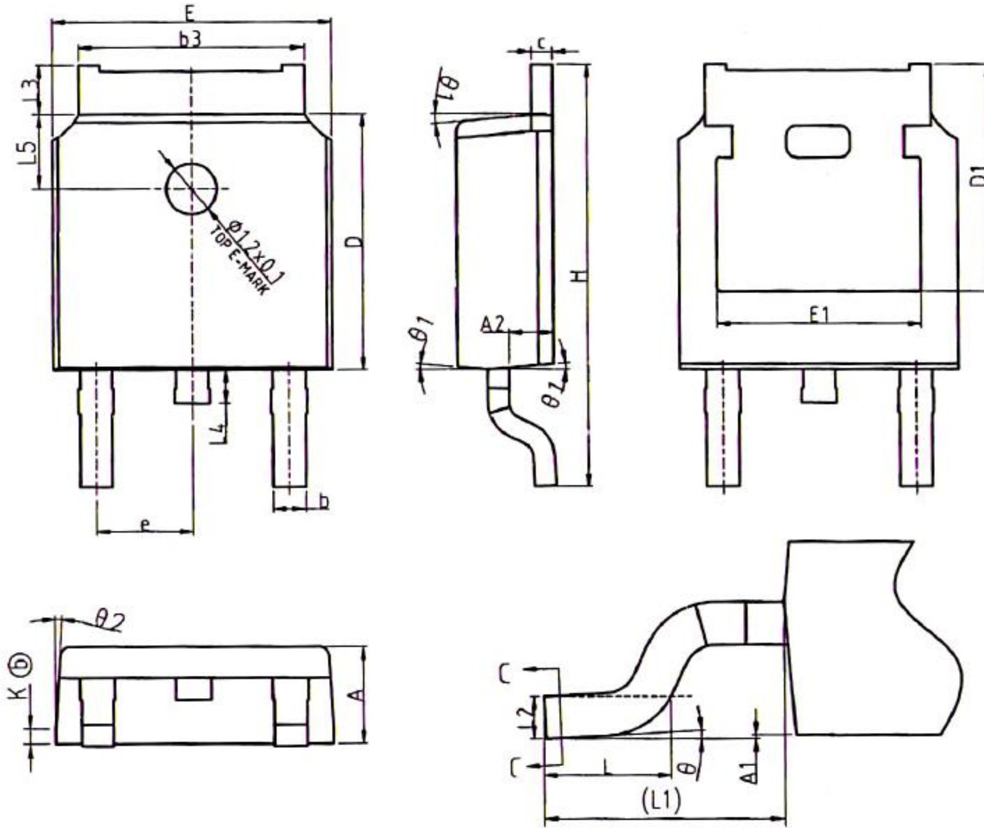
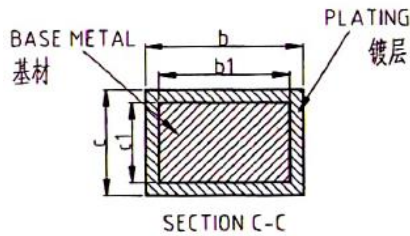
Package Outline

TO-252





COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ1	5°	7°	9°
θ2	5°	7°	9°
K	0.40REF		

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