



SUPER-SEMI



## SUPER-MOSFET

Super Gate Metal Oxide Semiconductor Field Effect Transistor

100V Super Gate Power Transistor  
SG\*100N45T

Rev. 1.0  
Dec. 2016

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# SGT100N45T/SGP100N45T 100V N-Channel MOSFET

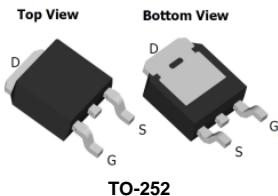
## Description

The SG-MOSFET uses trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of RDS(ON), Ciss and Coss. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

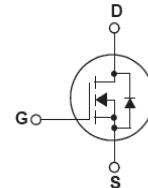
## Features

- V<sub>DS</sub> 100V
- I<sub>D</sub> (at V<sub>GS</sub>=10V) 25A
- RDS(on) (at V<sub>GS</sub>=10V) <45mΩ
- 100% avalanche tested

**SGT100N45T**



**SGP100N45T**



## Absolute Maximum Ratings

Symbol	Parameter	SGT_P100N45T	Unit
V <sub>DS</sub>	Drain-Source Voltage	100	V
I <sub>D</sub>	Drain Current - Continuous (TA = 25°C) - Continuous (TA = 100°C)	25* 16*	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	100*	A
V <sub>GS</sub>	Gate-Source voltage	±20	V
I <sub>AS</sub>	Avalanche Current, single pulse (Note 1)	27	A
E <sub>AS</sub>	Avalanche Energy, single pulse, L=0.5mH (Note 1)	360	mJ
P <sub>D</sub>	Power Dissipation - TA = 25°C (Note 2)	40	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C

\* Drain current limited by maximum junction temperature.

## Thermal Characteristics

Symbol	Parameter	SGT_P100N45T	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	3.1	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink Typ.	0.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62	°C/W



# Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

SGT100N45T/SGP100N45T 100V N-Channel MOSFET

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_{\text{D}} = 250\mu\text{A}$ , $T_J = 25^\circ\text{C}$	100	115	-	V
$\text{I}_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{\text{DS}} = 100\text{V}$ , $V_{\text{GS}} = 0\text{V}$ $-T_J = 125^\circ\text{C}$	-	10	1	$\mu\text{A}$
$\text{I}_{\text{GSSF}}$	Gate-Body Leakage Current, Forward	$V_{\text{GS}} = 20\text{V}$ , $V_{\text{DS}} = 0\text{V}$	-	-	100	nA
$\text{I}_{\text{GSSR}}$	Gate-Body Leakage Current, Reverse	$V_{\text{GS}} = -20\text{V}$ , $V_{\text{DS}} = 0\text{V}$	-	-	-100	nA
<b>On Characteristics</b>						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\mu\text{A}$	2.3	3.2	4.1	V
$\text{R}_{\text{DS(on)}}$	Static Drain-Source On-Resistance	$V_{\text{GS}} = 10\text{V}$ , $I_{\text{D}} = 12\text{A}$ $V_{\text{GS}} = 6\text{V}$ , $I_{\text{D}} = 6\text{A}$	-	38 48	45 62	$\text{m}\Omega$
$\text{g}_{\text{FS}}$	Forward Transconductance	$V_{\text{DS}} = 5\text{V}$ , $I_{\text{D}} = 12\text{A}$	-	16	-	S
$R_g$	Gate resistance	$V_{\text{GS}}=0\text{V}$ , $V_{\text{DS}}=0\text{V}$ , $f=1\text{MHz}$	-	1.5	-	$\Omega$
<b>Dynamic Characteristics</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 50\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $f=1\text{MHz}$	-	890	-	pF
$C_{\text{oss}}$	Output Capacitance		-	60	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	40	-	pF
<b>Switching Characteristics</b>						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DS}} = 50\text{V}$ , $R_g = 3\Omega$ , $I_{\text{D}} = 6\text{A}$ , $V_{\text{GS}} = 10\text{V}$ (Note 3, 4)	-	9	-	ns
$t_r$	Turn-On Rise Time		-	5	-	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		-	18	-	ns
$t_f$	Turn-Off Fall Time		-	5	-	ns
$Q_g$	Total Gate Charge	$V_{\text{DS}} = 50\text{V}$ , $I_{\text{D}} = 6\text{A}$ , $V_{\text{GS}} = 0\sim 10\text{V}$ (Note 3, 4)	-	14	-	nC
$Q_{gs}$	Gate-Source Charge		-	4	-	nC
$Q_{gd}$	Gate-Drain Charge		-	5	-	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_s$	Maximum Continuous Drain-Source Diode Forward Current	-	-	25	A	
$I_{\text{SM}}$	Maximum Pulsed Drain-Source Diode Forward Current	-	-	100	A	
$V_{\text{SD}}$	Drain-Source Diode Forward Voltage	$V_{\text{GS}} = 0\text{V}$ , $I_{\text{s}} = 1\text{A}$	-	0.7	1.0	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_{\text{GS}} = 0\text{V}$ , $VR=50\text{V}$ , $I_{\text{s}} = 6\text{A}$ $dI/dt = 500\text{A}/\mu\text{s}$ (Note 3)	-	44	-	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		-	60	-	nC

## NOTES:

- Repetitive Rating: Pulse width limited by maximum junction temperature  $T_J(\text{MAX})=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .
- The power dissipation PD is based on  $T_J(\text{MAX})=150^\circ\text{C}$ , using  $\leq 10\text{s}$  junction-to-ambient thermal resistance.
- Pulse Test: Pulse width  $\leq 300\text{us}$ , Duty Cycle  $\leq 2\%$
- Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

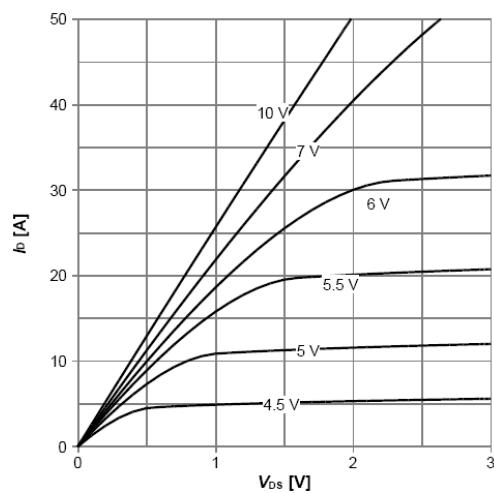


Figure 1: On-Region Characteristics

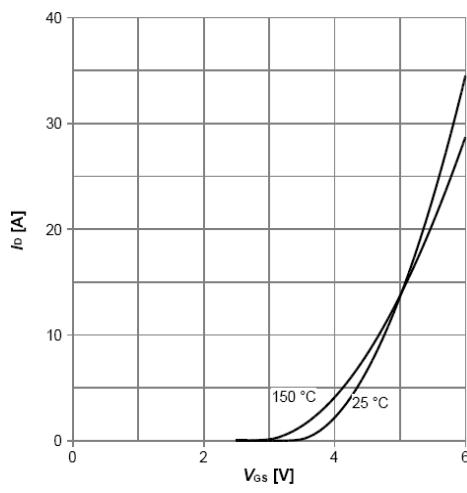


Figure 2: Transfer Characteristics

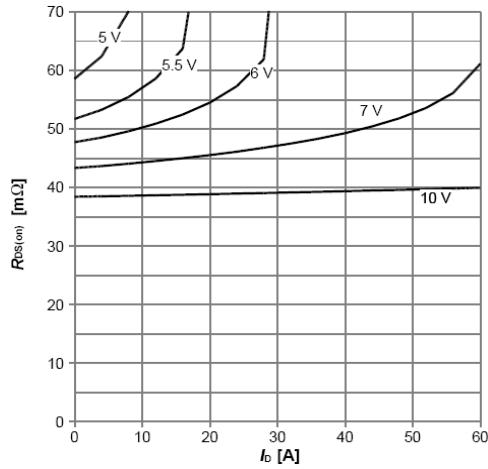


Figure 3: On-Resistance vs Drain current and Gate voltage

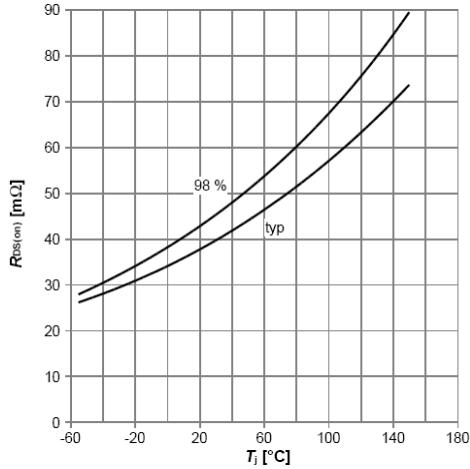


Figure 4: On-Resistance vs Junction Temperature

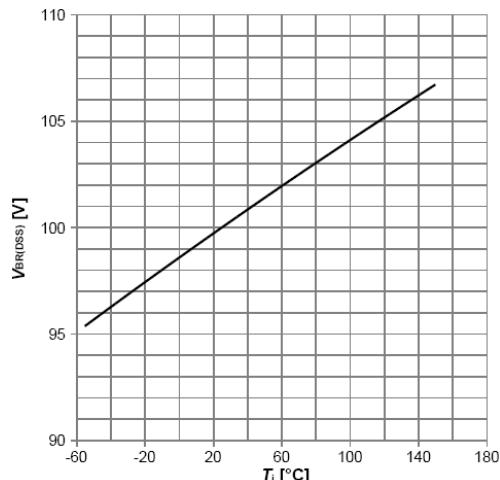


Figure 5: Drain-Source breakdown voltage

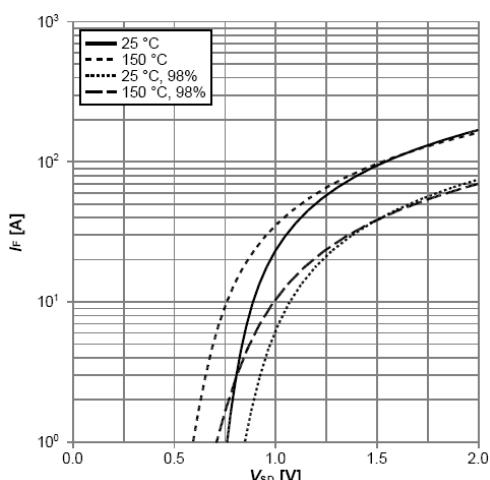


Figure 6: Body-Diode Characteristics



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## Typical Performance Characteristics

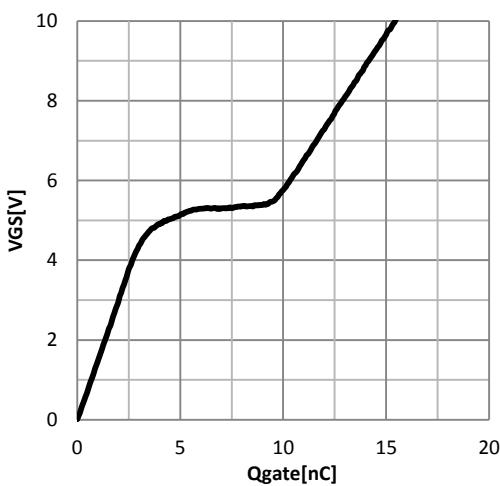


Figure 7: Gate-Charge Characteristics

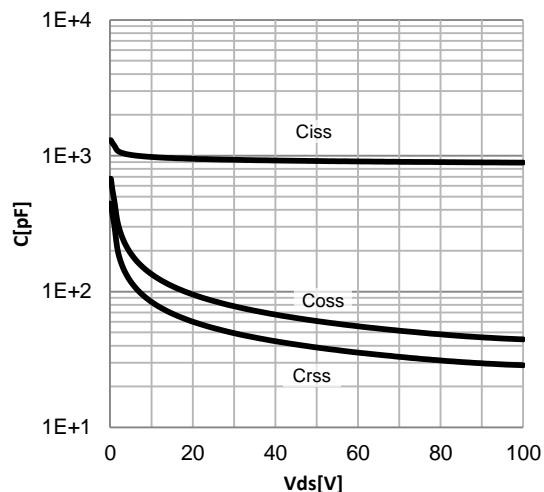


Figure 8: Capacitance Characteristics

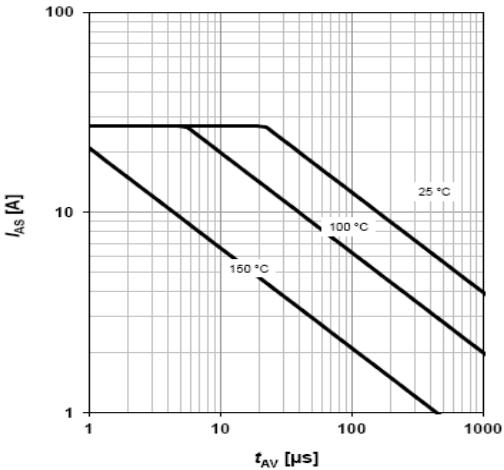


Figure 9: Avalanche Characteristics

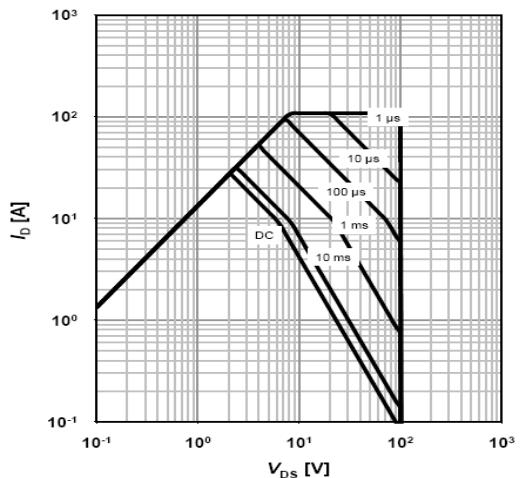


Figure 10: Maximum Forward Biased Safe Operating Area

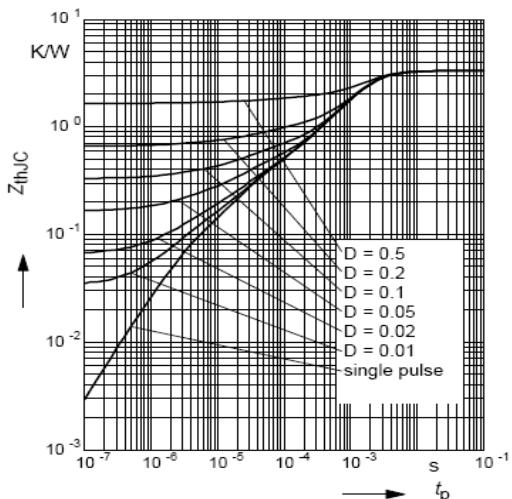


Figure 11: Maximum Transient Thermal Impedance

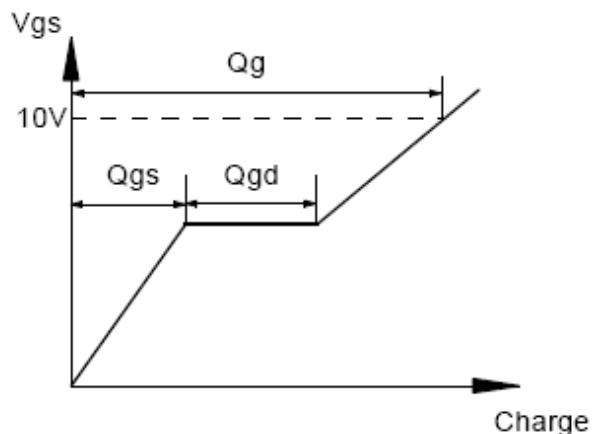
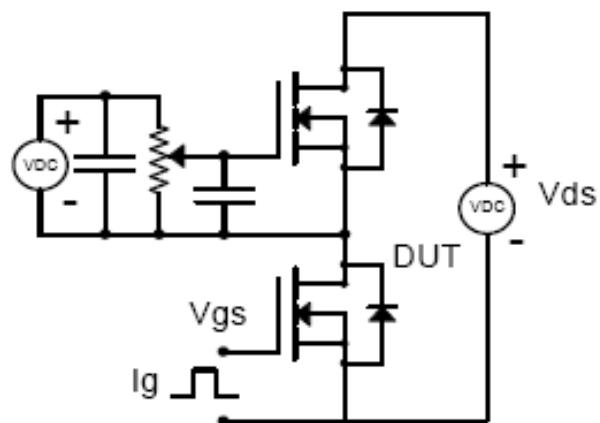


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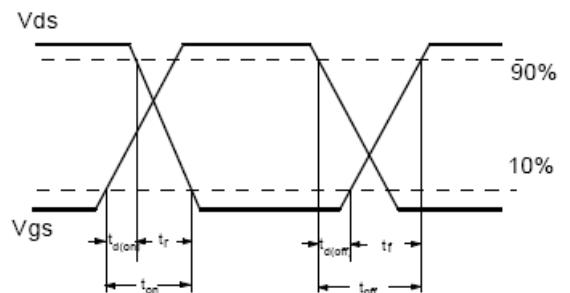
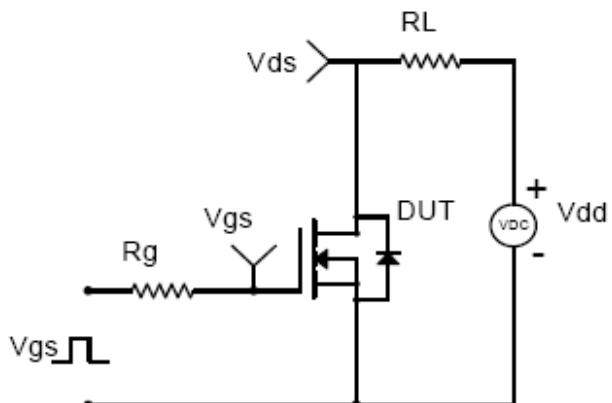
## Test circuits

SGT100N45T/SGP100N45T 100V N-Channel MOSFET

Gate Charge Test Circuit and Waveform



Resistive Switching Test Circuit and Waveforms



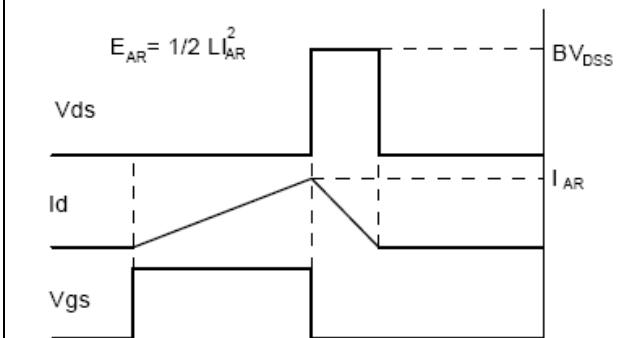
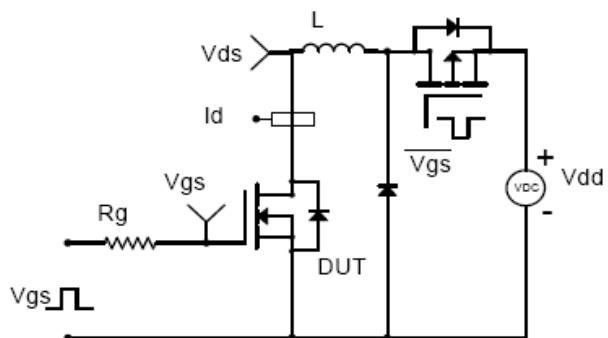


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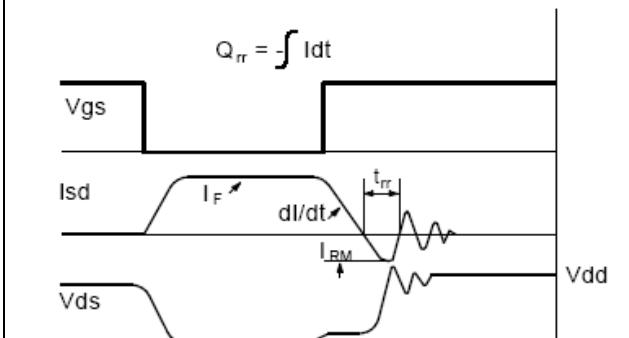
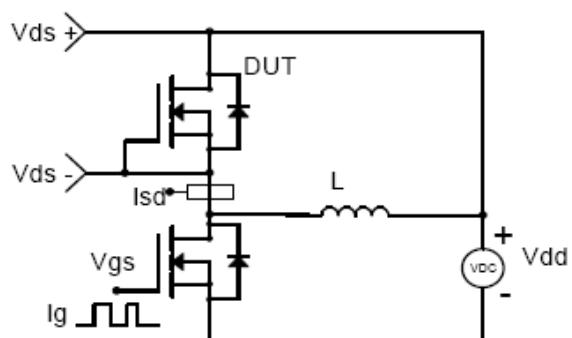
## Test circuits

SGT100N45T/SGP100N45T 100V N-Channel MOSFET

### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



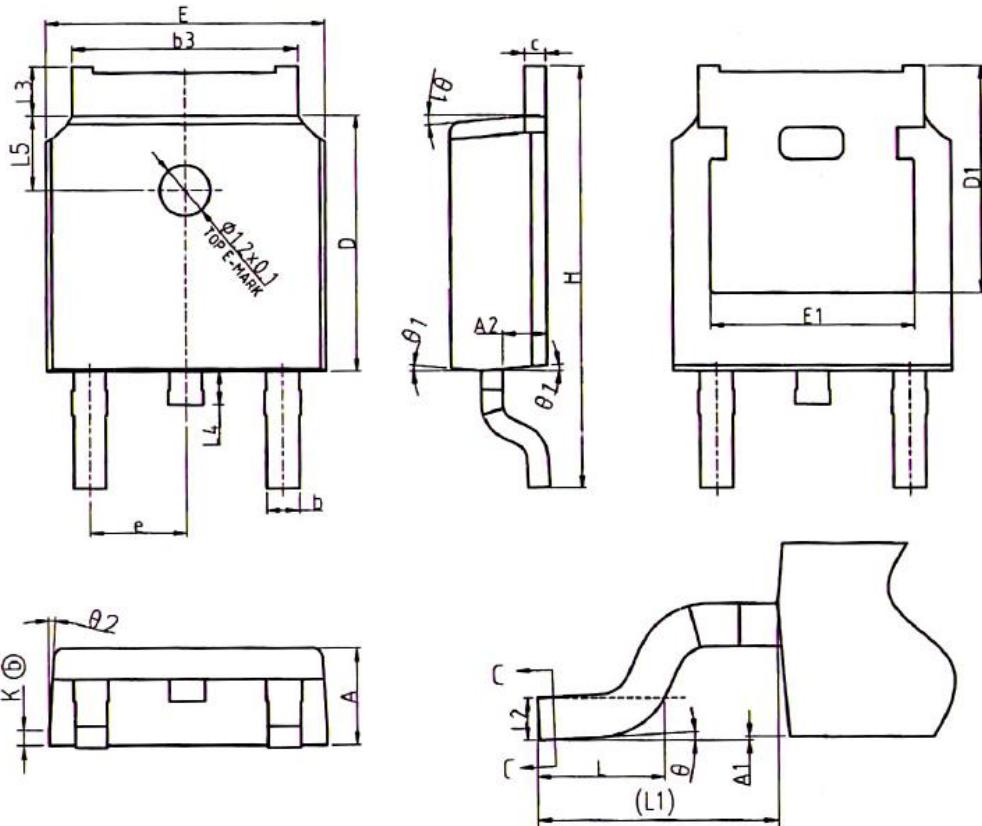
### Diode Recovery Test Circuit & Waveforms





## Package Outline

TO-252



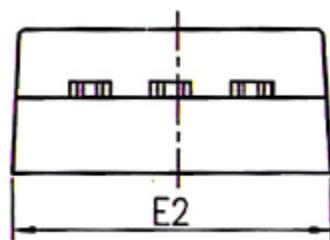
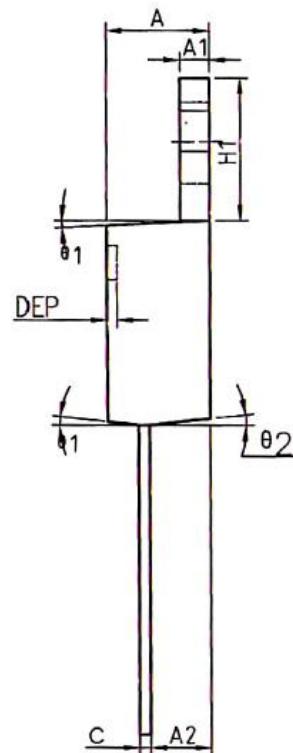
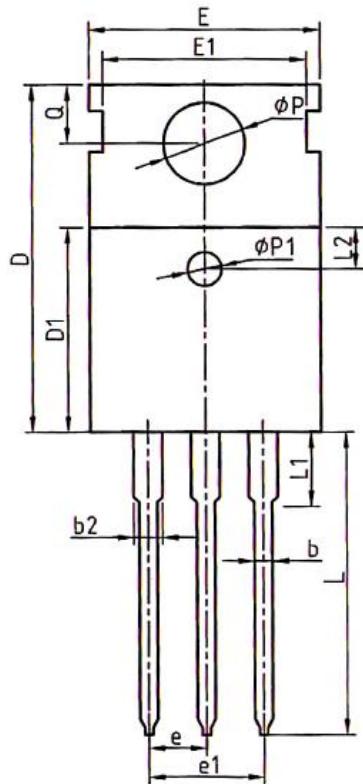
### COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.10
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
c1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	9.90	10.10	10.30
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	-	1.25
L4	0.60	0.80	1.00
L5	1.70	1.80	1.90
θ	0°	-	8°
θ1	5°	7°	9°
θ2	5°	7°	9°
K	0.40REF		



# Package Outline

TO-220



## COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.40	4.57	4.70
A1	1.27	1.30	1.37
A2	2.35	2.40	2.50
b	0.77	0.80	0.90
b2	1.17	1.27	1.36
c	0.48	0.50	0.56
D	15.40	15.60	15.80
D1	9.00	9.10	9.20
DEP	0.05	0.10	0.20
E	9.80	10.00	10.20
E1	—	8.70	—
E2	9.80	10.00	10.20
φP1	1.40	1.50	1.60
e	2.54BSC		
e1	5.08BSC		
H1	6.40	6.50	6.60
L	12.75	13.50	13.65
L1	—	3.10	3.30
L2	2.50REF		
φP	3.50	3.60	3.63
Q	2.73	2.80	2.87
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	1°	3°	5°