FORESEE eMMC NCEMASLD-xxG Datasheet

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Revision History:

Rev.	Date	Changes	Remark
1.0	2018/01/30	Basic spec and architecture	Preliminary
1.1	2018/03/29	Revise some descriptions	
1.2	2018/04/11	Add NCEMASLD-64G	
1.3	2018/04/19	Revise some descriptions	
1.4	2018/07/16	Add NCEMASLD-128G	

CONTENTS

1. Introduction

FORESEE eMMC is an embedded storage solution designed in the BGA package. The FORESEE eMMC consists of NAND flash and eMMC controller. The controller could manage the interface protocols，wear-leveling，bad block management and ECC.

FORESEE eMMC has high performance at a competitive cost, high quality and low power consumption, and eMMC is compatible with JEDEC standard eMMC 5.1 specifications.

2. Product List

Density	Part Number	NAND Flash Type	Capacity	Package Size(mm)	Package Type
32GB	NCEMASLD-32G	256Gb x1	28.8GB	11.5x13x1.0	153FBGA
64GB	NCEMASLD-64G	256Gb x2	57.6GB	11.5x13x1.0	153FBGA
128GB	NCEMASLD-128G	256Gb x4	115.2GB	11.5x13x1.2	153FBGA

3. Features

- **eMMC5.1 specification compatibility**
  (Backward compatible to eMMC4.41/4.5/5.0)
- **Bus mode**
  - Data bus width: 1 bit (default), 4 bits, 8 bits
  - Data transfer rate: up to 400MB/s (HS400)
  - MMC I/F Clock frequency：0~200MHz
- **Operating voltage range**
  - Vcc(NAND)：2.7 - 3.6V
  - Vccq(Controller)：1.7 - 1.95V / 2.7 - 3.6V
- **Temperature**
  - Operation (-25℃ ~ +85℃)
  - Storage without operation (-40℃ ~ +85℃)
- **Sudden-Power-Loss safeguard**
- **Hardware ECC engine**
- **Unique firmware backup mechanism**
- **Global-wear-leveling**
- **Supported features.**
  - HS400, HS200
  - Partitioning, RPMB
  - Boot feature, boot partition
  - HW Reset/SW Reset
  - Discard, Trim, Erase, Sanitize
  - Background operations, HPI
  - Enhanced reliable write
  - S.M.A.R.T. Health Report
  - Command queuing
  - FFU
  - Sleep / awake
- **Others**
  - Compliance with the RoHS Directive

4. Functional Description

FORESEE eMMC with powerful L2P (Logical to Physical) NAND Flash management algorithm provides unique functions:

- Host independence from details of operating NAND flash
- Internal ECC to correct defect in NAND flash
- Sudden-Power-Loss safeguard

  To prevent from data loss, a mechanism named Sudden-Power-Loss safeguard is added in the eMMC. In the case of sudden power-failure, the eMMC would work properly after power cycling.
- Global-wear-leveling

  To achieve the best stability and device endurance, this eMMC equips the Global Wear Leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.
- IDA(Initial Data Acceleration)

  The eMMC prevents the pre-burned data from data-loss with IDA, in case of our customer had pre-burned data to eMMC, before the eMMC being SMT.
- Cache

  The eMMC enhanced the data written performance with Cache, with which our customer would get more endurance and reliability.

5. Product Specifications

5.1 Performance

Part Number	Write	Read
NCEMASLD-32G	Up to 110MB/s	Up to 200MB/s
NCEMASLD-64G	Up to 150MB/s	Up to 200MB/s
NCEMASLD-128G	Up to 155MB/s	Up to 240MB/s

• Test Condition: Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead, measured on internal board

• Test tool: uBOOT (Without O/S)

• Chunk size: 1MB,

• Test area: 100MB/ Full-range of LBA.

5.2 Power Consumption

5.2.1 Active power consumption during operation

Part Number	Icc	Iccq
NCEMASLD-32G	100mA	150mA
NCEMASLD-64G	120mA	150mA
NCEMASLD-128G	120mA	150mA

• Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

• Vcc:3.3V & Vccq：1.8V.

• The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

5.2.2 Low power mode (stand-by)

Part Number	Icc	Iccq
NCEMASLD-32G	70uA	150uA
NCEMASLD-64G	100uA	160uA
NCEMASLD-128G	150uA	160uA

• Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

• Standby: Nand Vcc & Controller Vccq power supply is switched on.

• The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

5.2.3 Low power mode (sleep)

Part Number	Icc	Iccq
NCEMASLD-32G	0	150uA
NCEMASLD-64G	0	160uA
NCEMASLD-128G	0	160uA

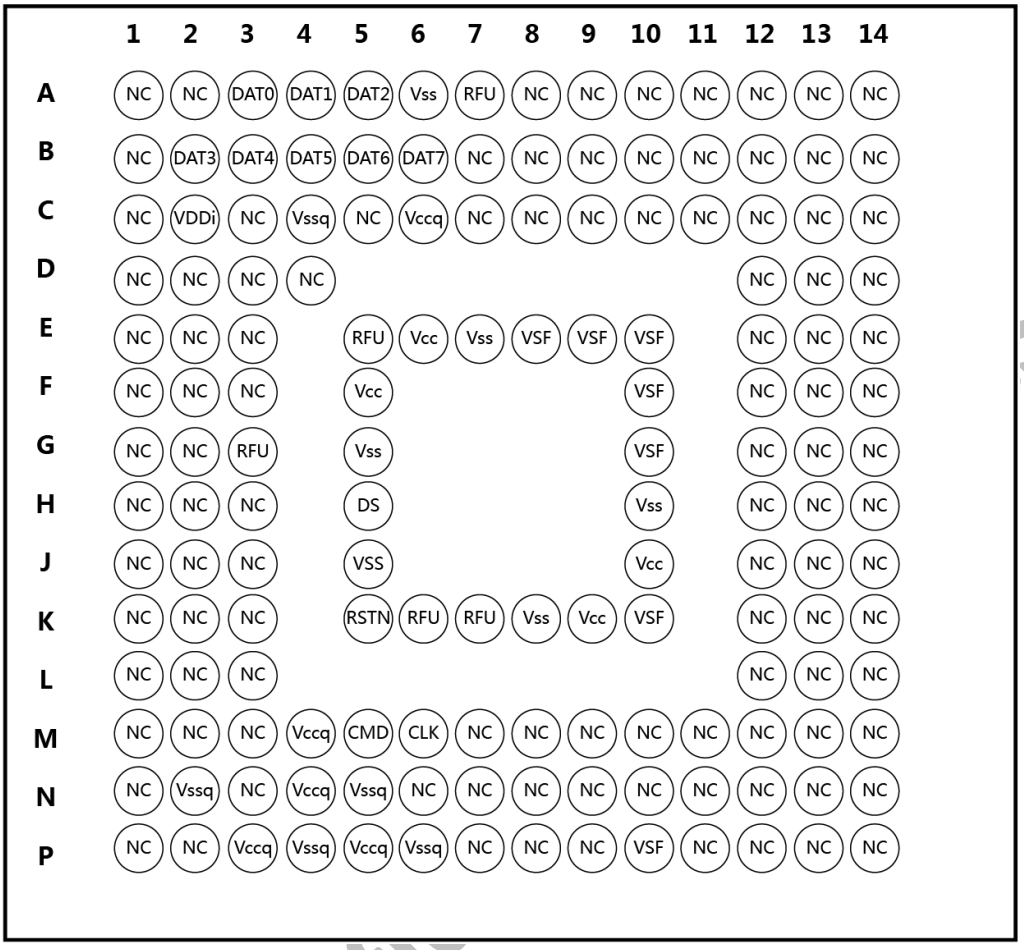
• Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 23℃.

• Sleep: Nand Vcc power supply is switched off(Controller Vccq on)

• The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

6. Pin Assignments

6.1 Ball Array view



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	Vss	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDi	NC	Vssq	NC	Vccq	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC								NC	NC	NC
E	NC	NC	NC		RFU	Vcc	Vss	VSF	VSF	VSF		NC	NC	NC
F	NC	NC	NC		Vcc					VSF		NC	NC	NC
G	NC	NC	RFU		Vss					VSF		NC	NC	NC
H	NC	NC	NC		DS					Vss		NC	NC	NC
J	NC	NC	NC		VSS					Vcc		NC	NC	NC
K	NC	NC	NC		RSTN	RFU	RFU	Vss	Vcc	VSF		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	Vccq	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	Vssq	NC	Vccq	Vssq	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	Vccq	Vssq	Vccq	Vssq	NC	NC	NC	VSF	NC	NC	NC	NC

FBGA153 - Ball Array (Top View through package)

6.2 Ball Array view

Signal	Description
CLOCK (CLK)	Each cycle of the clock directs a transfer on the command line and on the data lines.
COMMAND (CMD)	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain, for initialization, and push-pull, for command transfer. Commands are sent from the host to the device, and responses are sent from the device to the host.
DATA (DAT0-DAT7)	These are bidirectional data signal. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The controller can configure a wider data bus for data transfer wither using DAT [3:0](4bit mode)or DAT[7:0](8bit mode). Includes internal pull-up resistors for data lines DAT[7:1].Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT1 and DAT2 lines.(The DAT3 line internal pull-up is left connected.)Upon entering the 8bit mode, the device disconnects the internal pull-up on the DAT1, DAT2, and DAT[7:4]lines.
Data Strobe (DS)	Newly assigned pin for HS400 mode. Data Strobe is generated from e.MMC to host. In HS400 mode, read data and CRC response are synchronized with Data Strobe.
RESET (RSTN)	Hardware Reset Input
Vccq	Vccq is the power supply line for host interface, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V
Vcc	Vcc is the power supply line for internal flash memory, its power voltage range is:2.7V~3.6V
VDDi	VDDi is internal power node, not the power supply. Connect 1uF capacitor VDDi to ground
Vss,Vssq	Ground lines.

Note:

NC: No Connect, shall be connected to ground or left floating.

RFU: Reserved for Future Use, must be left floating for future use.

VSF: Vendor Specific Function, must be left floating.