

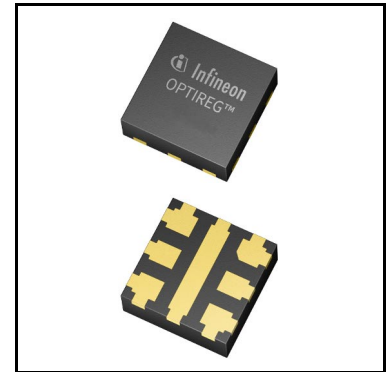
# OPTIREG™ Linear TLS715B0NAV50

## Low dropout linear voltage regulator



### Features

- Wide input voltage range from 4.0 V to 40 V
- Output voltage 5 V
- Output voltage accuracy  $\pm 2\%$
- Output current up to 150 mA
- Low current consumption of 36  $\mu\text{A}$
- Very low dropout voltage of typically 180 mV at 100 mA output current
- Stable with small output capacitor of 1  $\mu\text{F}$
- Enable
- Overtemperature shutdown
- Output current limitation
- Wide temperature range from  $-40^\circ\text{C}$  up to  $150^\circ\text{C}$
- Green Product (RoHS compliant)



### Potential applications

- ADAS applications (CAN supply)
- Infotainment, Dashboard
- Automotive applications especially with tight space constraints

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

### Description

The OPTIREG™ Linear TLS715B0NAV50 is a low dropout linear voltage regulator for load current up to 150 mA. An input voltage of up to 40 V is regulated to  $V_{Q,nom} = 5\text{ V}$  with  $\pm 2\%$  precision.

The TLS715B0NAV50, with a typical quiescent current of 36  $\mu\text{A}$ , is the ideal solution for systems requiring very low operating current, such as those permanently connected to the battery.

It features a very low dropout voltage of 180 mV, when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 4.0 V (extended operating range). This makes the TLS715B0NAV50 suitable to supply automotive systems with start-stop requirements.

The device can be switched on and off by the Enable feature as described on Chapter **“Enable” on Page 15**.

In addition, the TLS715B0NAV50’s new fast regulation concept requires only a single 1  $\mu\text{F}$  output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, over-current and over-temperature. The TLS715B0NAV50 can be also used in all other applications requiring a stabilized 5 V supply voltage.

<b>Type</b>	<b>Package</b>	<b>Marking</b>
TLS715B0NAV50	PG-TSNP-7	715B5

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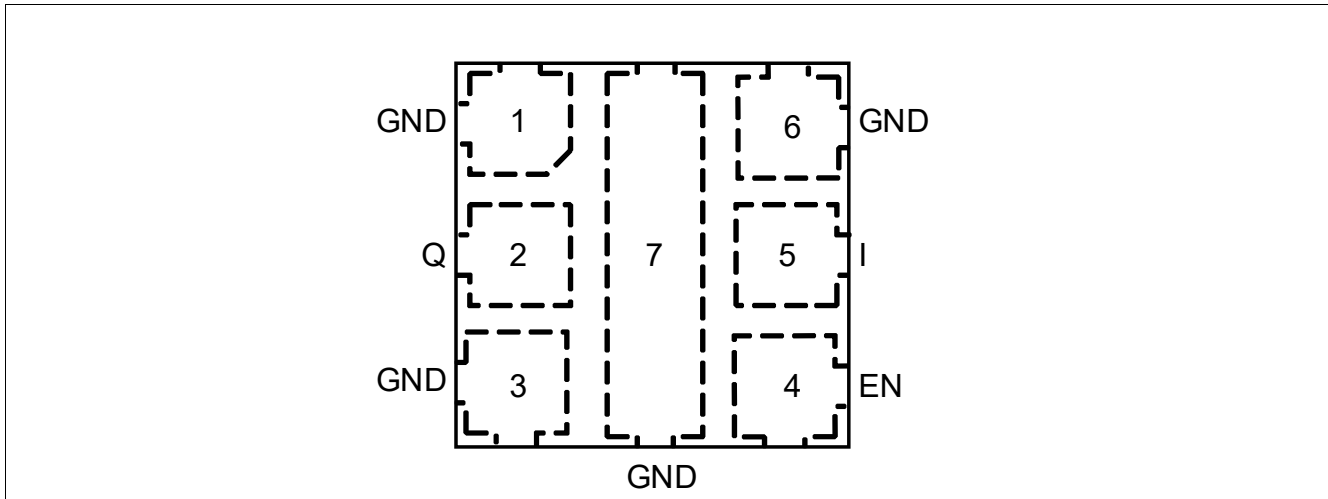
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**Pin configuration**

**2 Pin configuration**

**2.1 Pin assignment PG-TSNP-7**



**Figure 2 Pin configuration**

**2.2 Pin definitions and functions PG-TSNP-7**

Pin	Symbol	Function
1	GND	<b>Ground</b>
2	Q	<b>Output</b> Block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR in the table <b>“Functional range” on Page 7</b> .
3	GND	<b>Ground</b>
4	EN	<b>Enable</b> (integrated pull-down resistor) Enable the IC with high level input signal. Disable the IC with low level input signal.
5	I	<b>Input</b> For compensating line influences, a capacitor to GND close to the IC terminals is recommended.
6	GND	<b>Ground</b>
7	GND	<b>Ground</b>

General product characteristics

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 1 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input I, Enable EN</b>							
Voltage	$V_I, V_{EN}$	-0.3	–	45	V	–	P_4.1.1
<b>Output Q</b>							
Voltage	$V_Q$	-0.3	–	7	V	–	P_4.1.2
<b>Temperature</b>							
Junction temperature	$T_j$	-40	–	150	°C	–	P_4.1.3
Storage temperature	$T_{stg}$	-55	–	150	°C	–	P_4.1.4
<b>ESD absorption</b>							
ESD susceptibility to GND	$V_{ESD}$	-2	–	2	kV	HBM <sup>2)</sup>	P_4.1.5
ESD susceptibility to GND	$V_{ESD}$	-750	–	750	V	CDM <sup>3)</sup>	P_4.1.6

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

**3.2 Functional range**

**Table 2 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range for normal operation	$V_I$	$V_{Q,nom} + V_{dr}$	–	40	V	–	P_4.2.1
Extended input voltage range	$V_{I,ext}$	4.0	–	40	V	– <sup>1)</sup>	P_4.2.2
Enable voltage range	$V_{EN}$	0	–	40	V	–	P_4.2.3
Output capacitor's requirements for stability	$C_Q$	1	–	–	μF	– <sup>2)</sup>	P_4.2.4
Output capacitor's ESR	$ESR(C_Q)$	–	–	5	Ω	– <sup>3)</sup>	P_4.2.5
Junction temperature	$T_i$	-40	–	150	°C	–	P_4.2.6

1) When  $V_{I,ext,min} < V_I < V_{Q,nom} + V_{dr}$ , then  $V_Q = V_I - V_{dr}$ . When  $V_I$  is below  $V_{I,ext,min}$ , then  $V_Q$  can drop to 0 V.

2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

3) Relevant ESR value at  $f = 10$  kHz

**Note:** *Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

**General product characteristics**

**3.3 Thermal resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Package version PG-TSNP-7</b>							
Junction to case <sup>1)</sup>	$R_{thJC}$	–	14	–	K/W	–	P_4.3.1
Junction to ambient	$R_{thJA}$	–	61	–	K/W	2s2p board <sup>2)</sup>	P_4.3.2
Junction to ambient	$R_{thJA}$	–	196	–	K/W	1s0p board, footprint only <sup>3)</sup>	P_4.3.3
Junction to ambient	$R_{thJA}$	–	94	–	K/W	1s0p board, 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.4
Junction to ambient	$R_{thJA}$	–	83	–	K/W	1s0p board, 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup>	P_4.3.5

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
- 3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70 μm Cu).



## 4 Block description and electrical characteristics

### 4.1 Voltage regulation

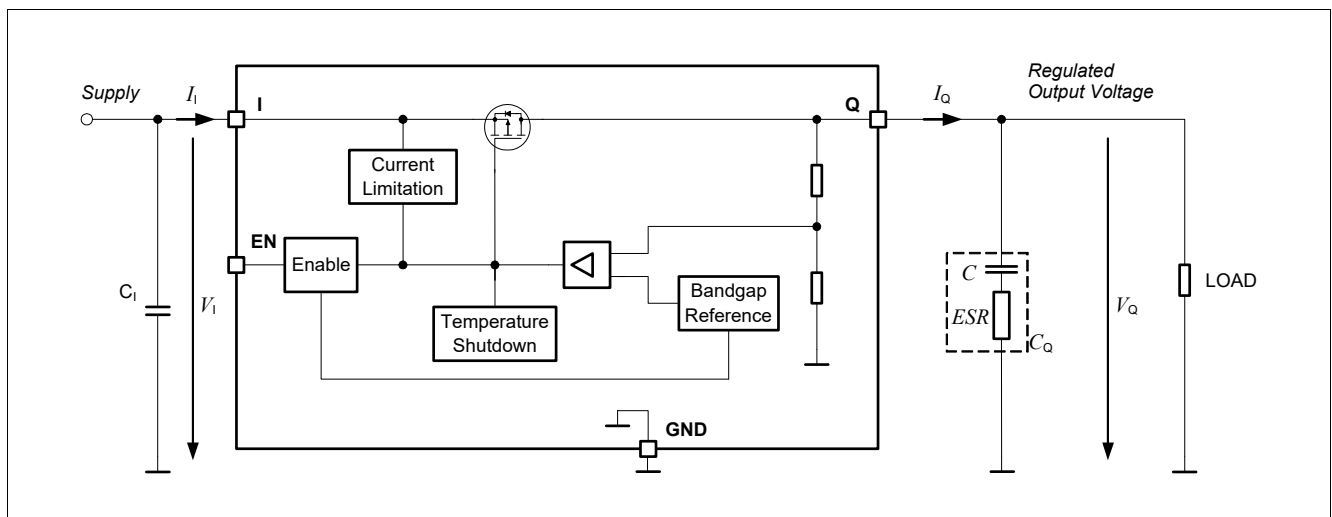
The output voltage  $V_Q$  is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor  $C_O$ , the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Table 2 "Functional range" on Page 7** must be maintained. For details see the typical performance graph **"Output capacitor series resistor ESR(CQ) versus output current IQ" on Page 12**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor  $C_I$  is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used, in case the input is connected directly to the battery line. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, for example in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (for example output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the maximum rating of 150°C and can significantly reduce the IC's lifetime.



**Figure 3 Block diagram voltage regulation**

**Block description and electrical characteristics**

**Table 4 Electrical characteristics voltage regulator**

$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified).  
 Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage precision	$V_Q$	4.9	5.0	5.1	V	$0.05\text{ mA} < I_Q < 150\text{ mA}$ $6\text{ V} < V_I < 28\text{ V}$	P_5.1.1
Output voltage precision	$V_Q$	4.9	5.0	5.1	V	$0.05\text{ mA} < I_Q < 100\text{ mA}$ $6\text{ V} < V_I < 40\text{ V}$	P_5.1.2
Output current limitation	$I_{Q,max}$	151	250	350	mA	$0\text{ V} < V_Q < 4.8\text{ V}$ $4\text{ V} < V_I < 28\text{ V}$	P_5.1.5
Load regulation steady-state	$ \Delta V_{Q,load} $	–	1	25	mV	$I_Q = 0.05\text{ mA}$ to $100\text{ mA}$ $V_I = 6\text{ V}$	P_5.1.9
Line regulation steady-state	$ \Delta V_{Q,line} $	–	1	25	mV	$V_I = 8\text{ V}$ to $32\text{ V}$ $I_Q = 5\text{ mA}$	P_5.1.10
Dropout voltage <sup>1)</sup> $V_{dr} = V_I - V_Q$	$V_{dr}$	–	180	500	mV	$I_Q = 100\text{ mA}$	P_5.1.11
Power supply ripple rejection <sup>2)</sup>	$PSRR$	–	60	–	dB	$f_{ripple} = 100\text{ Hz}$ $V_{ripple} = 0.5\text{ Vpp}$	P_5.1.12
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	$T_j$ increasing <sup>2)</sup>	P_5.1.13
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	$T_j$ decreasing <sup>2)</sup>	P_5.1.14

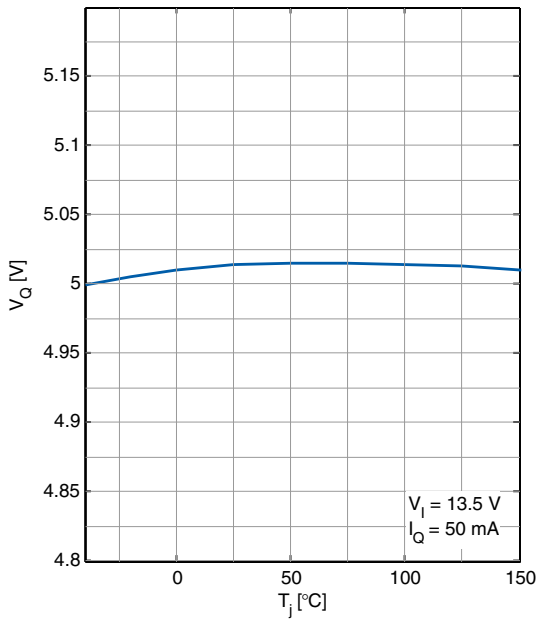
1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{V}$

2) Not subject to production test, specified by design

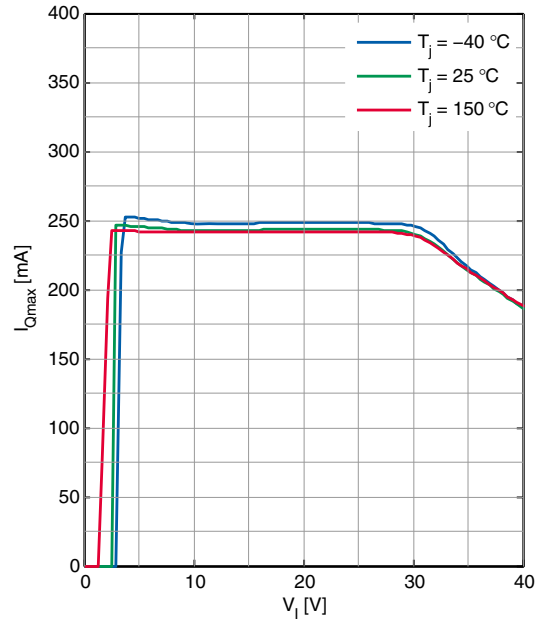
## 4.2 Typical performance characteristics voltage regulator

### Typical performance characteristics

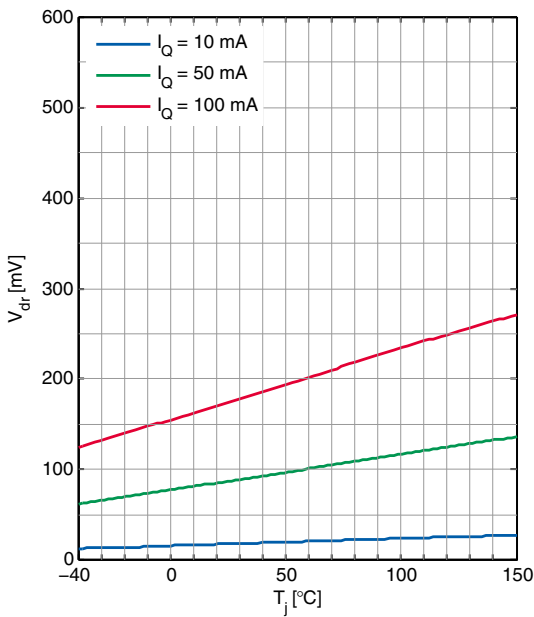
**Output voltage  $V_Q$  versus junction temperature  $T_j$**



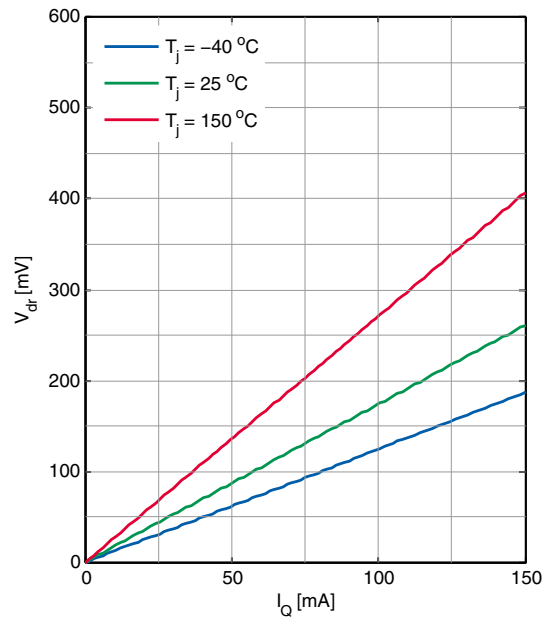
**Output current  $I_Q$  versus input voltage  $V_I$**



**Dropout voltage  $V_{dr}$  versus junction temperature  $T_j$**

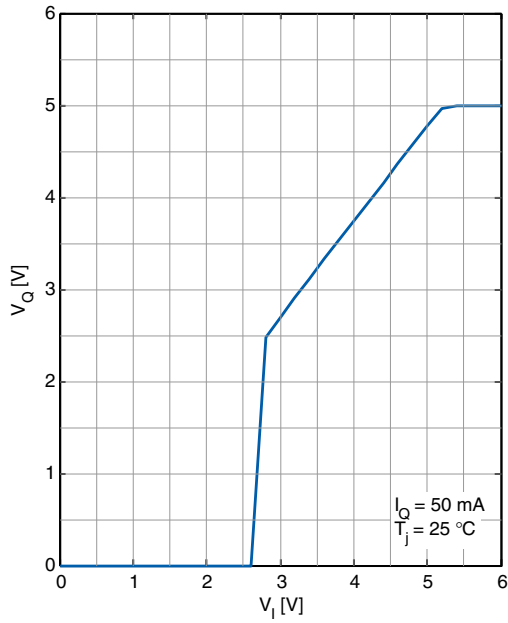


**Dropout voltage  $V_{dr}$  versus output current  $I_Q$**

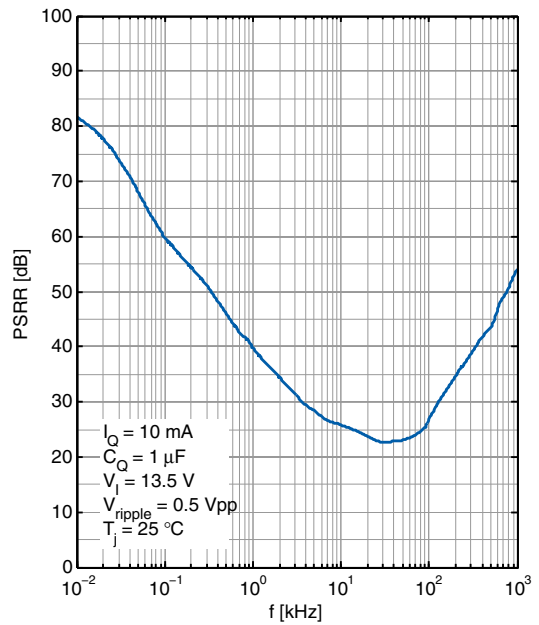


**Block description and electrical characteristics**

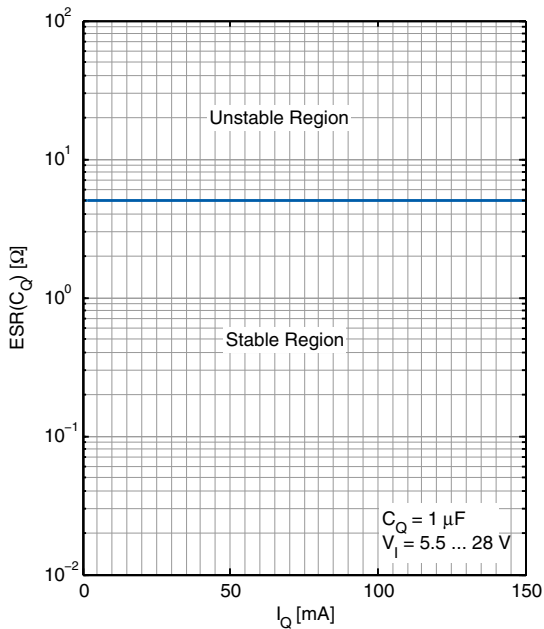
**Output voltage  $V_Q$  versus input voltage  $V_I$**



**Power supply ripple rejection  $PSRR$  versus ripple frequency  $f_r$**



**Output capacitor series resistor  $ESR(C_Q)$  versus output current  $I_Q$**



**Block description and electrical characteristics**

**4.3 Current consumption**

**Table 5 Electrical characteristics current consumption**

$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise specified).

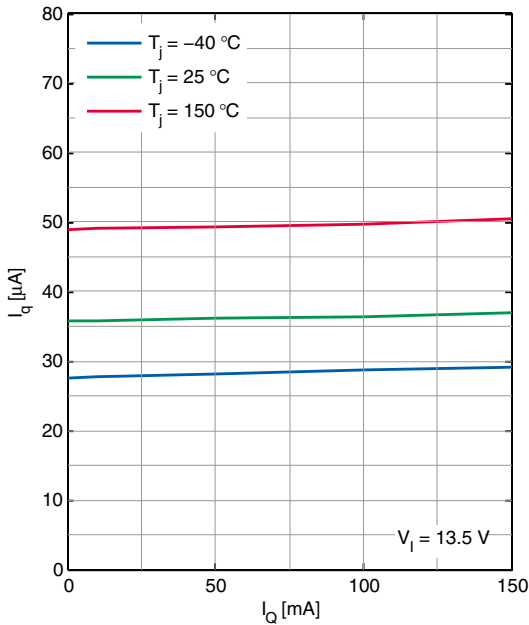
Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_1$	$I_{q,off}$	–	1.5	5	$\mu\text{A}$	$V_{EN} \leq 0.4\text{ V}$ $T_j < 105^\circ\text{C}$	P_5.3.1
Current consumption $I_q = I_1 - I_Q$	$I_q$	–	36	80	$\mu\text{A}$	$0.05\text{ mA} < I_Q < 100\text{ mA}$	P_5.3.2

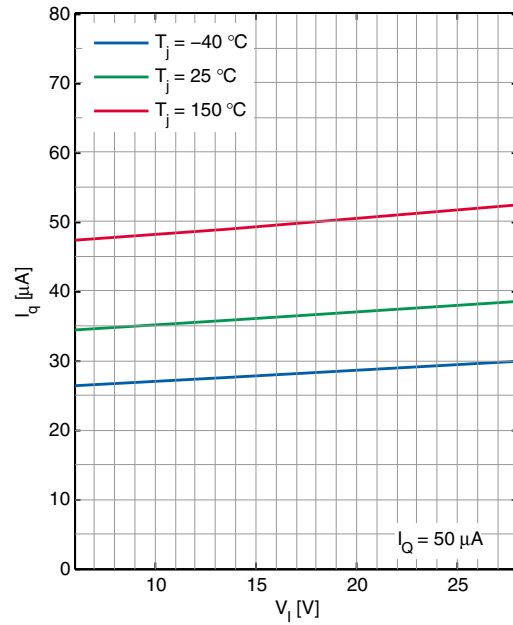
### 4.4 Typical performance characteristics current consumption

#### Typical performance characteristics

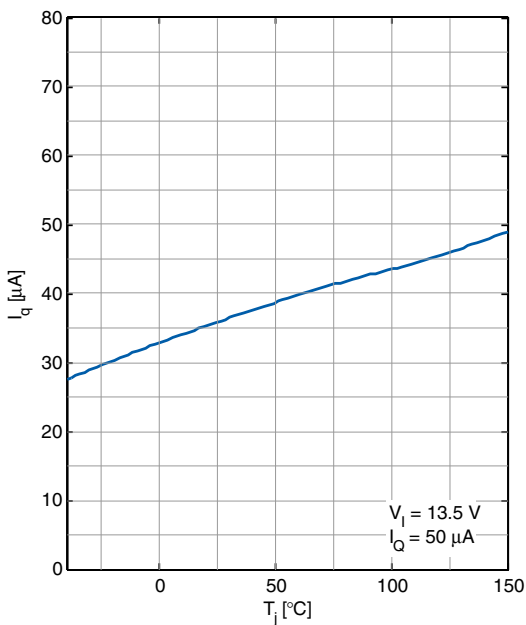
**Current consumption  $I_q$  versus output current  $I_Q$**



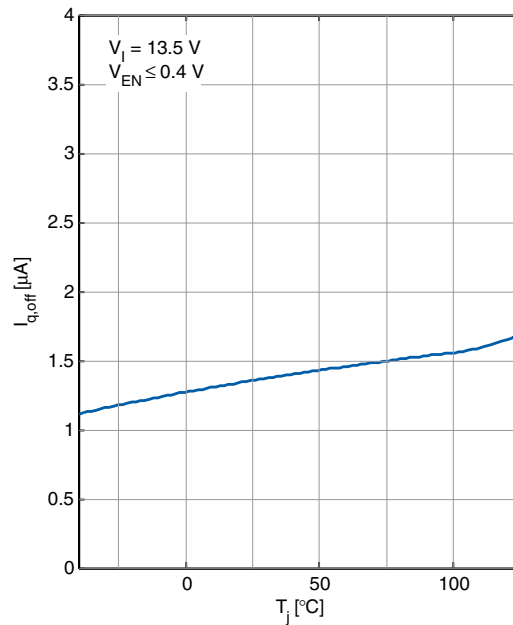
**Current consumption  $I_q$  versus input voltage  $V_i$**



**Current consumption  $I_q$  versus junction temperature  $T_j$**



**Current consumption in OFF mode  $I_{q,off}$  versus junction temperature  $T_j$**



**Block description and electrical characteristics**

**4.5 Enable**

The TLS715B0NAV50 can be switched on and off by the enable feature. Connect a HIGH level as specified below (for example the battery voltage) to pin EN to enable the device; connect a LOW level as specified below (for example GND) to switch it off. The Enable function has a build-in hysteresis to avoid toggling between ON/OFF state, if signals with slow slopes are applied to the input.

**Table 6 Electrical characteristics enable**

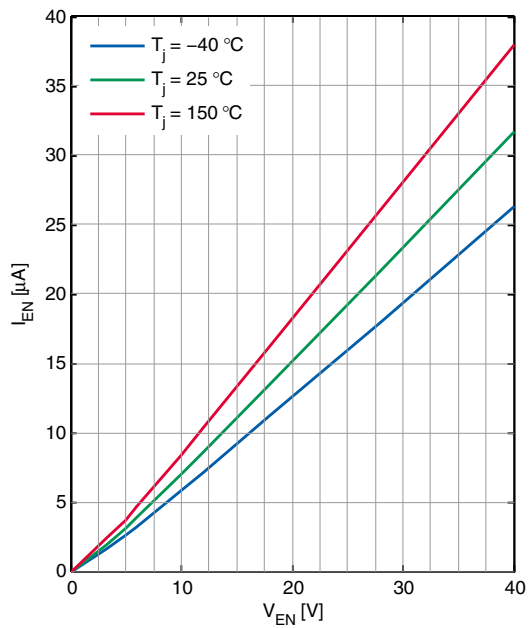
$V_I = 13.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified).  
 Typical values are given at  $T_j = 25^\circ\text{C}$ ,  $V_I = 13.5\text{ V}$ .

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable voltage high level	$V_{EN,H}$	2	–	–	V	$V_Q$ settled	P_5.5.1
Enable voltage low level	$V_{EN,L}$	–	–	0.8	V	$V_Q \leq 0.1\text{ V}$	P_5.5.2
Enable threshold hysteresis	$V_{EN,HY}$	75	–	–	mV	–	P_5.5.3
Enable input current low level	$I_{EN,H}$	–	–	5.5	$\mu\text{A}$	$V_{EN} = 5\text{ V}$	P_5.5.4
Enable input current high level	$I_{EN,H}$	–	–	22	$\mu\text{A}$	$V_{EN} < 18\text{ V}$	P_5.5.5
Enable internal pull-down resistor	$R_{EN}$	0.9	1.5	2.6	$\text{M}\Omega$	–	P_5.5.6

## 4.6 Typical performance characteristics enable

### Typical performance characteristics

**Enable input current  $I_{EN}$  versus  
enable voltage  $V_{EN}$**

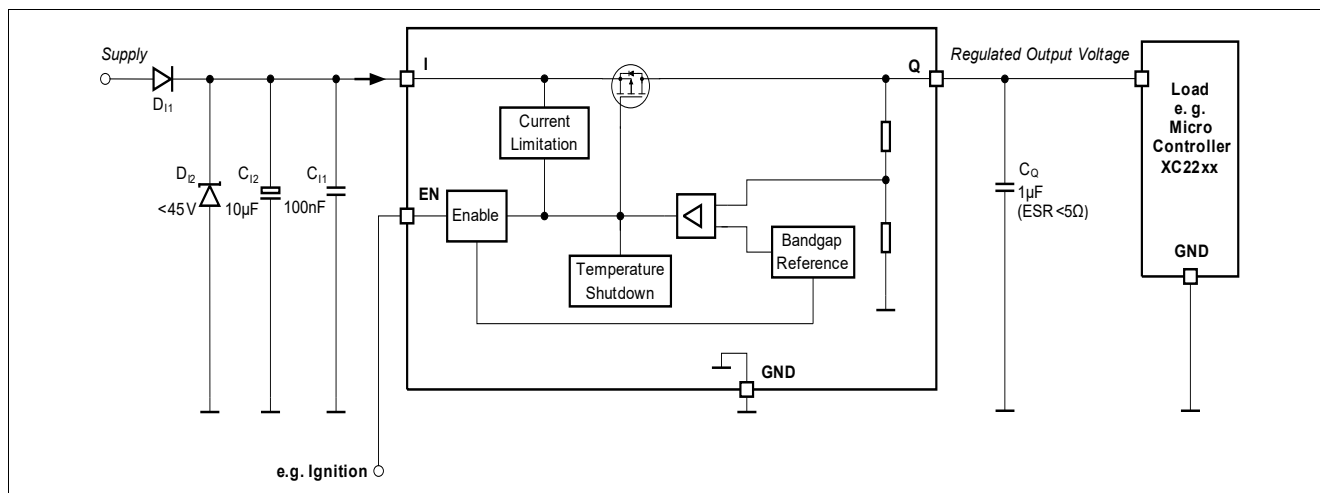




**Application information**

**5 Application information**

**5.1 Application diagram**



**Figure 4 Application diagram**

**5.2 Selection of external components**

**5.2.1 Input pin**

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

**5.2.2 Output pin**

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional range” on Page 7**. The graph **“Output capacitor series resistor ESR(CQ) versus output current IQ” on Page 12** shows the stable operation range of the device.

TLS715B0NAV50 is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

## Application information

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 5.3 Thermal considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (5.1)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5.2)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **“Thermal resistance” on Page 8**.

#### Example

Application conditions:

$$V_I = 13.5 \text{ V}$$

$$V_Q = 5 \text{ V}$$

$$I_Q = 100 \text{ mA}$$

$$T_a = 85^\circ\text{C}$$

Calculation of  $R_{thJA,max}$ :

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (V_I \times I_q \text{ can be neglected because of very low } I_q)$$

$$= (13.5 \text{ V} - 5 \text{ V}) \times 100 \text{ mA}$$

$$= 0.85 \text{ W}$$

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D$$

$$= (150^\circ\text{C} - 85^\circ\text{C}) / 0.85 \text{ W} = 76.47 \text{ K/W}$$

## **Application information**

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 76.47 K/W. According to **“Thermal resistance” on Page 8**, the FR4 2s2p board can be used.

### **5.4 Reverse polarity protection**

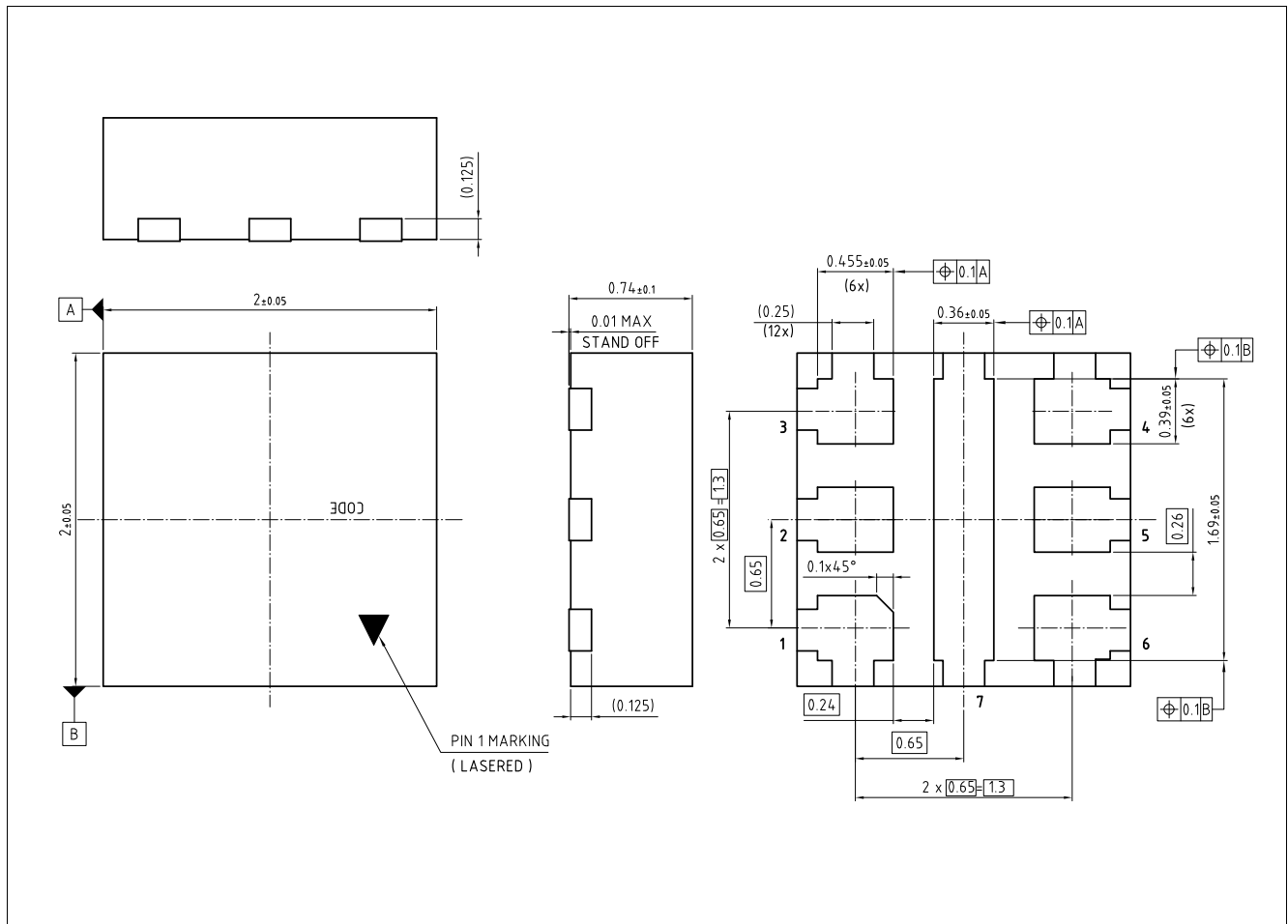
TLS715B0NAV50 is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **“Absolute maximum ratings” on Page 6** must be kept.

### **5.5 Further application information**

- For further information you may contact [www.infineon.com](http://www.infineon.com)

**Package information**

**6 Package information**



**Figure 5 PG-TSNP-7<sup>1)</sup>**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Further information on packages**

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.1	2019-07-31	Editorial change
1.0	2019-02-04	Data Sheet - Initial version

## Trademarks

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**Document reference**

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