TLF80511EJ

Low Dropout Linear Fixed Voltage Regulator

TLF80511EJV50
TLF80511EJV33

Data Sheet

Rev. 1.0, 2014-11-17

Automotive Power

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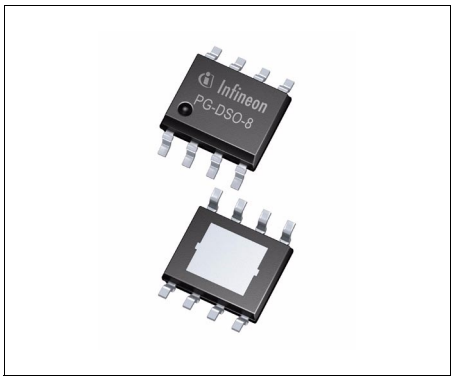
1 Overview



PG-DSO8-EP

Features

- Output Voltage 5 V and 3.3 V
- Output Voltage Precision ±2 %
- Output Current up to 400 mA
- Ultra Low Current Consumption 38 µA
- Very Low Dropout Voltage: 100 mV at 100 mA Output Current
- Extended Operating Range Starting at 3.3 V
- Small Output Capacitor 1 µF
- Output Current Limitation
- Overtemperature Shutdown
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLF80511EJ is a linear low dropout voltage regulator for load currents up to 400 mA. An input voltage of up to 40 V is regulated to $V_{Q,nom}$ = 5 V (TLF80511EJV50) or $V_{Q,nom}$ = 3.3 V (TLF80511EJV33) with ±2 % precision.

The TLF80511EJ with a typical quiescent current of 38 µA, is the ideal solution for systems requiring very low operating currents, such as those permanently connected to a battery.

It features a very low dropout voltage of 100 mV, when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 3.3 V (extended operating range). This makes the TLF80511EJ suitable to supply automotive systems.

In addition, the TLF80511's new fast regulation concept requires only a single, 1 µF output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, over-current and over-temperatures. The TLF80511EJ can be also used in all other applications requiring a stabilized 5 V or 3.3 V supply voltage.

Type	Package	Marking
TLF80511EJV50	PG-DSO8-EP	80511V5
TLF80511EJV33	PG-DSO8-EP	80511V3

2 Block Diagram

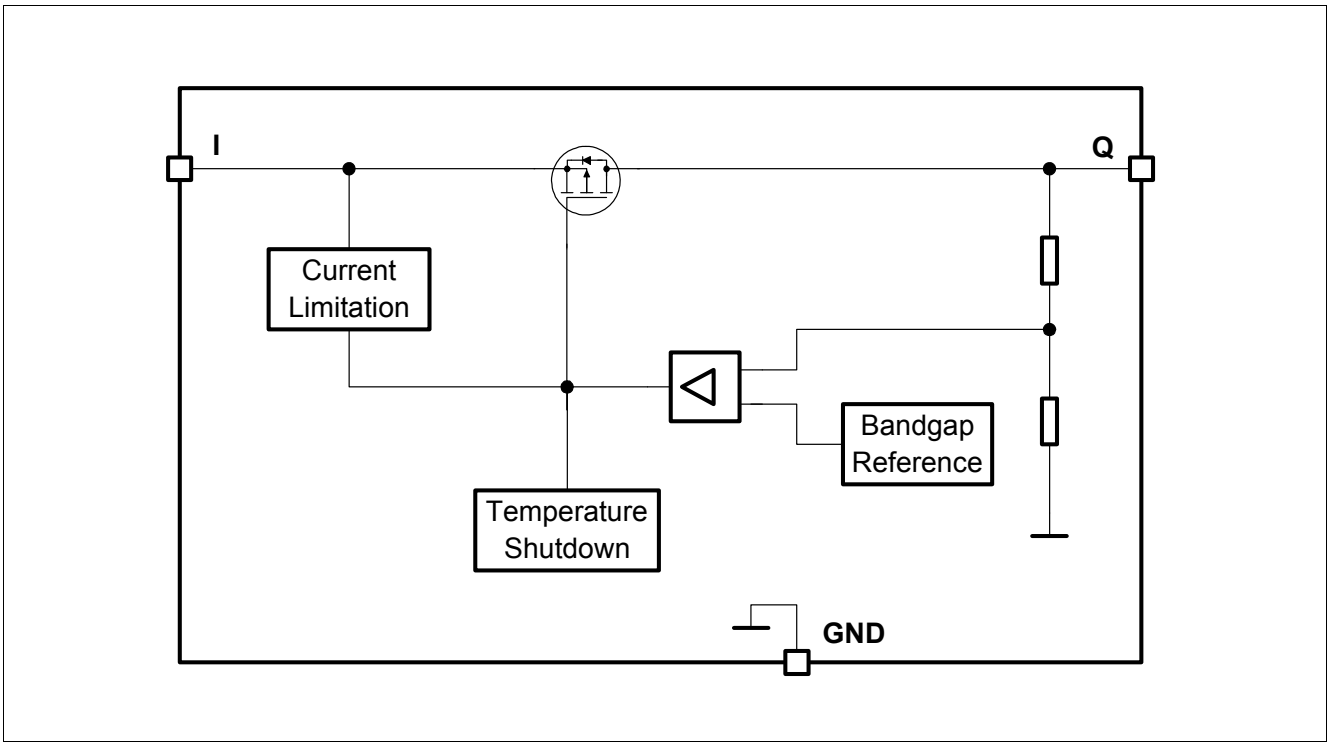


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-DSO8-EP

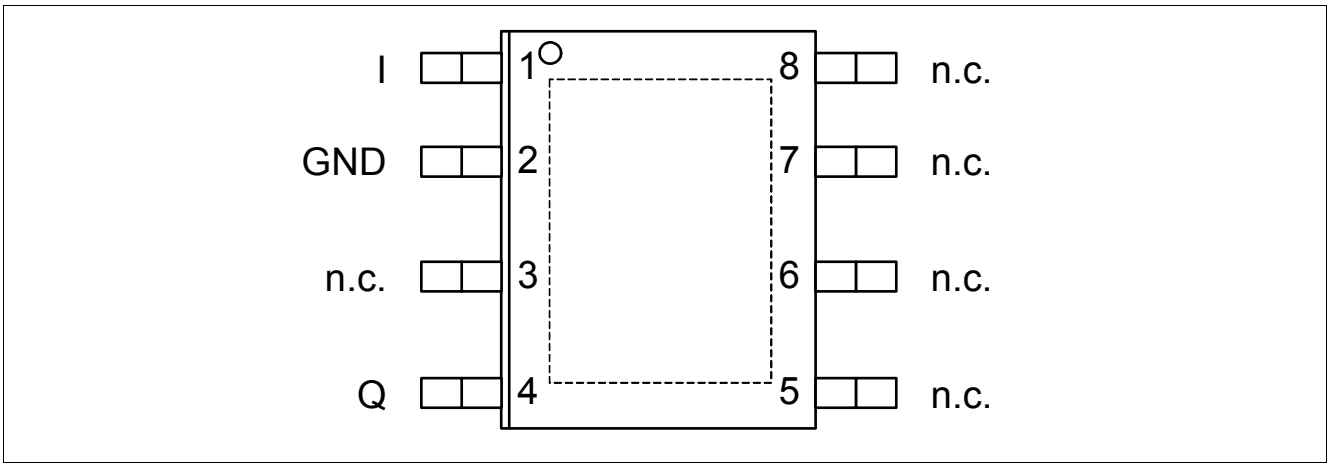


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions PG-DSO8-EP

Pin	Symbol	Function
1	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	GND	**Ground**
3	n.c.	**Not connected** Leave open or connect to GND
4	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance CQ and ESR in the table **“Functional Range” on Page 7**
5, 6, 7, 8	n.c.	**Not connected** Leave open or connect to GND
Pad	-	**Exposed Pad** Connect to heatsink area; Connect with GND on PCB

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	45	V	–	
Output Q							
Voltage	V_Q	-0.3	–	7	V	–	
Temperature							
Junction Temperature	T_j	-40	–	150	°C	–	
Storage Temperature	T_{stg}	-55	–	150	°C	–	
ESD Susceptibility							
ESD Susceptibility	V_{ESD}	-4	–	4	kV	HBM[2)]	
ESD Susceptibility	V_{ESD}	-1.5	–	1.5	kV	CDM[3)]	

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range for Normal Operation	V_I	$V_{Q,nom}$ + V_{dr}	–	40	V	–	
Extended Input Voltage Range	$V_{I,ext}$	3.3	–	40	V	T_j > 25 °C [1]	
Output Capacitor's Requirements for Stability	C_Q	1	–	–	µF	–[2]	
Output Capacitor's Requirements for Stability	$ESR(C_Q)$	–	–	5	Ω	–[3]	
Junction Temperature	T_j	-40	–	150	°C	–	

1) Between min. value and $V_{Q,nom}$ + V_{dr}: V_Q = V_I - V_{dr}. Below min. value: V_Q = 0 V

2) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

3) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Package Version PG-DSO8-EP							
Junction to Case[1]	R_{thJC}	–	11	–	K/W	–	
Junction to Ambient[1]	R_{thJA}	–	41	–	K/W	[2]	
Junction to Ambient[1]	R_{thJA}	–	152	–	K/W	footprint only[3]	
Junction to Ambient[1]	R_{thJA}	–	67	–	K/W	300 mm² heatsink area on PCB[3]	
Junction to Ambient[1]	R_{thJA}	–	56	–	K/W	600 mm² heatsink area on PCB[3]	

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Table 2 "Functional Range" on Page 7** must be maintained. For details see the typical performance graph **"Stability Region: Equivalent Serial Resistor ESR versus Output Current I_Q (TLF80511EJV50)" on Page 11**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor C_I is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the 150° C maximum and significantly reducing the IC's life.

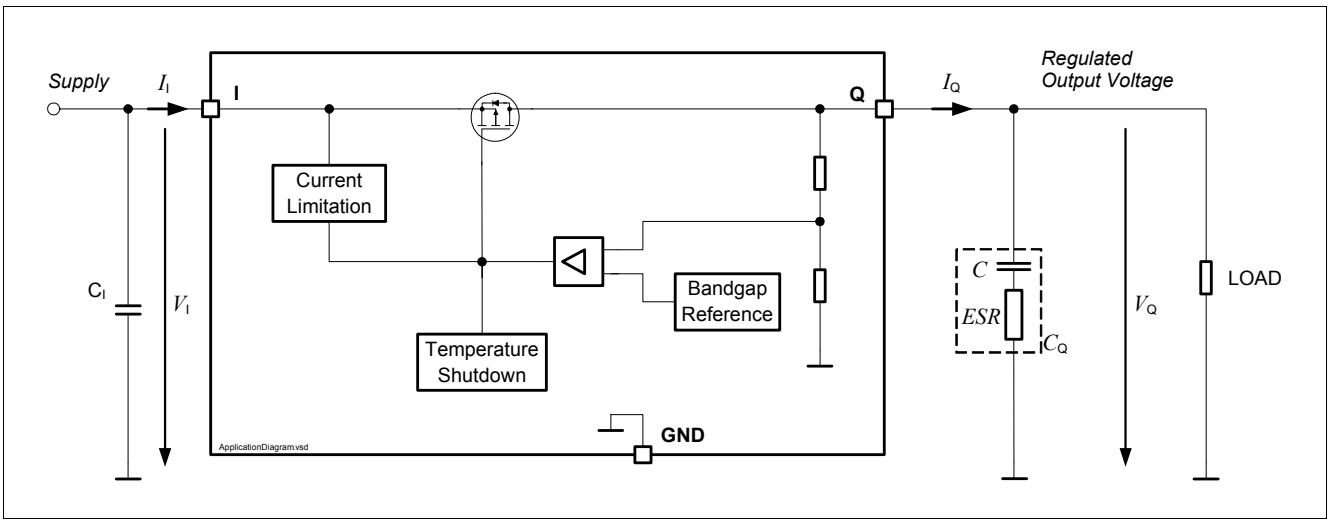


Figure 3 Block Diagram Voltage Regulation

Table 4 Electrical Characteristics Voltage Regulator 5 V and 3.3 V version

V_I = 13.5 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Precision TLF80511EJV50	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 400 mA 6 V < V_I < 28 V	
Output Voltage Precision TLF80511EJV50	V_Q	4.9	5.0	5.1	V	0.05 mA < I_Q < 200 mA 5.5 V < V_I < 40 V	
Output Voltage Precision TLF80511EJV33	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 400 mA 4.4 V < V_I < 28 V	
Output Voltage Precision TLF80511EJV33	V_Q	3.23	3.3	3.37	V	0.05 mA < I_Q < 200 mA 3.9 V < V_I < 40 V	
Output Current Limitation	$I_{Q,max}$	401	600	900	mA	0 V < V_Q < 4.8 V	
Load Regulation steady-state	|ΔVQ,load|	–	20	50	mV	I_Q = 0.05 mA to 400 mA V_I = 6 V	
Line Regulation steady-state	|ΔVQ,line|	–	10	30	mV	V_I = 8 V to 32 V I_Q = 5 mA	
Dropout Voltage[1] V_{dr} = V_I - V_Q TLF80511EJV50	Vdr	–	250	500	mV	I_Q = 250 mA	
Dropout Voltage[1] V_{dr} = V_I - V_Q TLF80511EJV50	Vdr	–	100	–	mV	I_Q = 100 mA	
Dropout Voltage[1] V_{dr} = V_I - V_Q TLF80511EJV33	Vdr	–	320	650	mV	I_Q = 250 mA	
Dropout Voltage[1] V_{dr} = V_I - V_Q TLF80511EJV33	Vdr	–	130	–	mV	I_Q = 100 mA	
Power Supply Ripple Rejection[2] TLF80511EJV50	$PSRR$	–	55	–	dB	f_{ripple} = 100 Hz V_{ripple} = 0.5 Vpp	
Overtemperature Shutdown Threshold	$T_{j,sd}$	151	175	200	°C	T_j increasing[2]	
Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	K	T_j decreasing[2]	

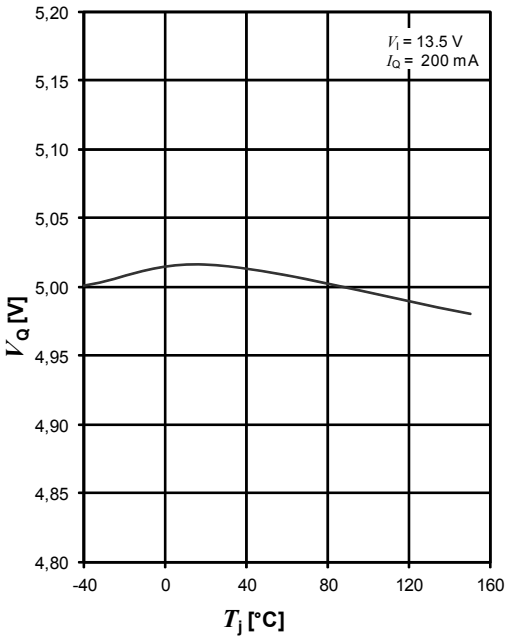
1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5V

2) Not subject to production test, specified by design

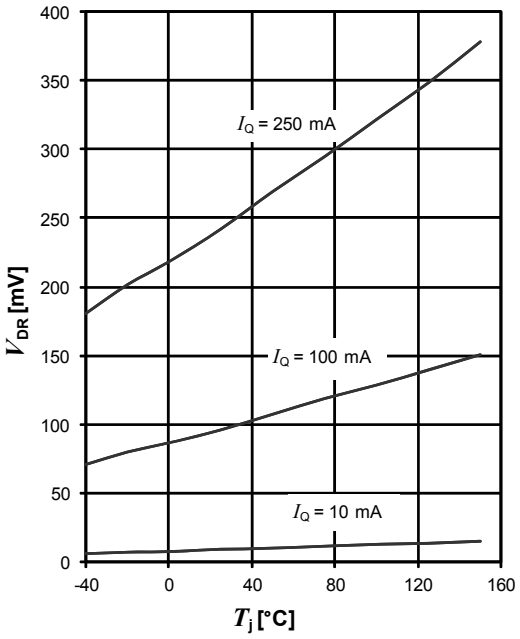
5.2 Typical Performance Characteristics Voltage Regulator

Typical Performance Characteristics

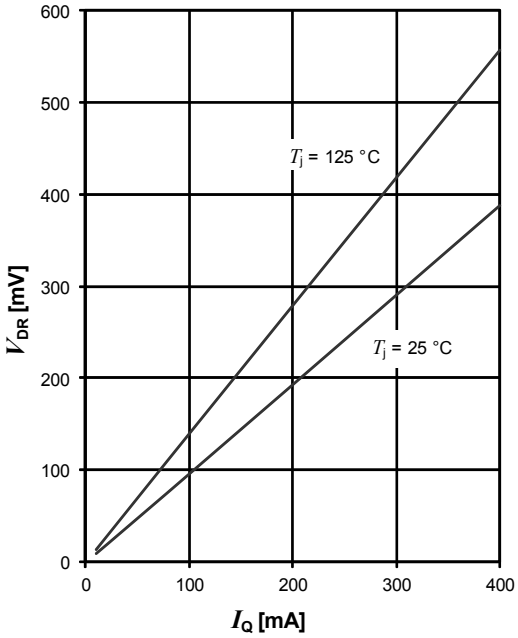
Output Voltage V_Q versus Junction Temperature T_j (TLF80511EJV50)



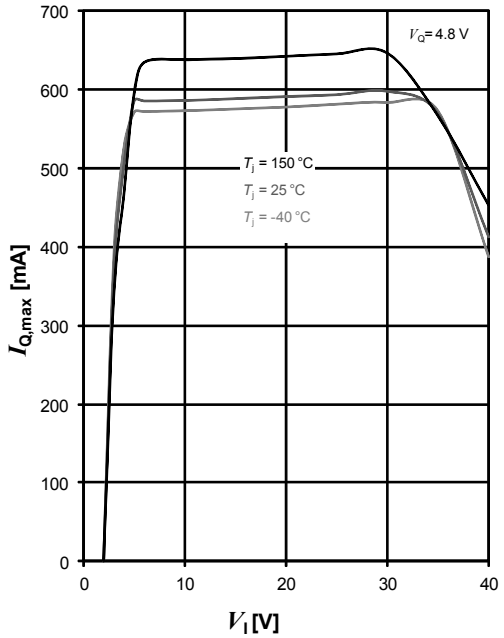
Dropout Voltage V_{dr} versus Junction Temperature T_j (TLF80511EJV50)



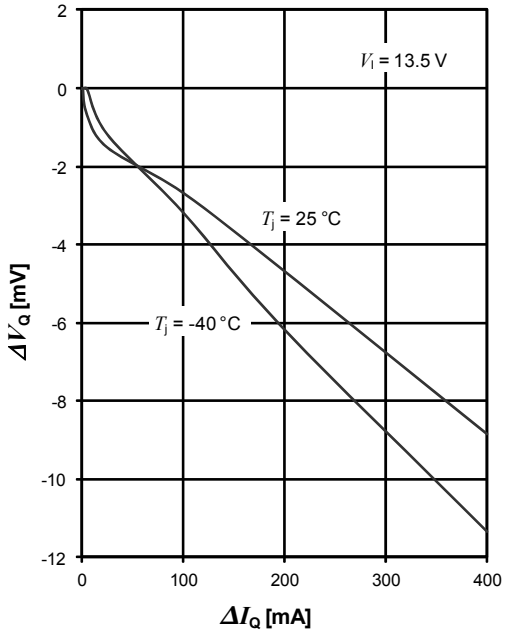
Dropout Voltage V_{dr} versus Output Current I_Q (TLF80511EJV50)



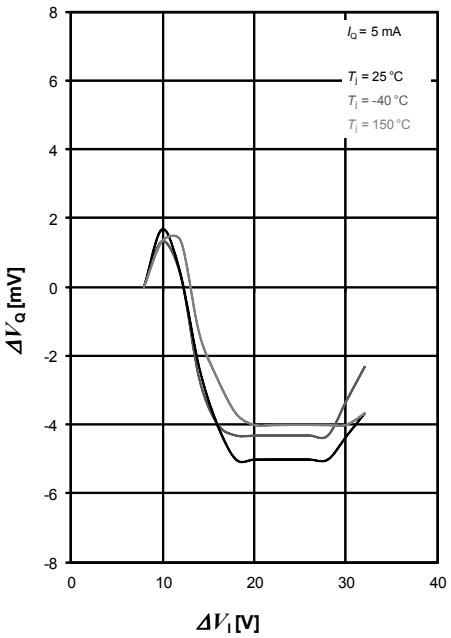
Maximum Output Current I_Q versus Input Voltage V_I (TLF80511EJV50)



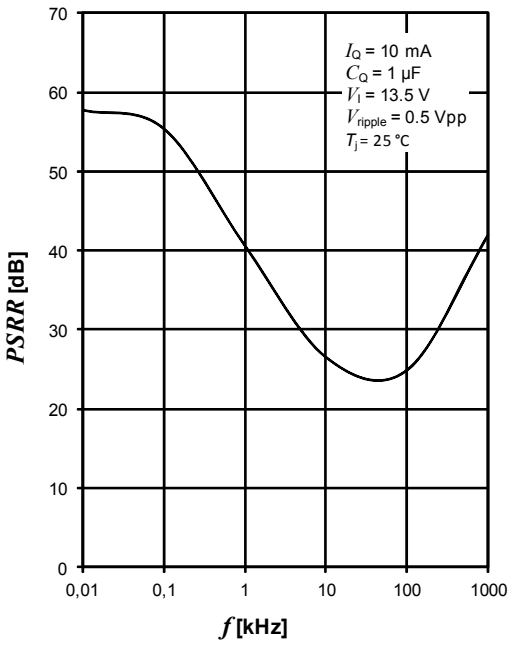
Load Regulation $\Delta V_{Q,load}$ versus Output Current Change ΔI_Q (TLF80511EJV50)



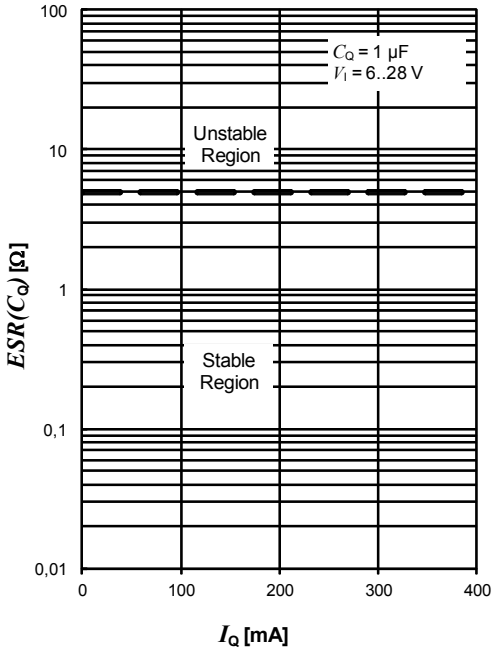
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage ΔV_I (TLF80511EJV50)



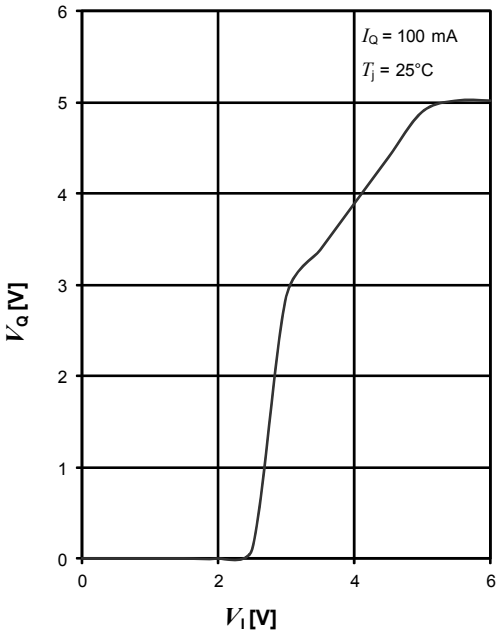
Power Supply Ripple Rejection versus Frequency (TLF80511EJV50)



Stability Region: Equivalent Serial Resistor ESR versus Output Current I_Q (TLF80511EJV50)



Output Voltage V_Q versus
Input Voltage V_I (TLF80511EJV50)



5.3 Current Consumption

Table 5 Electrical Characteristics Current Consumption

V_I = 13.5 V; T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

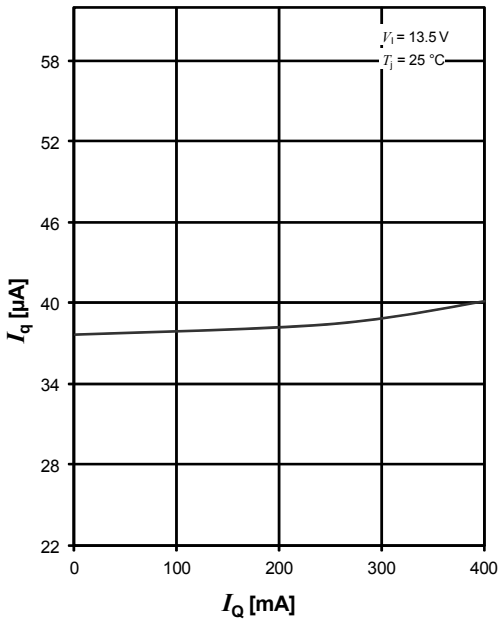
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I - I_Q$	I_q	–	38	46	µA	I_Q = 0.05 mA T_j < 25 °C	
Current Consumption $I_q = I_I - I_Q$	I_q	–	–	75	µA	I_Q = 0.05 mA T_j < 125 °C	
Current Consumption $I_q = I_I - I_Q$	I_q	–	67	80	µA	I_Q = 400 mA T_j < 125 °C[1)]	

1) Not subject to production test, specified by design.

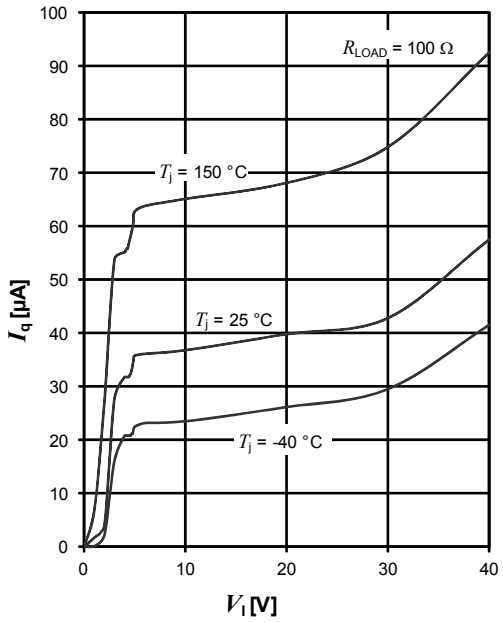
5.4 Typical Performance Characteristics Current Consumption

Typical Performance Characteristics

Current Consumption I_q versus Output Current I_Q (TLF80511EJV50)



Current Consumption I_q versus Input Voltage V_I (TLF80511EJV50)



6 Application Information

6.1 Application Diagram

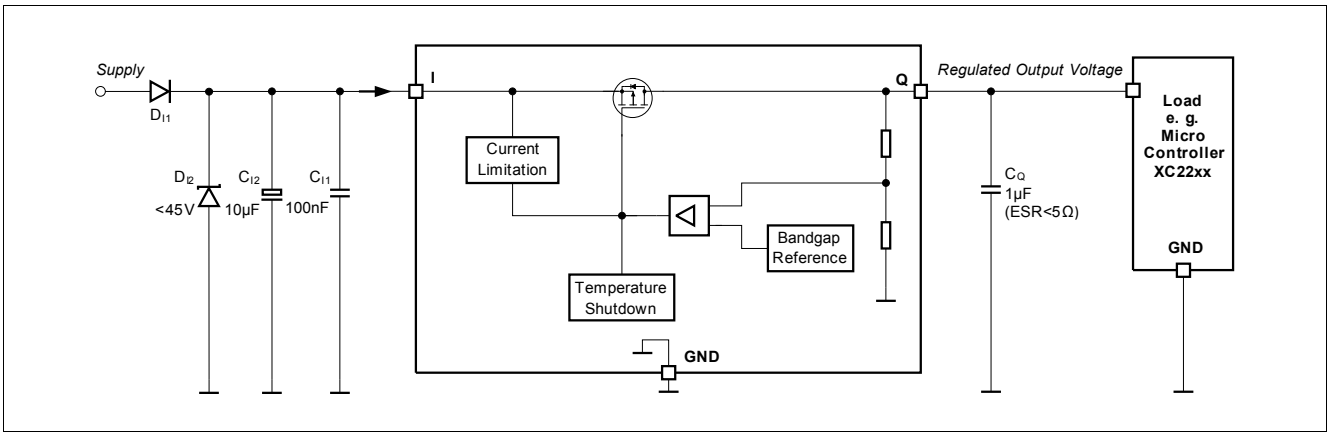


Figure 4 Application Diagram

6.2 Selection of External Components

6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional Range” on Page 7**. The graph **“Stability Region: Equivalent Serial Resistor ESR versus Output Current I_Q (TLF80511EJV50)” on Page 11** shows the stable operation range of the device.

TLF80511EJ is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **“Thermal Resistance” on Page 7**.

Example

Application conditions:

V_I = 13.5V

V_Q = 5V

I_Q = 120mA

T_a = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I – V_Q) \times I_Q + V_I \times I_q$ ($V_I \times I_q$ can be neglected because of very low I_q)

= (13.5V – 5V) × 120mA

= 1.02W

$R_{thJA,max} = (T_{j,max} – T_a) / P_D$

= (150°C – 85°C) / 1.02W = 63.73K/W

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 63.73 K/W. According to **“Thermal Resistance” on Page 7**, at least 600 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

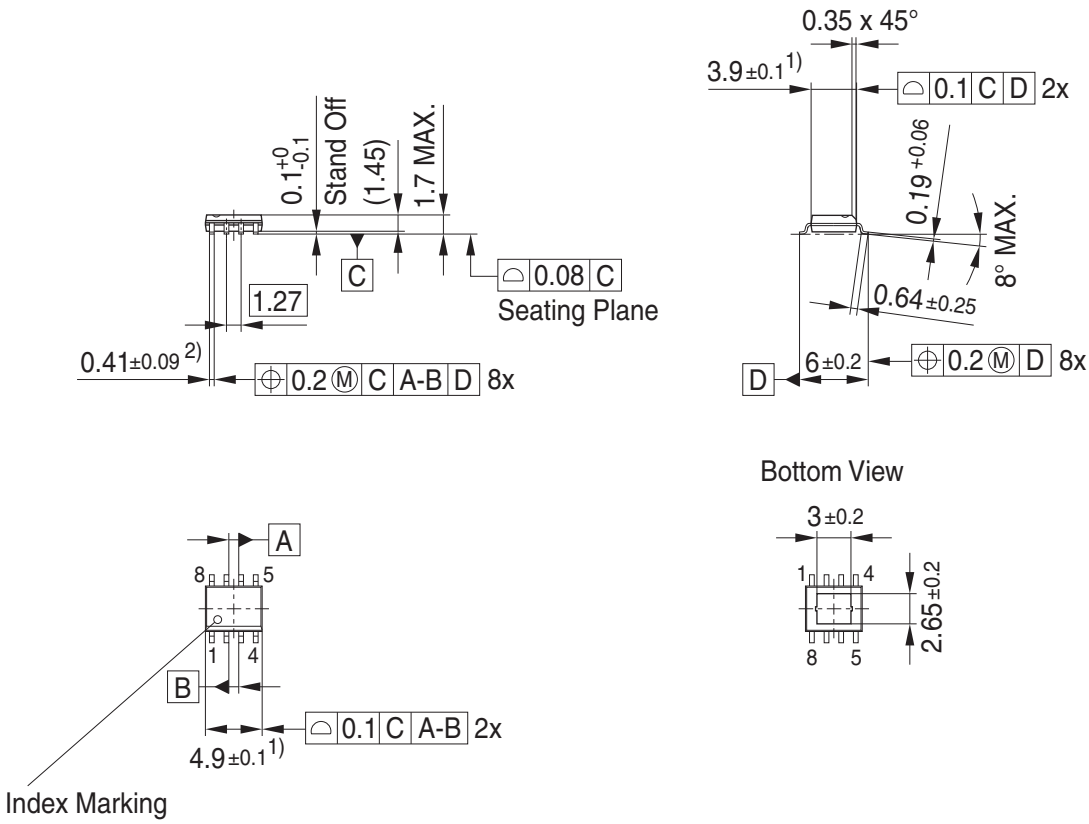
6.4 Reverse Polarity Protection

TLF80511EJ is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 6** must be kept.

6.5 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
3) JEDEC reference MS-012 variation BA

Figure 5 PG-DSO8-EP

7.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**

8 Revision History

Revision	Date	Changes
1.0	2014-11-17	Data Sheet - Initial version

Edition 2014-11-17

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