

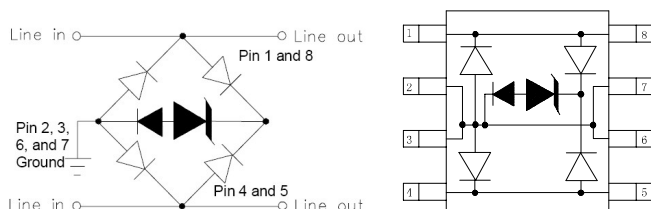
## Description

The LC03-3.3 is a 3.3V low capacitance TVS array, combining a TVS diode with a rectifier bridge to provide both common and differential transient protection in one package. The LC03-3.3 complies with the IEC 61000-4-2 (ESD) with  $\pm 30\text{kV}$  air and  $\pm 30\text{kV}$  contact discharge. It is assembled into a 8-pin lead-free SO-8 package, the LC03-3.3 is rated for GR-1089, intra-building transient immunity requirements for telecommunication installations and provide overvoltage protection for applications such as 10/100/1000 BaseT Ethernet and T3/E3 interfaces.

## Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage: 3.3V
- Ultra low clamping voltage
- Protects two lines in common and differential mode
- JEDEC SO-8 package
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test  
Air discharge:  $\pm 30\text{kV}$   
Contact discharge:  $\pm 30\text{kV}$
  - IEC61000-4-5 (Lightning) 100A (8/20 $\mu\text{s}$ )
- RoHS Compliant

## Dimensions and Pin Configuration



Circuit and Pin Schematic

SO-8 Outline

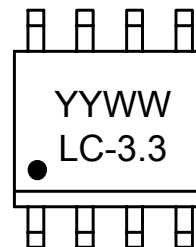
## Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below
- Marking Information: See Below

## Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

## Marking Information



LC-3.3 = Device Marking Code  
 YYWW = Date Code  
 Dot denotes Pin1

## Ordering Information

Part Number	Packaging	Reel Size
LC03-3.3	2500/Tape & Reel	13 inch

**Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise specified)**

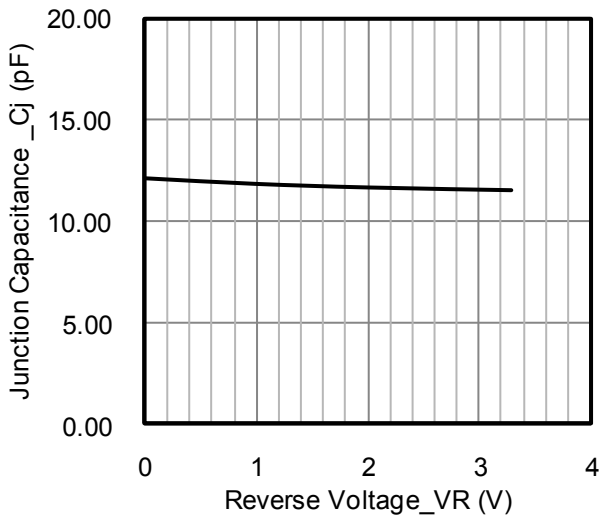
Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20 $\mu\text{s}$ )	Ppk	1800	W
Peak Pulse Current (8/20 $\mu\text{s}$ )	I <sub>PP</sub>	100	A
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	$\pm 30$	kV
ESD per IEC 61000-4-2 (Contact)		$\pm 30$	
Operating Temperature Range	T <sub>J</sub>	-55 to +125	$^{\circ}\text{C}$
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	$^{\circ}\text{C}$

**Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise specified)**

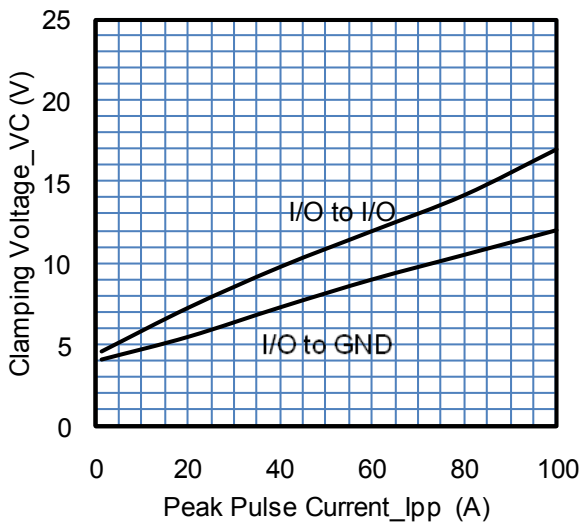
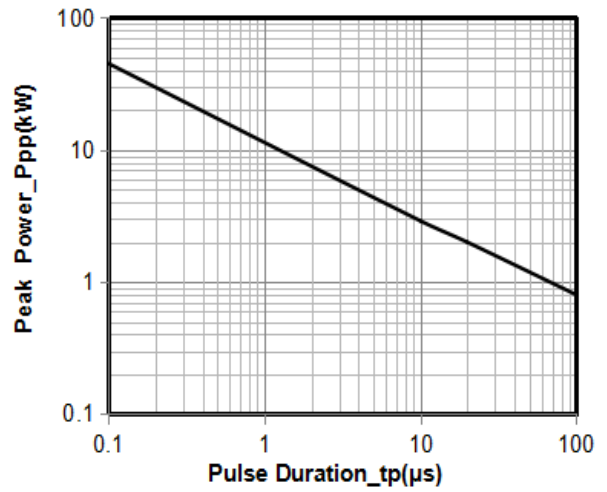
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V <sub>RWM</sub>			3.3	V	
Punch-Through Voltage	V <sub>P</sub>	3.5			V	I <sub>T</sub> = 2 $\mu\text{A}$
Snap-Back Voltage	V <sub>SB</sub>	2.8			V	I <sub>T</sub> = 50mA
Reverse Leakage Current	I <sub>R</sub>			0.5	$\mu\text{A}$	V <sub>RWM</sub> = 3.3V
Clamping Voltage	V <sub>C</sub>			11	V	I <sub>PP</sub> = 50A (8 x 20 $\mu\text{s}$ pulse), any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			13	V	I <sub>PP</sub> = 50A (8 x 20 $\mu\text{s}$ pulse), between I/O pins
Clamping Voltage	V <sub>C</sub>			15	V	I <sub>PP</sub> = 100A (8 x 20 $\mu\text{s}$ pulse), any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			18	V	I <sub>PP</sub> = 100A (8 x 20 $\mu\text{s}$ pulse), between I/O pins
Junction Capacitance	C <sub>J</sub>		16	25	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins and ground
Junction Capacitance	C <sub>J</sub>		8	12	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins

Note 1: I/O pins are Pin 1, 4, 5 and 8

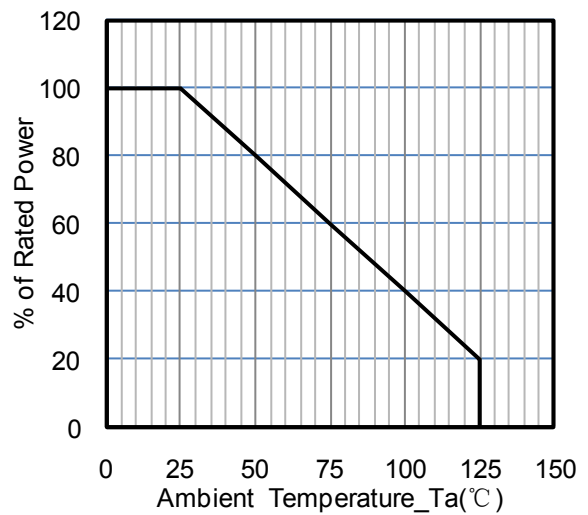
**Typical Performance Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise Specified)**



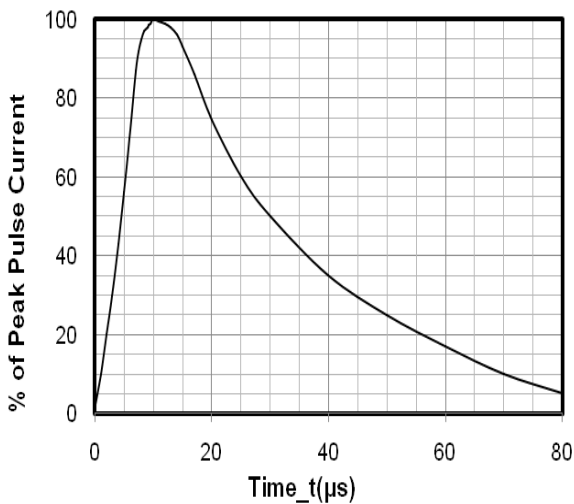
**Junction Capacitance vs. Reverse Voltage**



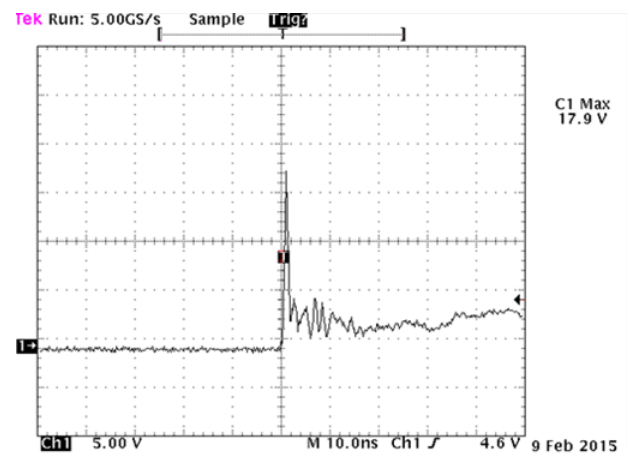
**Clamping Voltage vs. Peak Pulse Current**



**Power Derating Curve**



**8 X 20 $\mu\text{s}$  Pulse Waveform**



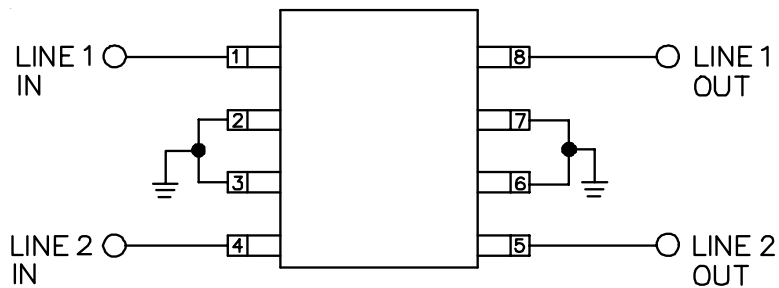
Note: Data is taken with a 10x attenuator

**ESD Clamping Voltage**

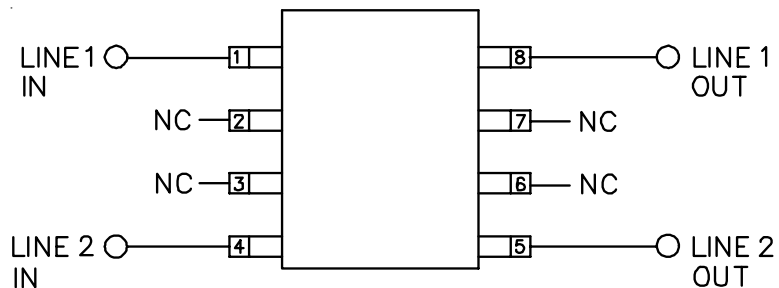
**+8 kV Contact per IEC61000-4-2**

**Typical Application**

The LC03-3.3 is designed to protect two high speed data lines (one differential pair) from transient over-voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.

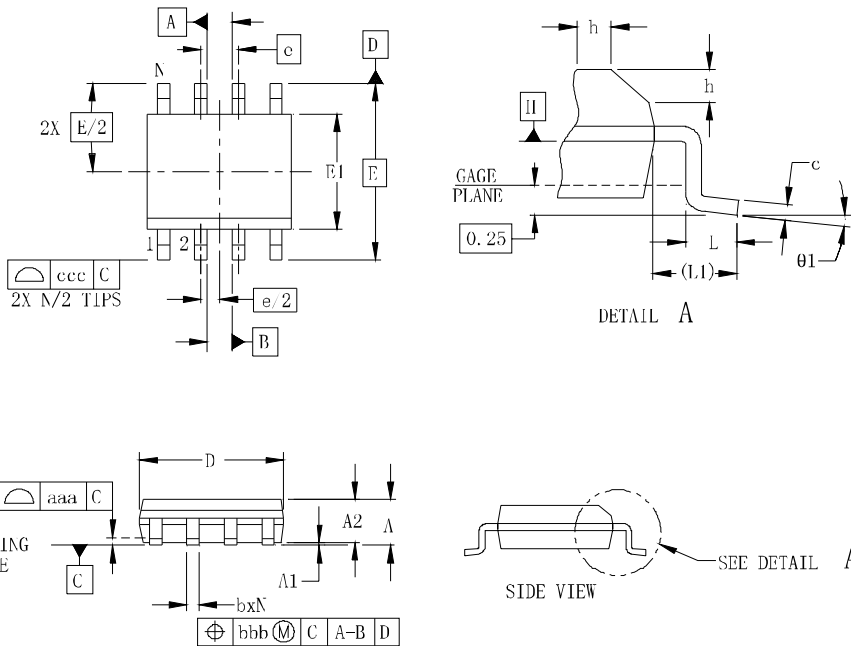


**Connection for differential (Line to Line) and common mode protection (Line to Ground)**



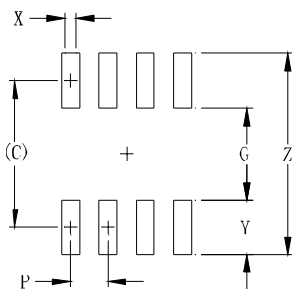
**Connection for differential protection (Line to Line)**

### SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
$\theta 1$	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

### Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	(5.20)	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291

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