AW9201 Single Key Capacitive Controller

FEATURES

- Configurable Touch Sensitivity
- RF Noise Filter
- Automatically Calibrate Varying Environmental Changes
- Intrinsic Capacitance Compensation
- Support Interrupt Output, Open-drain output, Low Active
- Support Compatible I²C Interface, Interface Voltage range of 1.8V ~ 2.8V
- I²C Address: 0x45
- Single Power Supply, Voltage Range: 2.5V-3.6V
- QFN1.6mm×1.6mm_8L Package

APPLICATIONS

Mobile Phones, MID

Portable Media Player

White Goods

GENERAL DESCRIPTION

AW9201 is capacitive single-channel touch sensor. It integrates a precise Capacitance Digital Converter (CDC) and a DSP core for touch detecting.

This device automatically track slow varying environmental changes via special signal processing algorithms. The integrated RF noise filter and touch detection algorithm to ensure the reliability of applications in a variety of environments.

AW9201 provides compatible I²C interface to communicate with MCU, it supports 400kHz fast mode.

AW9201 is available in QFN1.6mm×1.6mm_8L package. Operating voltage range is 2.5V-3.6V.

TYPICAL APPLICATION CIRCUIT

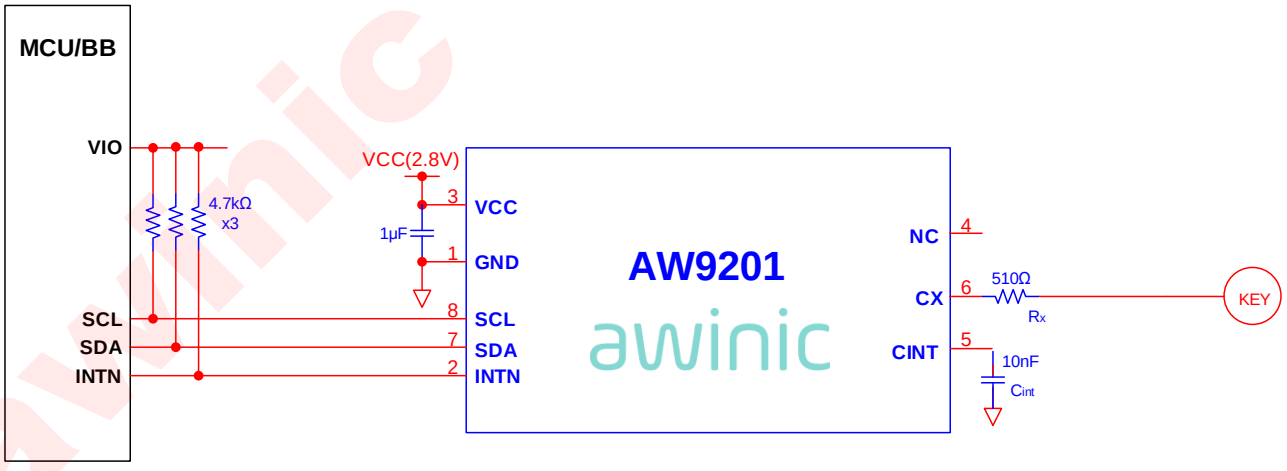
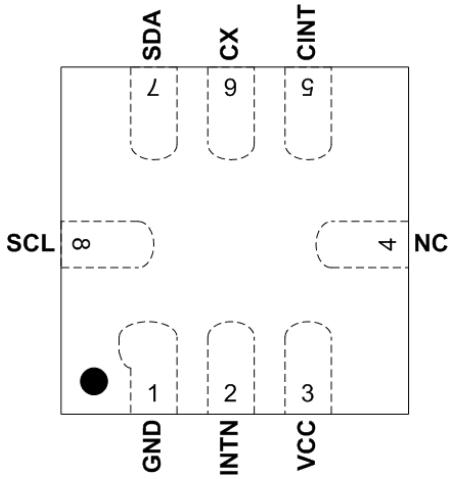


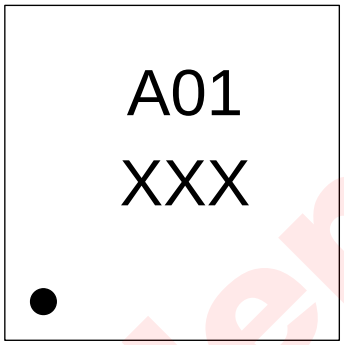
Figure 1 Typical Application Circuit

PIN CONFIGURATION AND TOP MARK

AW9201 TOP VIEW



AW9201 MARK



A01-AW9201QNR
XXX-Manufacture Track Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Power ground.
2	INTN	Interrupt output. Open-drain output and low active. (Typically tie 4.7kΩ resistor to VIO).
3	VCC	Power supply, 2.5 – 3.6V
4	NC	Not connect, floating
5	CINT	Reference capacitance.(10nF).
6	CX	Touch Sensor.
7	SDA	I²C data bus
8	SCL	I²C clock input

FUNCTIONAL BLOCK DIAGRAM

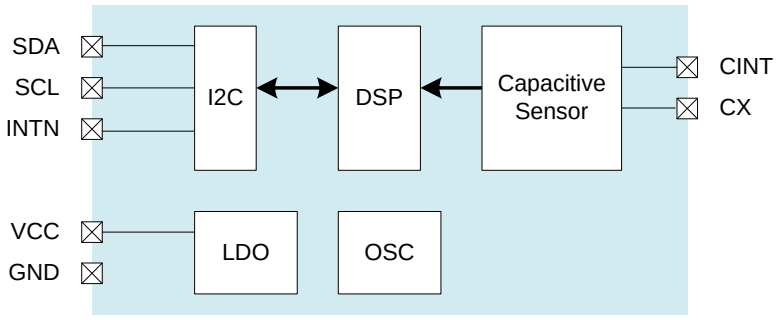


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

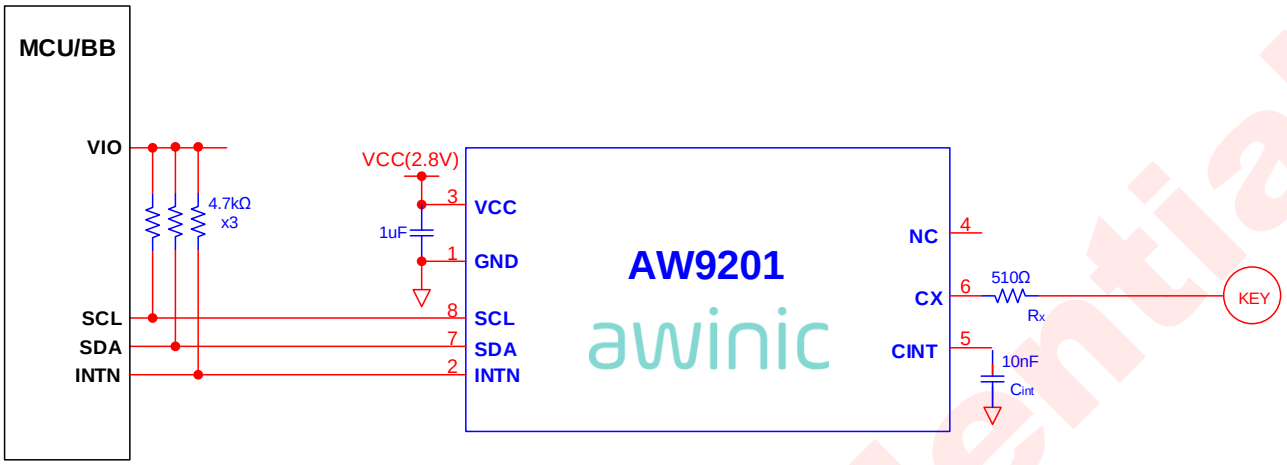


Figure 4 Typical Application Circuit

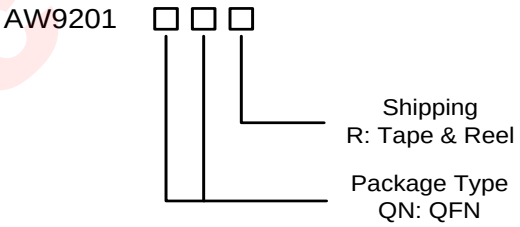
NOTE:

1, *Pin C_X must be connected a 500Ω ~ 600Ω resistance.*

2, *The capacitor C_{int} and resistor R_X need to be as close as possible to the chip placement.*

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW9201QNR	-40℃～85℃	1.6mm×1.6mm×0.75mm QFN1.6mm×1.6mm-8L	A01	MSL3	ROHS +HF	3000units Tape and Reel



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.3V to 3.6V
Input voltage range	SCL, SDA	-0.3V to 3.6V
Output voltage range	SDA, INTN	-0.3V to 3.6V
Junction-to-ambient thermal resistance θ_{JA}		60℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		125℃
Storage temperature T_{STG}		-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 2)		
HBM (human body model)		±4kV
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		+IT：450mA -IT：-450mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7*

ELECTRICAL CHARACTERISTICS

Circuit of Figure 5, VCC=3.0V, T_A=25℃ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Power supply	-	2.5	3.0	3.6	V
$I_{STANDBY}$	Current in Standby mode	GCR=0x00	75	95	115	μA
I_{NORMAL}	Current in Normal mode	GCR=0x02	600	780	880	μA
I_{IDLE}	Current in IDLE mode	GCR=0x02 SCFG3=0x9A	550	680	800	μA
F_{OSC}	Internal oscillator frequency accuracy (16MHz)		14.4	16	17.6	MHz
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL	-0.3		0.45	V
V_{IH}	Logic input high level	SDA,SCL	0.9			V
I_{IL}	Low level input current	SDA,SCL		5		nA

I_{IH}	High level input current	SDA,SCL		5		nA
V_{OL}	Logic output low level	SDA, INTN I_{OUT}=3mA			0.4	V
I_{OL}	Maximum output current	SDA, INTN		2		mA
I_L	Output leakage current	SDA, INTN			1	μA
Accuracy and Range of Measured Capacitance						
$CX_{resolution}$	Resolution(NOTE 3)	CX		0.01		pF
CX_{range}	Range(NOTE 3)	CX		50		pF

NOTE3：the value is test in default configuration.

INTERFACE TIMMING

Parameter Name			MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs

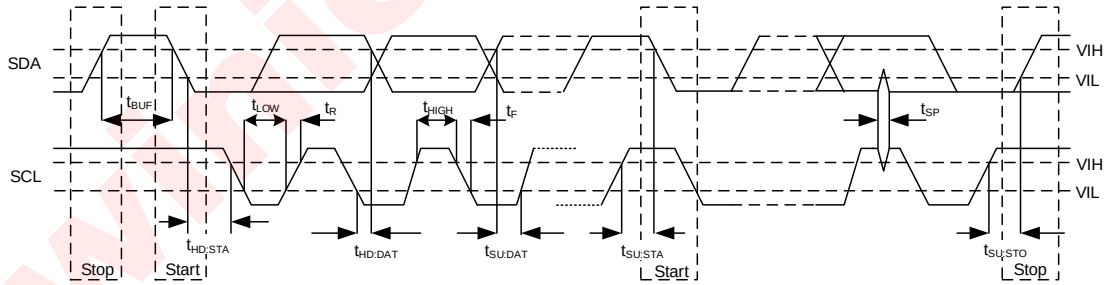


Figure 5 I²C timing

FUNCTIONAL DESCRIPTION

Work Mode

Standby Mode

AW9201 will be in Standby mode after power-up or software reset. At that time, the device is in low power consumption, that the touch detection is disabled while I²C interface is active for communication.

Normal Mode

When the register bit GCR.SENE is set, the chip enter Normal mode. In this mode, AW9201 scans the touch sensor periodically and touch detection is active.

Idle Mode

In Normal mode, when a long time not to touch the key, the AW9201 will automatically enter IDLE mode. In IDLE mode, the AW9201 automatically in the insert wait time between the two scan frames, decrease key capacitor sampling rate, thereby reducing the chip power consumption.
In IDLE mode, once the fingers touch keys, AW9201 immediately back to the Normal mode.

The inserted waiting time is determined by the SCFG3.IPER register.

SCFG3.IPER[2:0]	Inserted Wait Time
000b	1ms
001b	16ms
010b	32ms
011b	48ms
100b	64ms
101b	80ms
110b	96ms
111b	112ms

Reset

Power-up Reset

After power-up, the power-up reset signal is generated, it will reset whole chips and alert a interrupt. User must read the register ISR to clear the interrupt.

Software Reset

Writing 0x55 to register IDRST through I²C interface, will produce a software reset and reset all registers.

Interrupt

INTN pin serves as an interrupt requirement signal. It is an open-drain output, and it is active low.

If no interrupt generated, the INTN port will keep HI-Z output and the pin should be pulled-up by outside resistor connected with power supply; If there's interrupt generated, the INTN port will be driven low. Once an interrupt generated, the master device can read the ISR register to decide which kind of interrupt source and the ISR register will be cleared automatically after the read operation and the INTN pin will return back to HIZ output.

AW9201 has 3 interrupt sources: power-up reset, the touch events and scanning boundary interrupt.

1) Power-up Reset Interrupt

After power-up, this interrupt is generated. This interrupt can not be masked. If the interrupt is generated, user clears it through read register ISR.

2) Scan Boundary Interrupt

When new CDC data is generated, the interrupt active.

This interrupt used for test purpose, it can be masked through writing 0 to register bit SBISE.

3) Touch event Interrupt

AW9201 through the GCR.TIE register enable the interrupt.

When touch detected, the device generates interrupt optionally in two ways (configure register bit GCR.IMD).

GCR.IMD=0: When key status changes, interrupt generated and register ISR.TIS is set to 1.

GCR.IMD=1: When key is ON, generates interrupt; when key released, clear interrupt.

I²C Interface

AW9201 uses a serial bus, which conforms to the I²C protocol to control the chip with two-wire: SCL and SDA. The maximum clock frequency supported is 400 KHz, which is compatible with I²C standard.

Device Address

The I²C device address (7-bit) of AW9201 is 45h, followed by the R/W bit(Read=1/Write=0).

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

1) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
2) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master sends data byte to be written to the addressed register
7) Slave sends acknowledge signal
8) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6,7)
9) Master generates STOP condition to indicate write cycle end

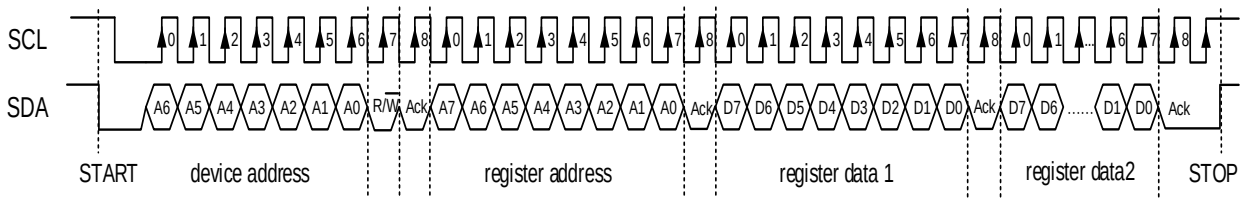


Figure 6 I²C Write Timing

Read Cycle

In a read cycle, the following steps should be followed:

1) Master device generates START condition
2) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master generates STOP condition followed with START condition or REPEAT START condition
7) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
8) Slave device sends acknowledge signal if the slave address is correct.
9) Slave sends data byte from addressed register.
10) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
11) If the master device generates STOP condition, the read cycle is ended.

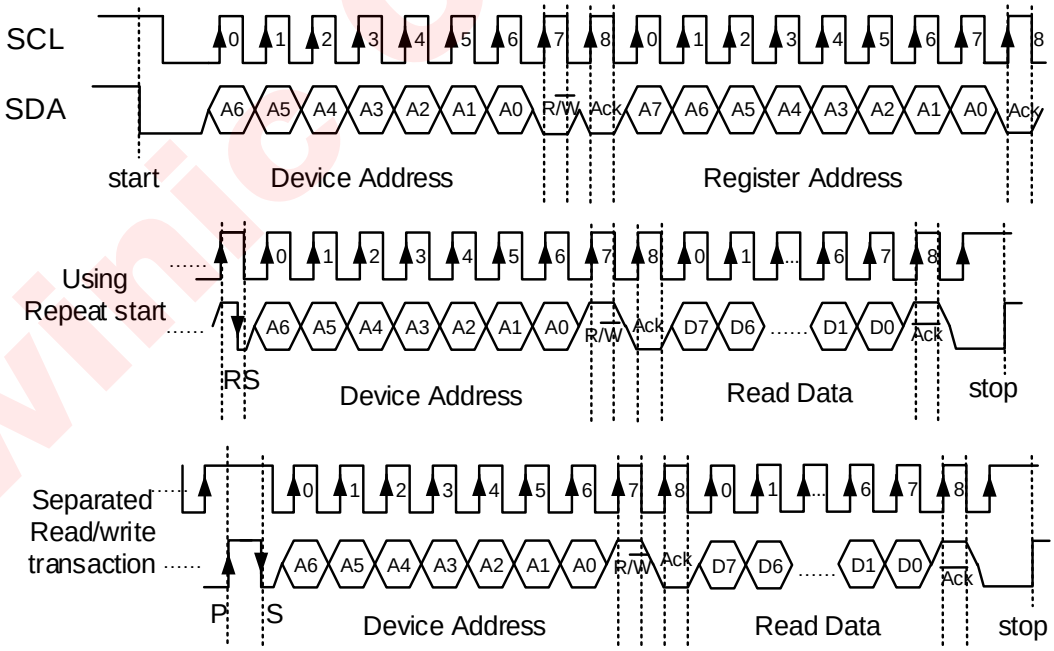


Figure 7 I²C Read Timing

SDA and SCL

The two interface line SCL and SDA should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

The pull-up resistor can be selected in the range of 1k~10KΩ to make the rising time fit with the requirement of I^2C compatible standard. The typical value is 4.7KΩ.

AW9201 can support different high level (1.8V~3.3V) of this two-wire interface. And deglitch circuit is also implemented inside to filter out the glitch in the SCL, SDA line.

Key Detection and Configuration

The Sigma-Delta method of capacitive sensing is employed on AW9201. The capacitance to digital converter (CDC) samples the sensor and generates 16 bit data to integrated processor.

The decision logic is implemented in processor. The processor analyzes data of capacitance measurement, tracks the slow capacitance changes due to environmental factors, and runs decision logic to detect button touches.

Key Status output

The touch state output on register ISR.TS.

If Touch is ON, the register bit ISR.TS is set to 1;if Touch is OFF，clear register bit ISR.TS.

Touch decision

AW9201 has two touch threshold registers: SETTH and CLRTH, the touch threshold is selected by the user to obtain the desired touch sensitivity.

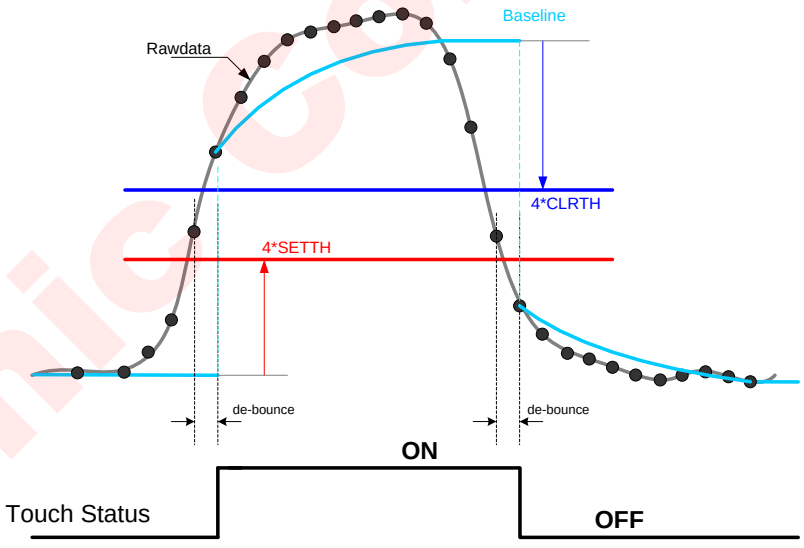


Figure 8 Touch Decision

A touch ON is identified when for at least *2* consecutive capacitance changes (delta) greater than 4×SETTH, A touch OFF is identified when for at least *2* consecutive capacitance changes (delta) lower than 4×CLRTH.

Configurable capacitance resolution

AW9201 provides 4bit (up to 16 stage) capacitance resolution for capacitance measurement (register SCFG1.SENS), with smaller setting value, the higher the resolution.

SCFG1.SENS (binary)	Resolution
0000	capacitance resolution 1 (the maximum resolution)
0001	capacitance resolution 2
0010	capacitance resolution 3
0011	capacitance resolution 4
0100	capacitance resolution 5
0101	capacitance resolution 6
0110	capacitance resolution 7
0111	capacitance resolution 8
1000	capacitance resolution 9
1001	capacitance resolution 10
1010	capacitance resolution 11
1011	capacitance resolution 12
1100	capacitance resolution 13
1101	capacitance resolution 14
1110	capacitance resolution 15
1111	capacitance resolution 16 (the minimum resolution)

Parasitic capacitance compensation

In practical application, the parasitic capacitance is too large, will affect the touch detection. A built-in specialized parasitic capacitance cancellation circuit can as far as possible to eliminate the impact of parasitic capacitance on measurement.

The register SCFG2.OFFSET sets the parasitic capacitance cancellation.

Adaptive Calibration(Environmental variation compensation)

AW9201 detect the capacitance changes based on the baseline, that is an average of sampling data of capacitance for long times. But the changes of the environment (temperature, humidity, voltage and so on) will cause the baseline drift. An adaptive calibration filter in AW9201 tracks environmental changes automatically , ensure reliable detection.

AW9201 can configure the baseline tracking speed through the registers BLTRACES.

RF noise Filter

AW9201 uses a special digital filter to eliminate the interference of 217Hz RF Noise. Through register SCFG2.bit7~bit6 to choose whether or not to open the RF filter .

Frame Period (Sample Rate)

AW9201 continuously transmit N carrier to sensor CX for each CDC conversion period, between two sampling period without waiting time. The carrier number is selected by register SCNUM.

The Frame period is Tscan = 2us×(SCNUM+1) ×4096.

The Maximum Time of Touch ON state

When the time of finger staying in the key exceeds the register MOT, AW9201 will automatically re-initialization baseline and then start a new detection.

MOT	Maximum time of ON state
00b	forever
01b	600×Tscan

10b 11b	2000×Tscan 100×Tscan

REGISTER CONFIGURATION

Address（Hex）	Name	W/R	7	6	5	4	3	2	1	0
00	IDRSTR	R	0	0	1	1	0	0	1	1
01	GCR	WR	0	0	0	IMD	0	TIE	SENE	0
02	ISR	R	0	0	0	PUIS	TIS	0	TS	0
03	-	-	-	-	-	-	-	-	-	-
04	SETTH	WR	SETTH							
05	CLRTH	WR	CLRTH							
06	SCFG1	WR	SENS				SCNUM			
07	SCFG2	WR	RF		0	OFFSET				
08	SCFG3	WR	MOT		IDLEINTIM		FIDLE	IPER		
09	DEB	WR	0	5			TDEB		0	
0A	BLTRACES	WR	0	BLUS			0	BLDS		
0B	BLDTH	WR	BLDTH							
0D	SBISE	WR	0	0	0	0	SBISE	0	0	0
20	SAMPLEH	R	SAMPLEH							
21	SAMPLEL	R	SAMPLEL							
22	LPFH	R	LPFH							
23	LPFL	R	LPFL							
24	DELTAH	R	DELTAH							
25	DELTAL	R	DELTAL							
27	BASELINEH	R	BASELINEH							
28	BASELINEL	R	BASELINEL							
2B	CDCFILTER	WR	0	1	0	0	FILCOEF		0	0
2D	SBIS	R	0	0	0	0	0		0	SBIS

REGISTER DETAILED DESCRIPTION

IDRST，Chip ID and Software Reset

Address：00H， RW							
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol	Description					
7:0	IDRST	1) Chip ID, Read out is 0x33 2) Write 55H，then reset whole chip.					

GCR，Global Control Register

Address：01H，RW							
7	6	5	4	3	2	1	0
0	0	0	IMD	0	TIE	SENE	0
Bit	Symbol	Description					
7:5	-	Reserved. Must be 0.					
4	IMD	Touch Interrupt mode 0: touch events triggered, generates interrupt. 1: touch ON generate interrupt; touch OFF clear interrupt.					
3	-	Reserved. Must be 0.					
2	TIE	Touch Interrupt enable 1: enable 0: disable					
1	SENE	Touch detection function enable 1: enable. Chip in Normal work state					

		0: disable. Chip in Standby state.
0	-	Reserved. Must be 0.

ISR，Status and Interrupt Register

Address：02H，R							
7	6	5	4	3	2	1	0
0	0	0	PUIS	TIS	-	TS	-
Bit	Symbol	Description					
7:5	-	Reserved. Must be 0.					
4	PUIS	Power-up reset interrupt. After power-up, this bit set 1. Clear after read this register. 1: power-up interrupt 0: no interrupt					
3	TIS	Touch interrupt register. Clear after read this register. 1: interrupt generated 0: no interrupt					
2	-	-					
1	TS	Touch state register. 1: Touch ON 0: Touch OFF					
0	-	-					

SETTH，Touch Set Threshold

Address：04H，RW							
7	6	5	4	3	2	1	0
SETTH							
Bit	Symbol	Description					
7:0	SETTH	Touch set threshold. Default is 20H.					

CLRTH，Touch Clear Threshold

Address：05H，RW							
7	6	5	4	3	2	1	0
CLRTH							
Bit	Symbol	Description					
7:0	CLRTH	Touch clear threshold. Default is 14H.					

SCFG1， Scan Control Register 1

Address：06H，RW							
7	6	5	4	3	2	1	0
SENS				SCNUM			
Bit	Symbol	Description					
7:4	SENS	Resolution of Capacitance detection. Default is 07H. 0000b: Resolution 1 (Maximum resolution) 0001b: Resolution 2 0010b: Resolution 3 … 1111b: Resolution 16 (Minimum resolution)					

3:0	SCNUM	The number of scan carrier. Default is 02H. Nc = (SCNUM+1)×4096 The time of sample is Tscan = Nc× 2us.

SCFG2， Scan Control Register 2

Address：07H，RW							
7	6	5	4	3	2	1	0
RF		0	OFFSET				
Bit	Symbol	Description					
7:6	RF	The RF noise filter configure register. 00b: disable 01b: select filter 1 10b: select filter 2 11b: select filter 3					
5	-	Reserved. Must be 0.					
4:0	OFFSET	Parasitic Capacitance Compensation selection. 00000b: no compensate 00001b: compensate capacitance is 2×$C_{full\text{-}scale}$ /16 00010b: compensate capacitance is 3×$C_{full\text{-}scale}$ /16 …….. 11111b: compensate capacitance is 32×$C_{full\text{-}scale}$ /16					

SCFG3， Scan Control Register 3

Address：08H，RW							
7	6	5	4	3	2	1	0
MOT		IDLEINTIM		FIDLE	IPER		
Bit	Symbol	Description					
7:6	MOT	Maximum time of Touch ON state. AW9201 stay in touch ON state for long than MOT setting, will automatically re-initialization baseline, start a new detection. 00: disable 01: N = 600 (600×Tscan) 10: N = 2000 (2000×Tscan) 11: N = 100 (100×Tscan)					
5:4	IDLEINTIM	AW9201 stay in touch OFF state for long than IDLEINTIM setting, will enter IDLE state. 00： never 01： N=64 (64×Tscan) 10： N=256 (256×Tscan) 11： N=1024 (1024×Tscan)					
3	-	Reserved. Must be 0.					
2:0	IPER	In IDLE state, AW9201 insert waiting time to reduce sample rate. Default value is 02H. 000: 0ms 001: 16ms 001: 32ms 011: 48ms 100: 64ms 101: 80ms					

		110: 96ms 111: 112ms

TDEB， Touch De-bounce Configuration Register

Address：09H, RW							
7	6	5	4	3	2	1	0
0	5			TDEB		0	
Bit	Symbol	Description					
7:4	-	Reserved. Must set 101b.					
3:2	TDEB	Touch De-bounce configuration. For consecutive N times the capacitance changes(delta) is great than touch threshold, determined touch ON. 00b: 2 times 01b: 4 times 10b: 6 times 11b: 8 times					
1:0	-	Reserved. Must set 0.					

BLTRACE， Tracing Baseline Configuration Registers

Address : 0AH, RW							
7	6	5	4	3	2	1	0
0	BLUS			0	BLDS		
Bit	Symbol	Description					
6:4	BLUS	Baseline up tracing filter control. Default is 3. In touch off state, when consecutive BLUS×2 times the sample data greater than baseline, then baseline increment 1.					
2:0	BLDS	Baseline down tracing filter control. Default is 3. In touch off state, when consecutive BLDS×2 times the sample data less than baseline, then baseline decrease 1.					

BLDTH， Baseline Down Threshold

Address : 0BH, RW							
7	6	5	4	3	2	1	0
BLDTH							
Bit	Symbol	Description					
7:0	BLDTH	Default is 8. When continuous samples is less than the baseline, and this difference is too large(greater then BLDTH×2), will re-initializes baseline.					

SBISE， Scan boundary Interrupt Enable

Address : 0DH, RW							
7	6	5	4	3	2	1	0
SBISE							
Bit	Symbol	Description					
7:4	-	Reserve bits, should be 0					
3	SBISE	Interrupt enable. 1, enable scan boundary interrupt. 0, disable.					
2:0	-	Reserve bits, should be 0					

DEBUG, Debug Data Registers

Address	Name	Description
20H	SAMPLEH	CDC Raw-data high 8 bit
21H	SAMPLEL	CDC Raw-data Low 8 bit
22H	LPFH	Filtered CDC data high 8 bit
23H	LPFL	Filtered CDC data low 8 bit
24H	DELTAH	Capacitance changes data high 8bit
25H	DELTAL	Capacitance changes data low 8bit
26H	BASELINEH	Long term average CDC data high 8 bit
27H	BASELINEL	Long term average CDC data low 8 bit

CDCFILTER， CDC Data Filter Setting

Address: 2BH, RW							
7	6	5	4	3	2	1	0
0	1	0	0	FILCOEF		0	0
Bit	Symbol	Description					
7:4	-	Reserved. Must set 0100b.					
3:2	FILCOEF	CDC filter coefficient . Default is 11b. 00：1/4 01：1/8 10：1/2 11：bypass					
1:0	-	Reserved. Must set 1.					

SBIS， Scan Boundary Interrupt

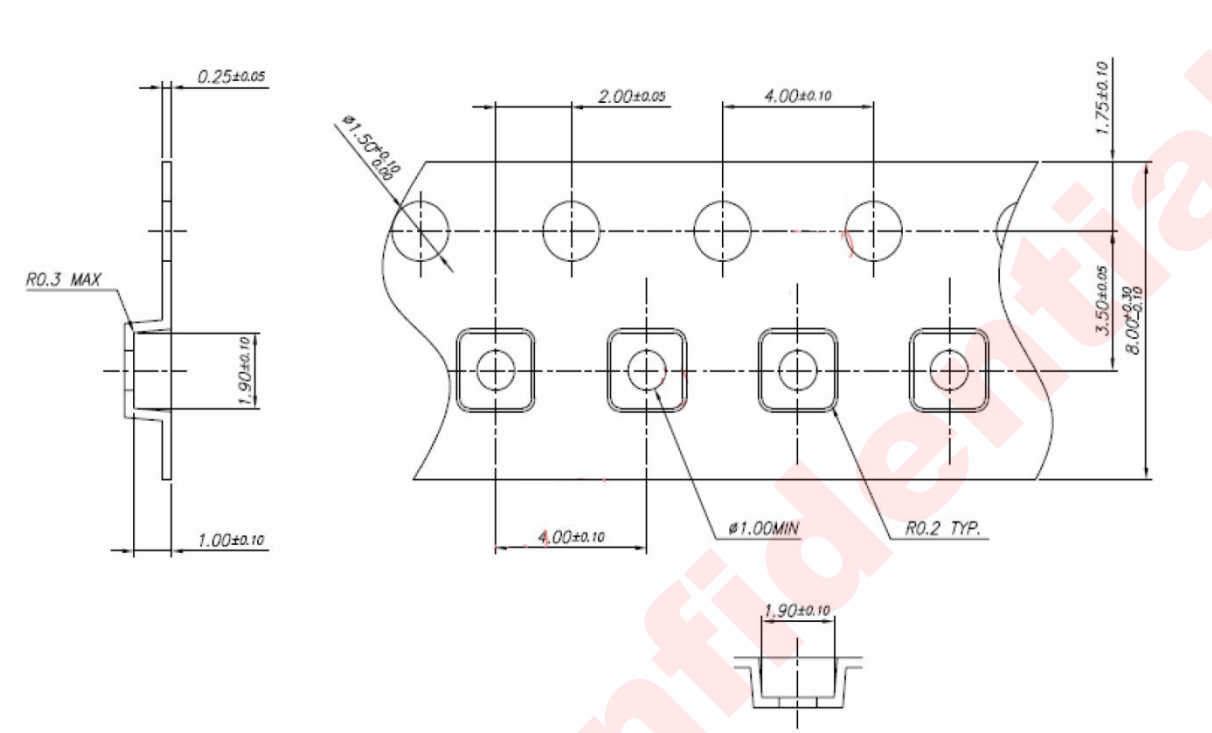
Address : 2DH, R							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	SBIS
Bit	Symbol	Description					
7:6	-	Read out 0.					
0	SBIS	After SBIS, the new CDC is generated. This bit is cleared after read. 1: Interrupt 0: no Interrupt					

PCB LAYOUT CONSIDERATION

AW9201 is a capacitive sensor, to obtain the optimal performance, PCB layout should be considered carefully. Refer to are users guide.

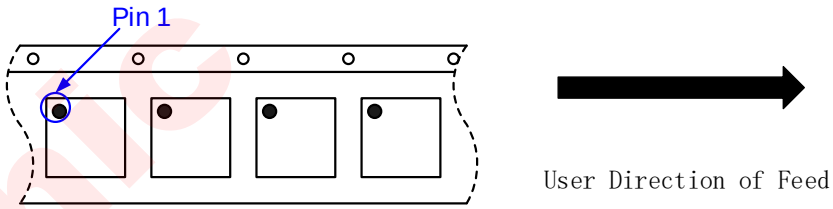
TAPE AND REEL INFORMATION

Carrier Tape

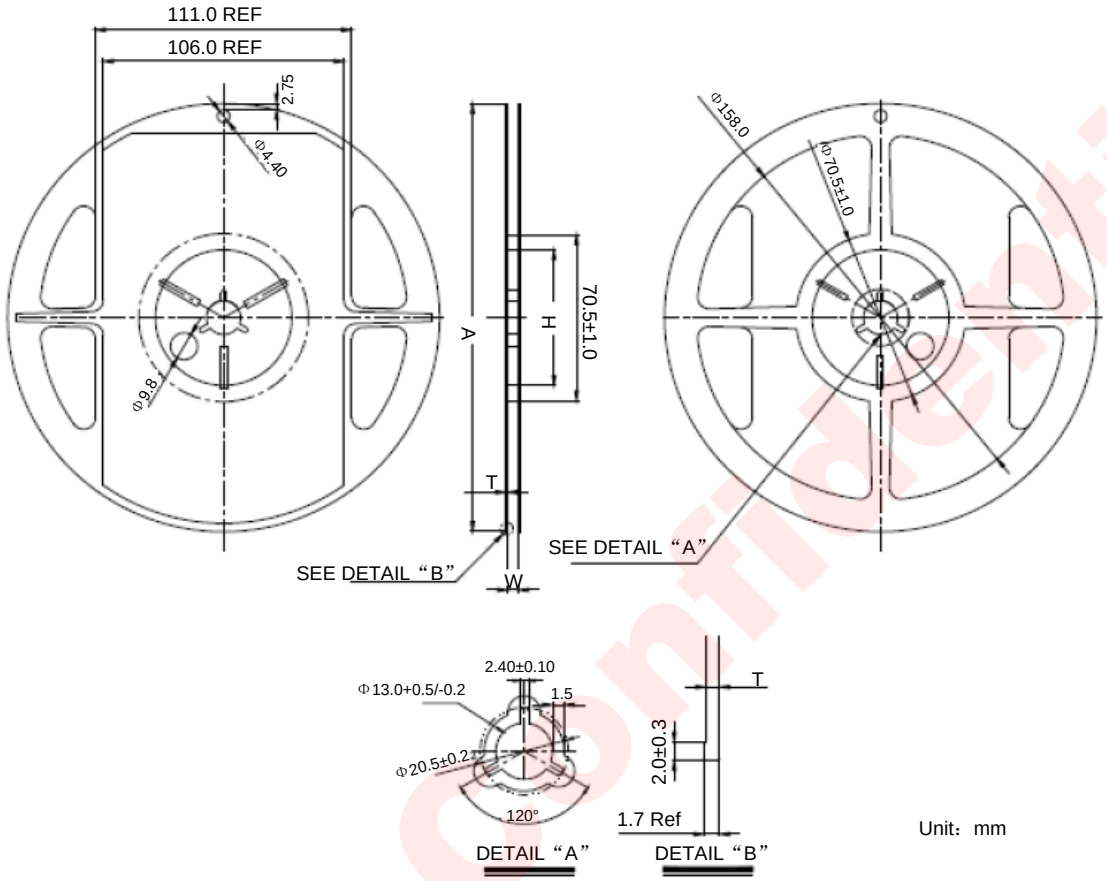


NOTE：All Dimensions in Millimeters.

Pin 1 direction



Reel



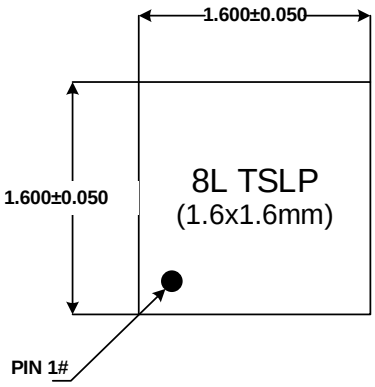
Unit：mm

P/N	A±1.0	H±1.0	T±0.3	W±0.5
RD27608(-BK,-BL)	Φ178.0	Φ60.0	1.40	9.0
RS27608(-BK,-BL)	Φ178.0	Φ60.0	1.40	9.0
RD27612(-BK,-BL)	Φ178.0	Φ60.0	1.40	13.2
RS27612(-BK,-BL)	Φ178.0	Φ60.0	1.40	13.2

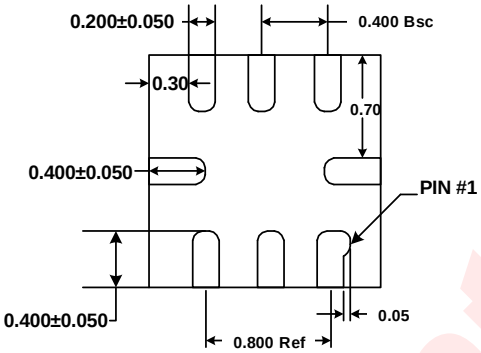
Notes:

1. RD stands for Reel Dipped;
2. RS stands for Reel Standard;
3. BK stands for black Reel;
4. BL stands for blue Reel;

PACKAGE DESCRIPTION

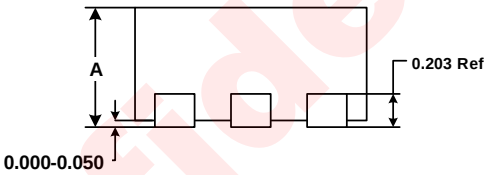


TOP VIEW



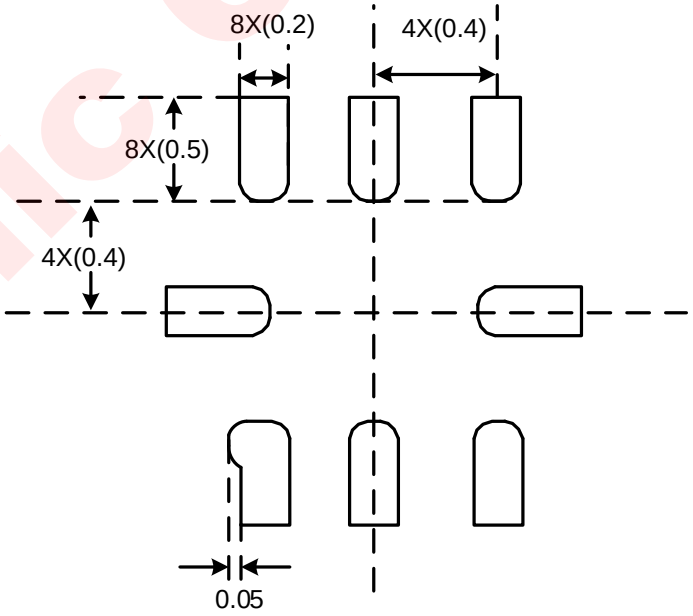
BOTTOM VIEW

		TSLP
A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700



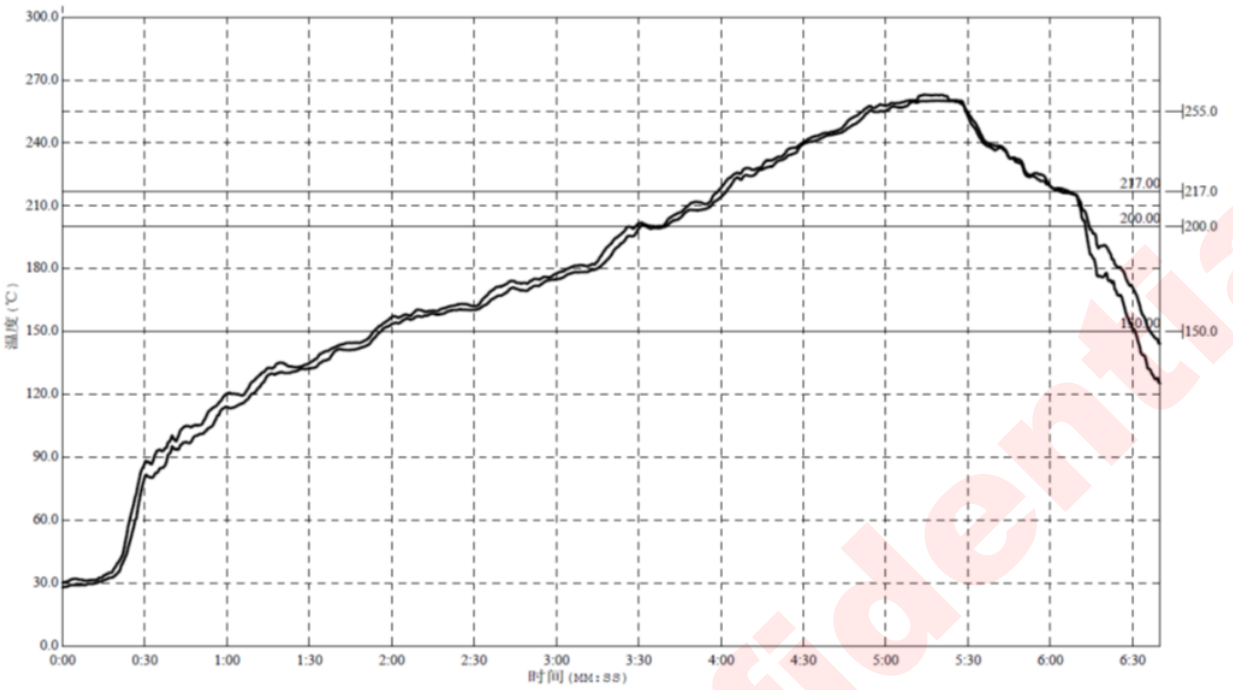
SIDE VIEW

RECOMMENDED LAND PATTERN



TOP VIEW

REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

Package Reflow Standard Profile

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW9201 adopted the Pb-Free assembly.

REVISION HISTORY

Vision	Date	Change Record
V1.0	Oct. 2014	Officially Released
V1.0.1	May 2016	Update Ordering Information
V1.0.2	Sep. 2016	Update Package Description
V1.1	Nov. 2017	Remove the Chinese description Update the ordering information
V1.2	Sep. 2018	Update the storage temperature

RELATED PARTS

Part No.	Description	Comments
AW9136 QNR	Capacitive Key and LED Driver Controller	QFN3×3-20L, 3 channel capacitive key and 6 channel LED controller
AW9163 QNR	Capacitive Key and LED Driver Controller	QFN3×3-20L, 6 channel capacitive key and 3 channel LED controller

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