

CMOS Presettable Up/Down Counter (Dual Clock With Reset)

High-Voltage Types(20-Volt Rating)

XD40192-BCD Type

XD40193-Binary Type

■XD40192 Presettable BCD Up/Down Counter and the XD40193 Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET . Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

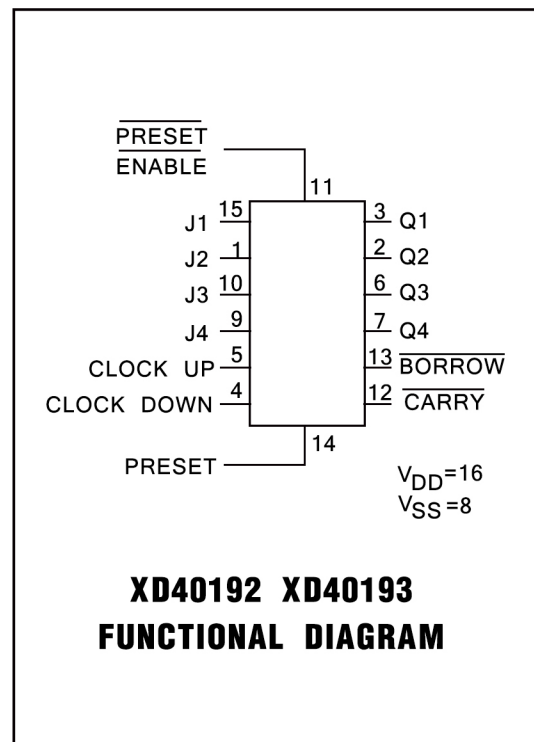
The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

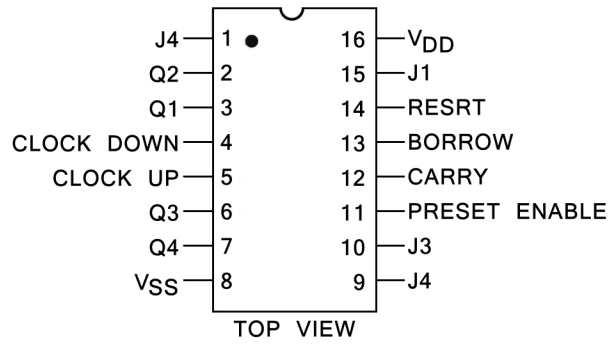
Features:

- Individual clock lines for counting up or counting down
- Synchronous high-speed carry and borrow propagation delays for cascading
- Asynchronous reset and preset capability
- Medium-speed operation- $f_{\text{CL}} = 8 \text{ MHz (typ.) @ } 10 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\mu\text{A}$ at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin over full package temperature range:
 - 1 V at $V_{\text{DD}} = 5\text{V}$ 2 V at $V_{\text{DD}} = 10\text{V}$
 - 2.5V at $V_{\text{DD}} = 15\text{V}$

Applications:

- Up/down difference counting
- Multistage ripple counting
- Synchronous frequency dividers
- A/D and D/A conversion
- Programmable binary or BCD counting





XD40192 XD40193
TERMINAL ASSIGNMENT

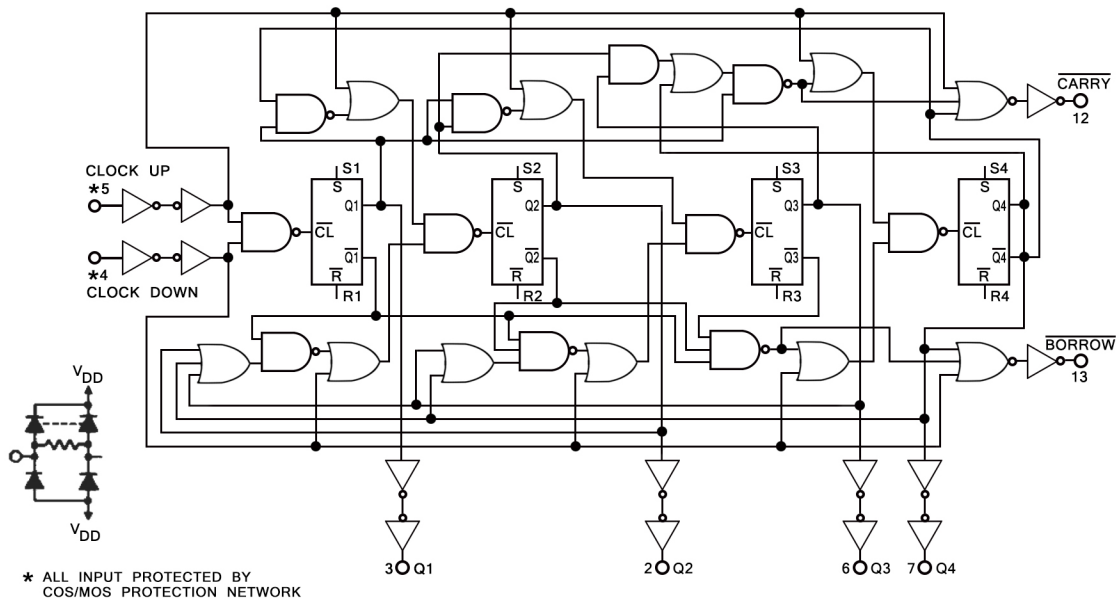
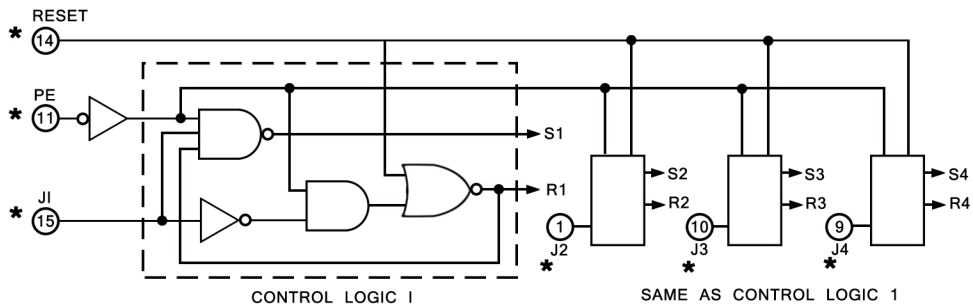


Fig.1-XD40192 logic diagram(BCD).

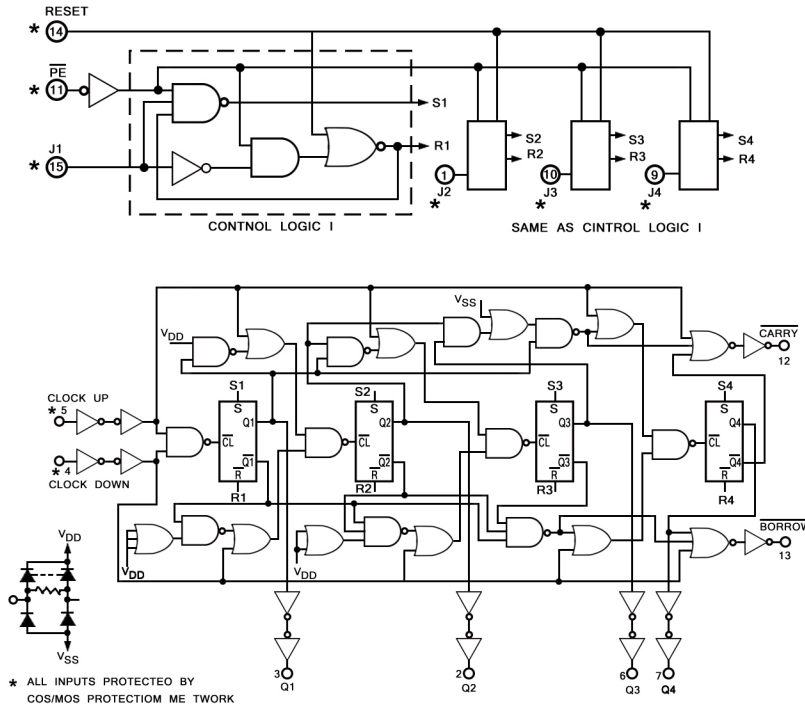


Fig.2-XD40193 logic diagram (binary).

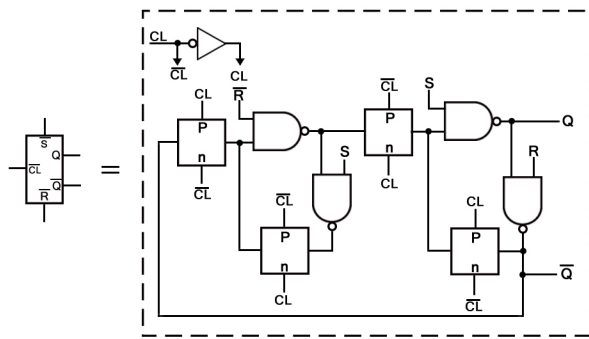


Fig.4 -Internal logic of Flip-flop.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
	1	1	0	COUNT UP
	1	1	0	NO COUNT
1		1	0	COUNT DOWN
1		1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	PESET

1=HIGH LEVEL

0=LOW LEVEL

X=DON'T CARE

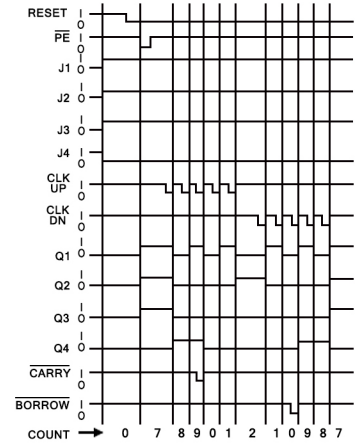


Fig.3 -XD40192 timing diagram.

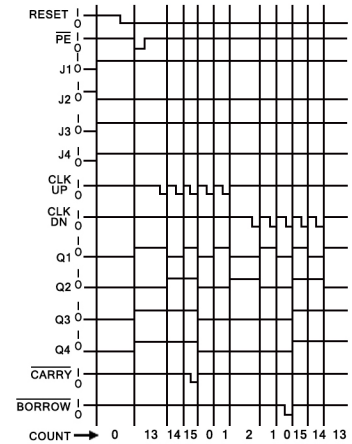


Fig.5 -XD40193 timing diagram.

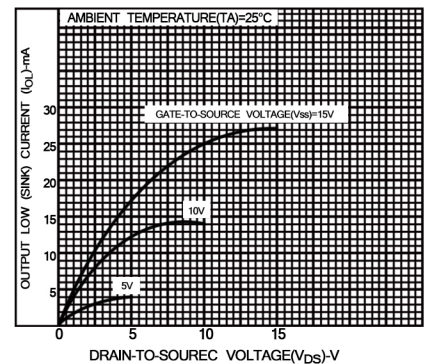


Fig.6 -Typical output low (sink) current characteristics.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY -VOLTAGE RANGE, (VDD)

Voltages referenced to Vss Terminal) -0.5Vto+20V

INPUT VOLTAGE RANGE, ALL INPUTS. -0.5VtoVDD+0.5V

DC INPUT CURRENT, ANY ONE INPUT. ±10mA

POWER DISSIPATION PER PACKAGE (PD):

For TA = -55°C to +100°C 500mW

For TA = +100°C to +125°C. Derate Linearity at 12mW/°Cto 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types).100mW

OPERATING-TEMPERATURE RANGE (TA)-55°C to+ 125°C

STORAGE TEMPERATURE RANGE (Tstg) -65° to+ 150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance1/6±1/32 inch (1.59±0.79mm) from case for 10s max +265°C

RECOMMENDED OPERATING CONDITIONS at TA = 25°C (unless otherwise specified)

For maximum reliability, nominal operating conditions should be. selected so that operation is a/ways within the following ranges.

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For TA =Full Temp. Range)	-	3	18	V
Removal Time: RESET or PE	5	80	-	ns
	10	40	-	
	15	30	-	
Pulse Width: RESET	5	480	-	ns
	10	300	-	
	15	260	-	
PE	5	240	-	ns
	10	170	-	
	15	140	-	
CLOCK	5	180	-	ns
	10	90	-	
	15	60	-	
Clock Input Frequency	5	DC	2	MHz
	10	DC	4	
	15	DC	5.5	
Clock Rise & Fall Time	5	-	15	μs
	10	-	15	
	15	-	5	

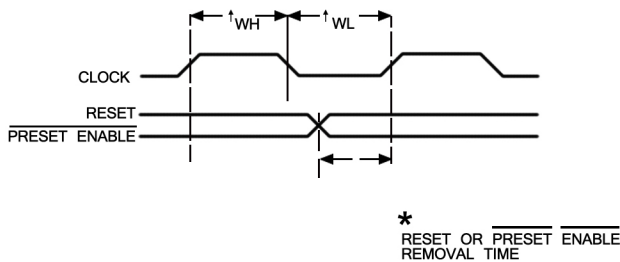


Fig.10 -Timing diagram defining trem.

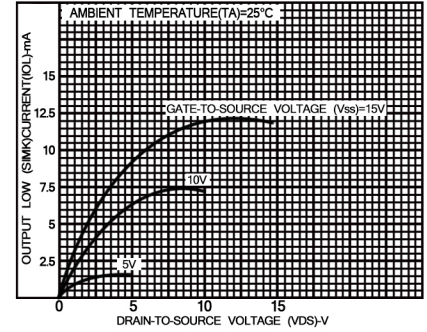


Fig.7 -Minimum output low (sink) current characteristics.

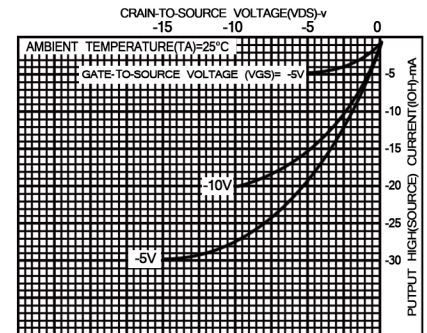


Fig.8 -Typical output high (source) current characteristics.

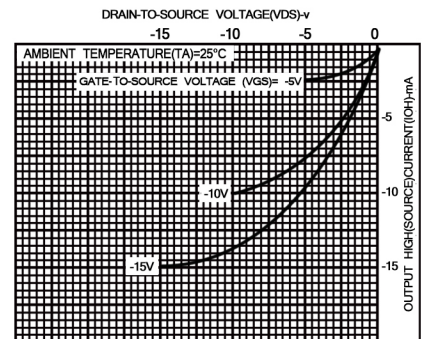


Fig.9 -Minimum output high (source) current characteristics.

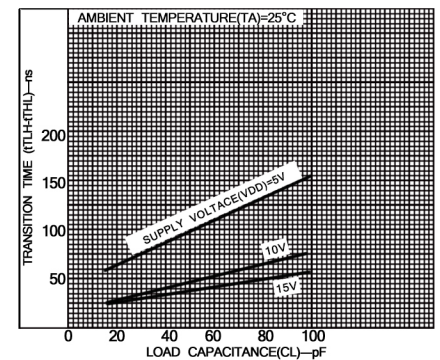


Fig.11 -Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES(°C)							UNITS
	VO (V)	VIN (V)	VDD (V)	-55	-40	+85	+125	+25			
								Min	Typ	Max	
Quiescent Device Current IDD Max	-	0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current IOL Min	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current IOH Min	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, VOL Max	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, VOH Min	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, VIL Max	0.5,4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, VIH Min	0.5,4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current IIN Max	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

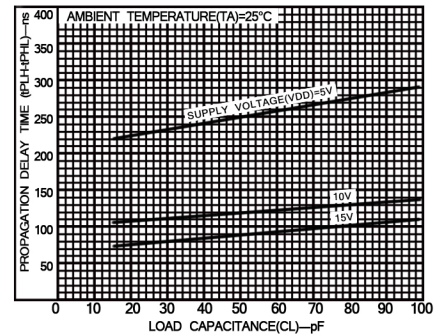


Fig.12 -Typical propagation delay time as a function of load capacitance.

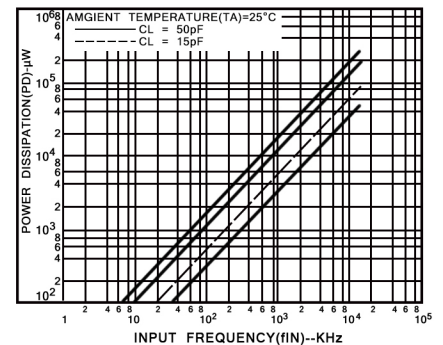


Fig.13 -Dynamic power dissipation

DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C
 Input tr = 20 ns, CL = 50 pF, RL = 200kΩ

CHARACTERISTIC	VDD (V)	LIMITS			UNITS
		Min	Typ	Max	
Propagation Delay Time tPHL, tPLH: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5 10 15	-	250 120 90	500 240 180	ns
\overline{PE} to Q	5 10 15	-	200 100 70	400 200 140	ns
CLOCK UP to \overline{CARRY} , CLOCK DOWN to \overline{BORROW}	5 10 15	-	160 80 60	320 160 120	ns
\overline{RESET} or PE to \overline{BORROW} or \overline{CARRY}	5 10 15	-	300 150 110	600 300 220	ns
Transition Time, tTHL, tTLH	5 10 15	-	100 50 40	200 100 80	ns
Min. Removal Time, trem* RESET or \overline{PE}	5 10 15	-	40 20 15	80 40 30	ns
Min. Pulse Width, tW RESET	5 10 15	-	240 150 130	480 300 260	ns
\overline{PE}	5 10 15	-	120 85 70	240 170 140	ns
CLOCK	5 10 15	-	90 45 30	180 90 60	ns
Max. Clock Input Frequency, fCL	5 10 15	2 4 5.5	4 8 11	-	MHz
Clock Rise & Fall Time, tr, tf	5 10 15	-	-	15 15 5	μs
Input Capacitance, CIN: RESET	-	-	10	15	pF
All Other Inputs	-	-	5	7.5	pF

*The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram, Fig. 10).

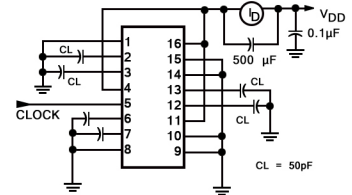


Fig.14 -Dynamic power dissipation test circuit.

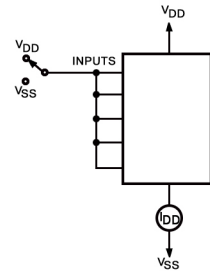


Fig.15 -Quiescent- device-current test circuit.

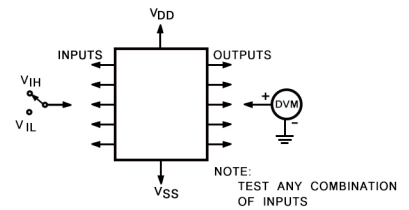


Fig.16 -Input-voltage test circuit.

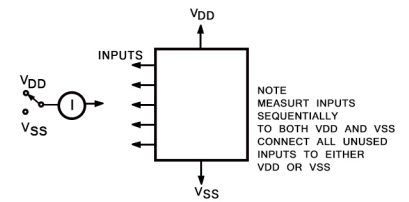


Fig.17 -Input current test circuit.

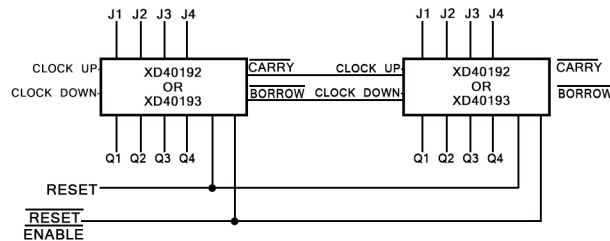
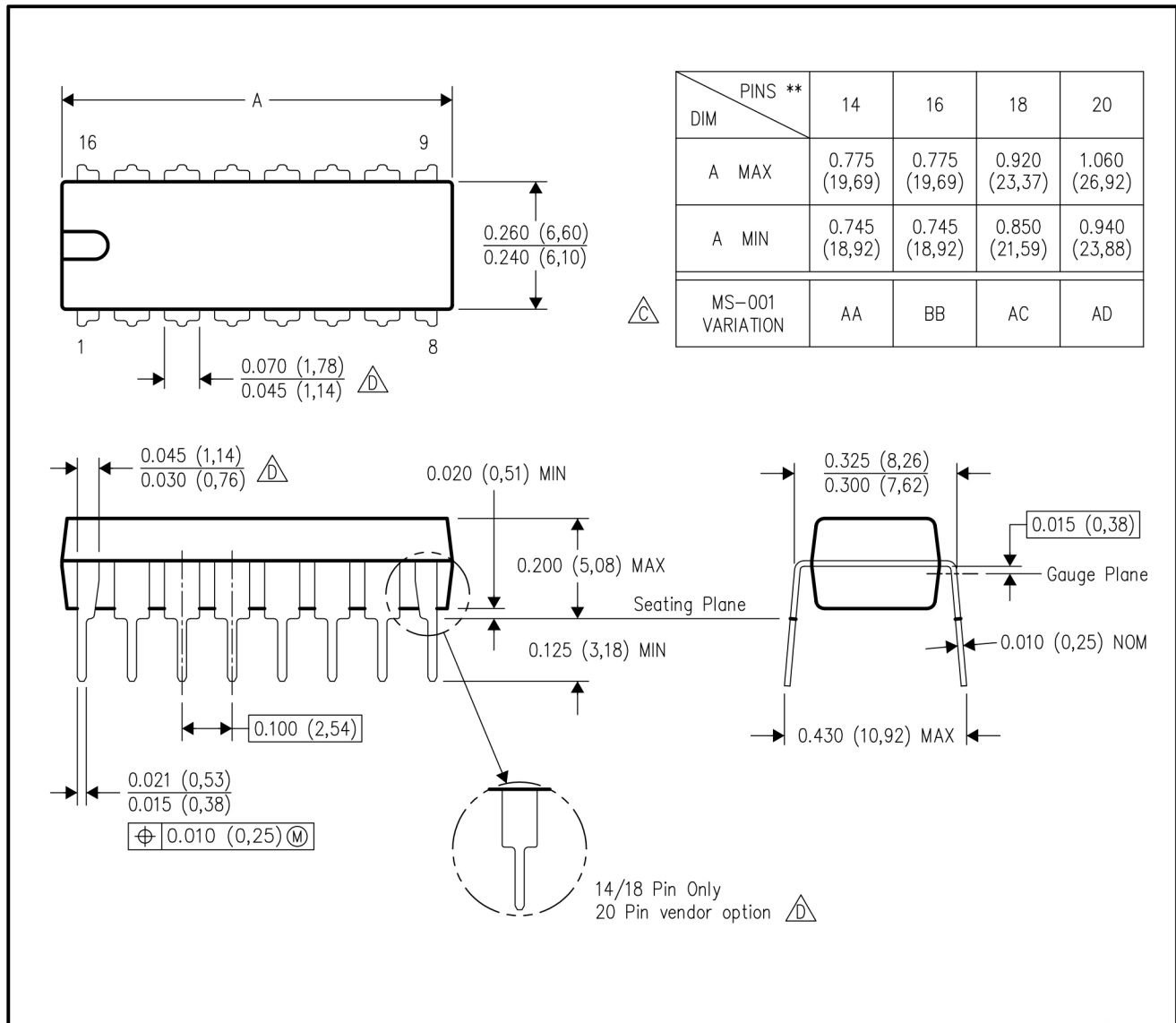


Fig.18 -Cascaded counter packages.

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

以上信息仅供参考. 如需帮助联系客服人员. 谢谢 XINLUDA