

N-Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The MEE3710-G is a N-Channel enhancement mode power field effect transistor, using Force-MOS patented Extended Trench Gate (ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leq 23m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

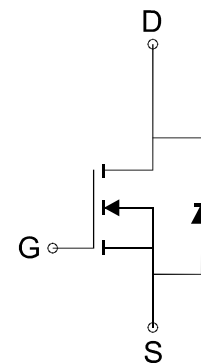
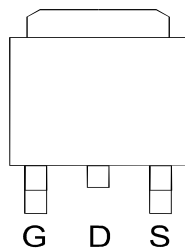
APPLICATIONS

- Power Management
- Synchronous Rectification
- Load Switch

PIN CONFIGURATION

(TO-252-3L)

Top View



N-Channel MOSFET

Ordering Information: MEE3710-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current*	I_D	$T_C=25^\circ C$	37
		$T_C=70^\circ C$	30
Single pulse Avalanche Energy L=0.5mH	I_{AS}	16	A
Single pulse Avalanche Energy L=0.5mH	E_{AS}	64	mJ
Pulsed Drain Current	I_{DM}	151	A
Maximum Power Dissipation*	P_D	$T_C=25^\circ C$	69
		$T_C=70^\circ C$	44
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case*	$R_{\theta Jc}$	1.8	$^\circ C/W$

*The device mounted on 1in² FR4 board with 2 oz copper

*100% UIS Tested base on TESEC machine



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Electrical Characteristics ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	100			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	2		4	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance ^a	$V_{GS}=10V, I_D=28A$		19	23	$m\Omega$
V_{SD}	Diode Forward Voltage	$I_S=28A, V_{GS}=0V,$			1.2	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=80V, V_{GS}=10V, I_D=28A$		25		nC
Q_{gs}	Gate-Source Charge			10		
Q_{gd}	Gate-Drain Charge			6		
C_{iss}	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$		1728		pF
C_{oss}	Output Capacitance			530		
C_{rss}	Reverse Transfer Capacitance			32		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=50V, R_L=1.8\Omega$ $V_{GS}=10V, R_G=2.5\Omega$ $I_D=28A$		22		ns
t_r	Turn-On Rise Time			60		
$t_{d(off)}$	Turn-Off Delay Time			25		
t_f	Turn-Off Fall Time			16		
T_{rr}	Reverse Recovery Time	$I_F=28A, V_{GS}=0V, di/dt=100A/us$		40		ns
Q_{rr}	Reverse Recovery Charge			60		nC

 Notes: a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

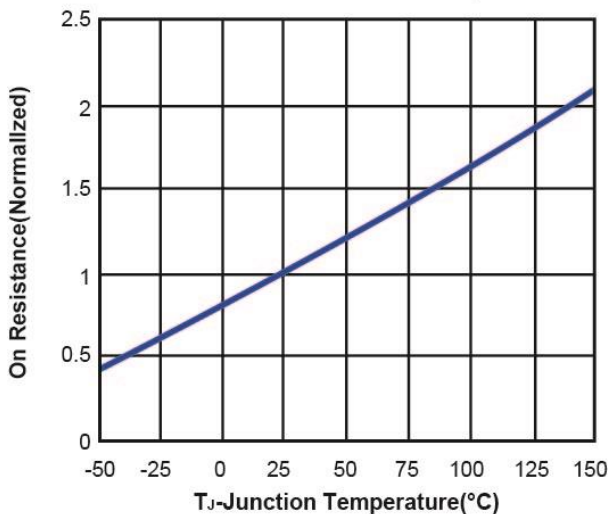
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



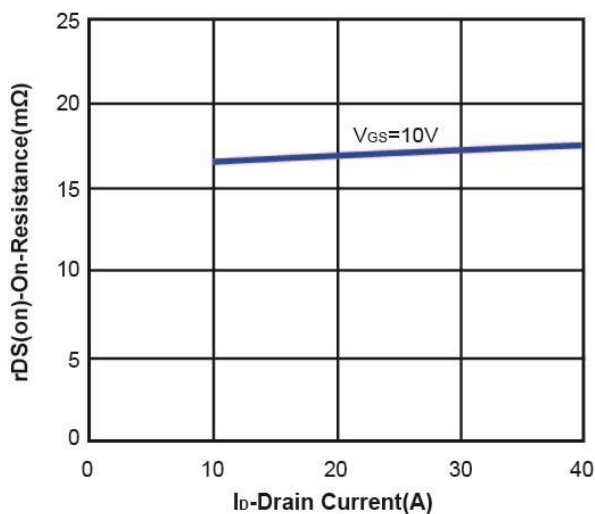
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Typical Characteristics (T_J =25°C Noted)

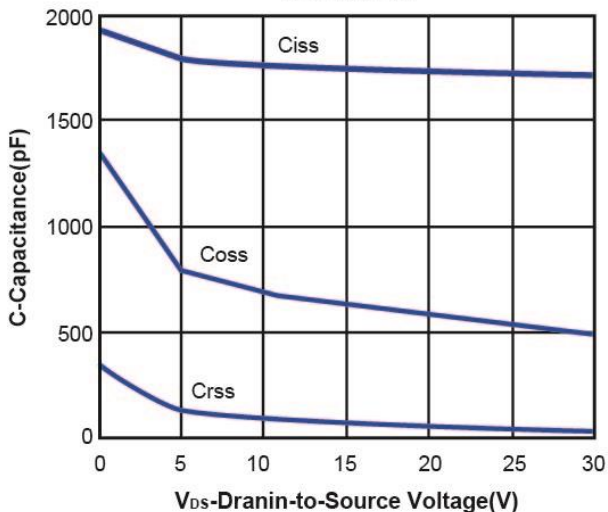
On Resistance vs. Junction Temperature



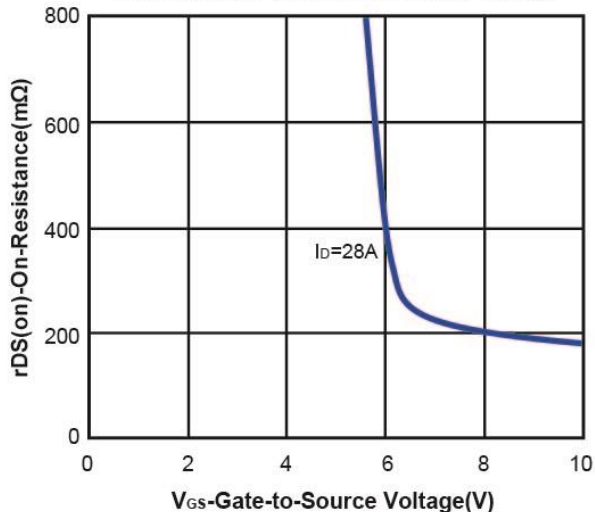
On Resistance vs. Drain Current



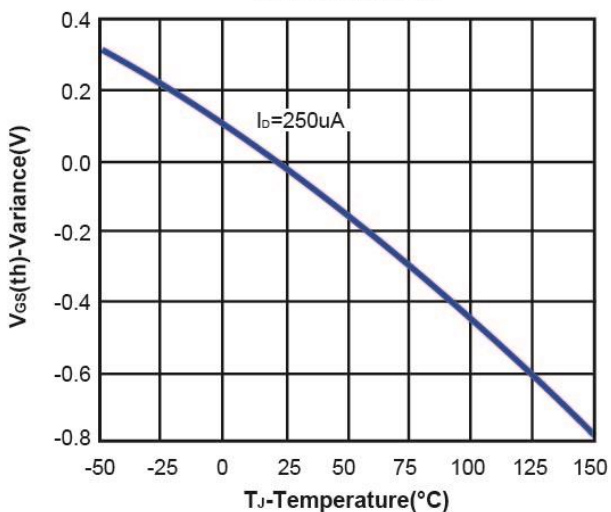
Capacitance



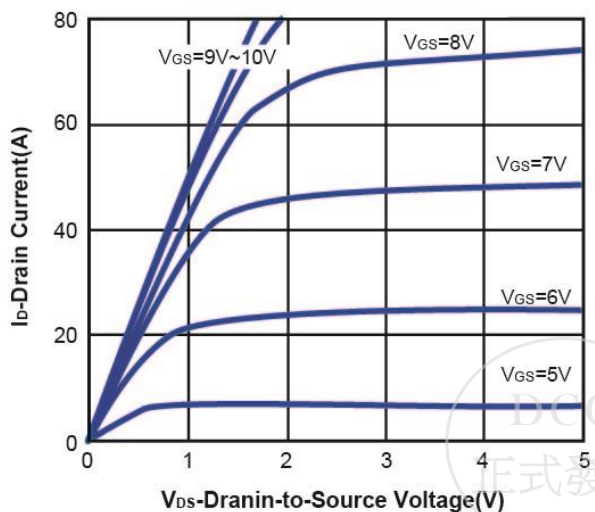
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

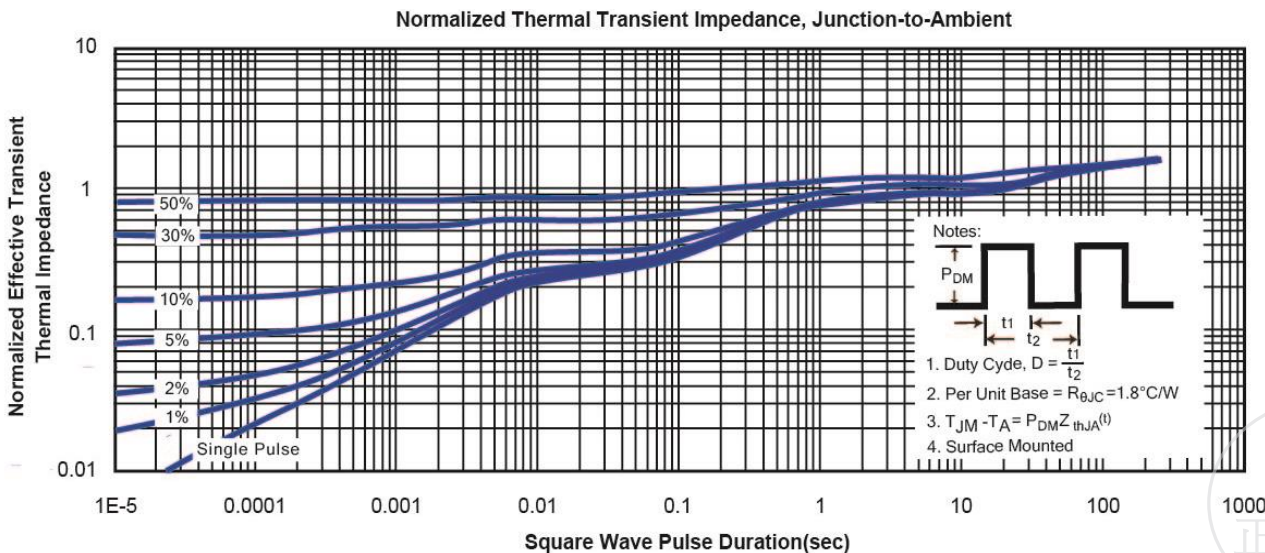
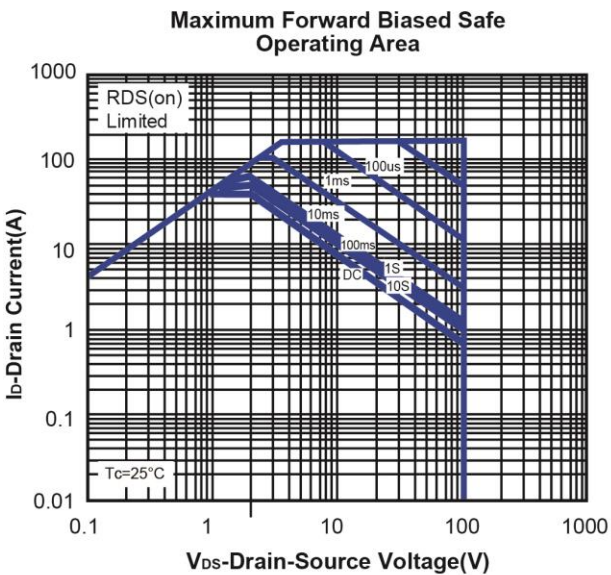
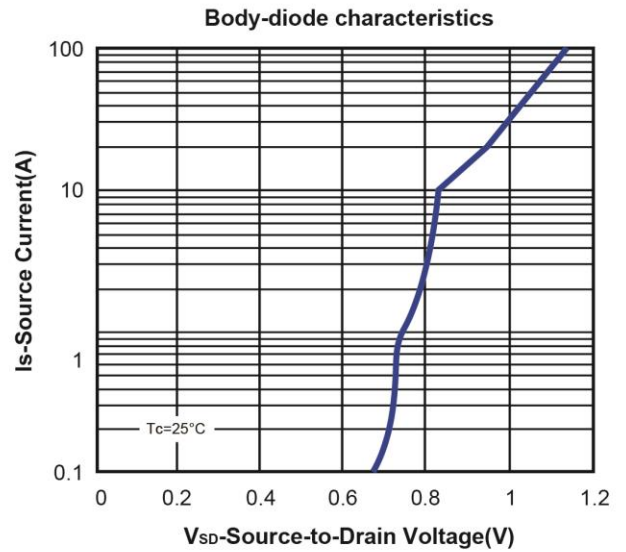
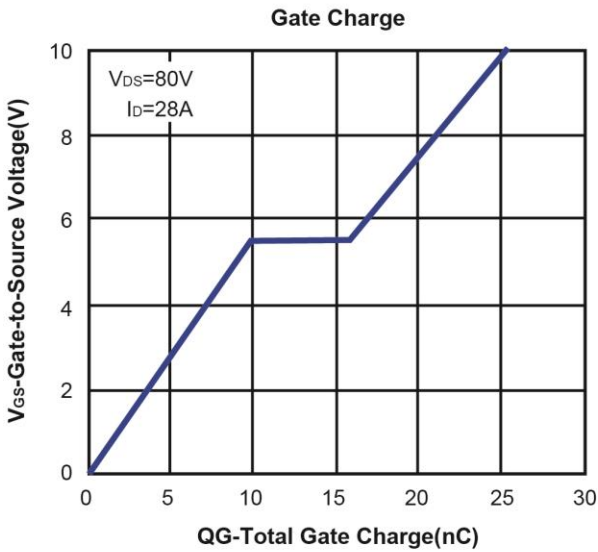


On-Region Characteristics

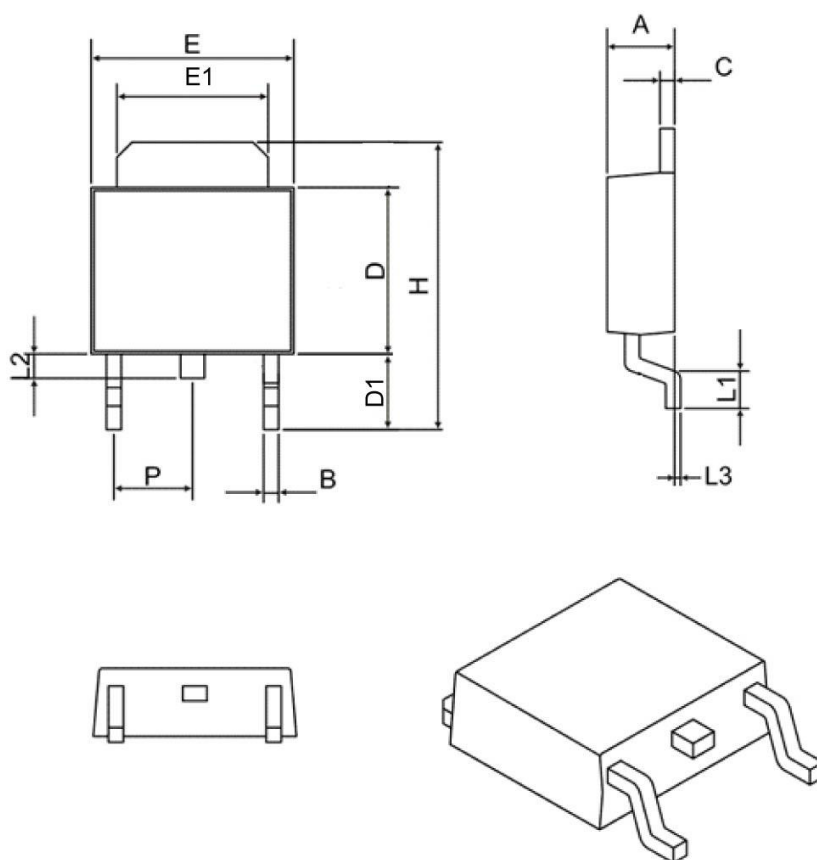


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Typical Characteristics (T_J =25°C Noted)



TO-252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

