ME55N06A/ ME55N06A-G

N-Channel 75-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME55N06A is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 9.5m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

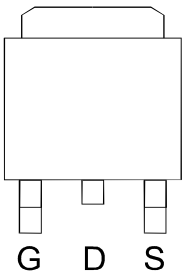
APPLICATIONS

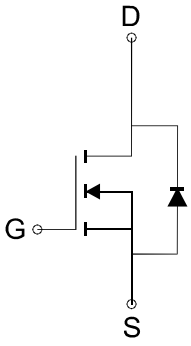
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME55N06A (Pb-free)

ME55N06A-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	75	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25℃	I_D	64	A
	T_C=70℃		51	
Pulsed Drain Current		I_{DM}	256	A
Maximum Power Dissipation	T_C=25℃	P_D	63	W
	T_C=70℃		40	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel 75-V (D-S) MOSFET

Electrical Characteristics (T_J =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	75			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2		4	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=75V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=25A		7.5	9.5	mΩ
V_{SD}	Diode Forward Voltage	I_S=25A, V_{GS}=0V		0.85	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=44V, V_{GS}=10V, I_D=25A		114		nC
Qg	Total Gate Charge	V_{DS}=44V, V_{GS}=4.5V, I_D=25A		26		
Qgs	Gate-Source Charge			34		
Qgd	Gate-Drain Charge			33		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		1563		pF
Coss	Output Capacitance			363		
Crss	Reverse Transfer Capacitance			194		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=28V, R_L=28Ω, V_{GS} =10V, R_G=4.5Ω		51.4		ns
t_r	Turn-On Rise Time			19.3		
$t_{d(off)}$	Turn-Off Delay Time			104		
t_f	Turn-Off Fall Time			19.9		

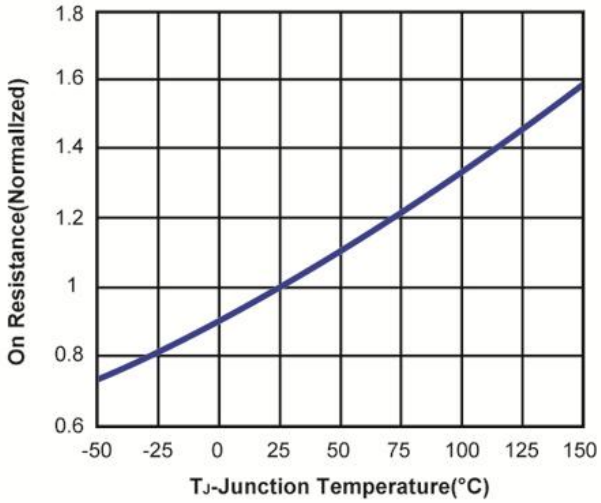
Note: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

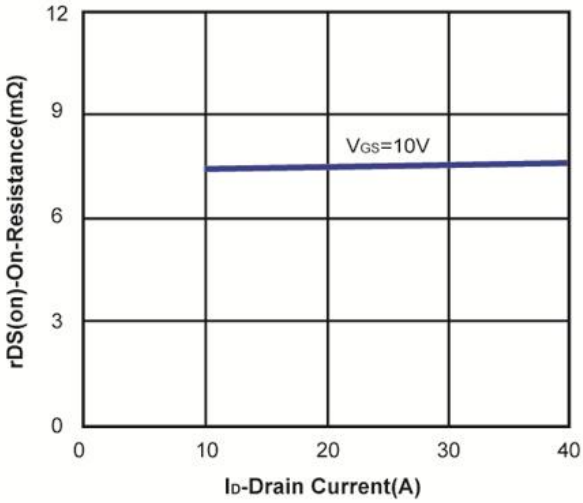
N-Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

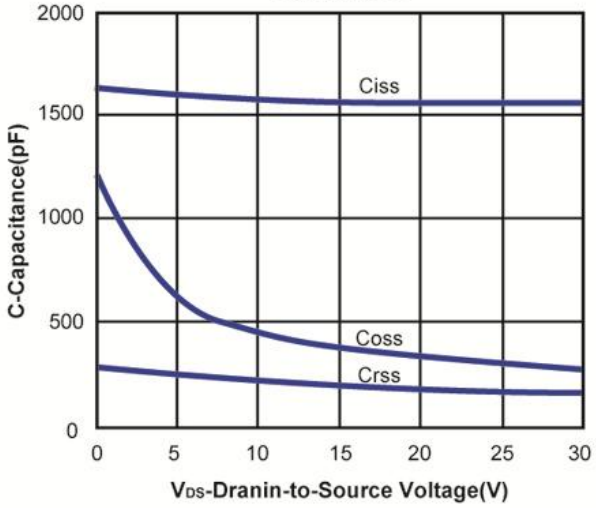
On Resistance vs. Junction Temperature



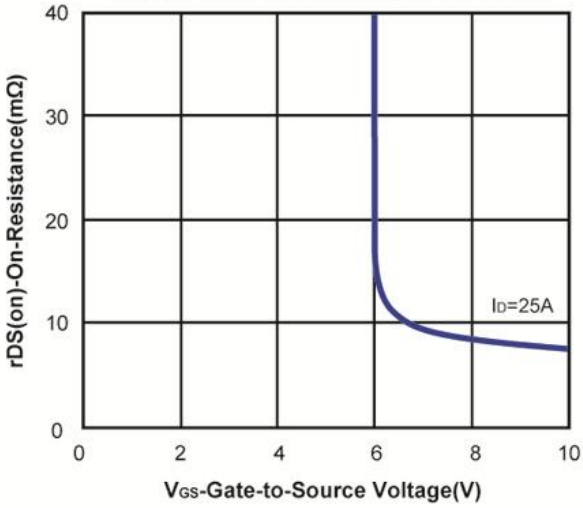
On Resistance vs. Drain Current



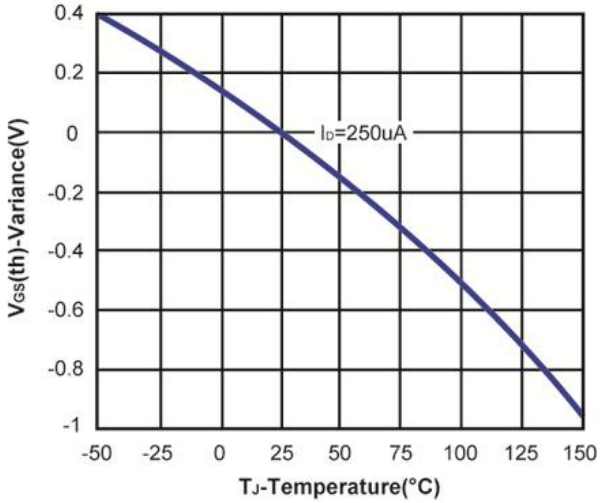
Capacitance



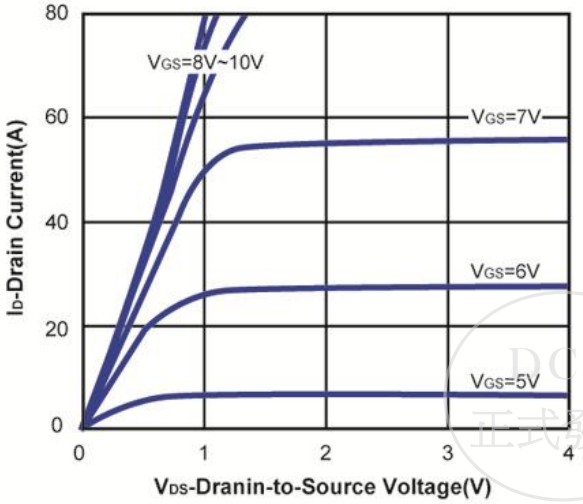
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



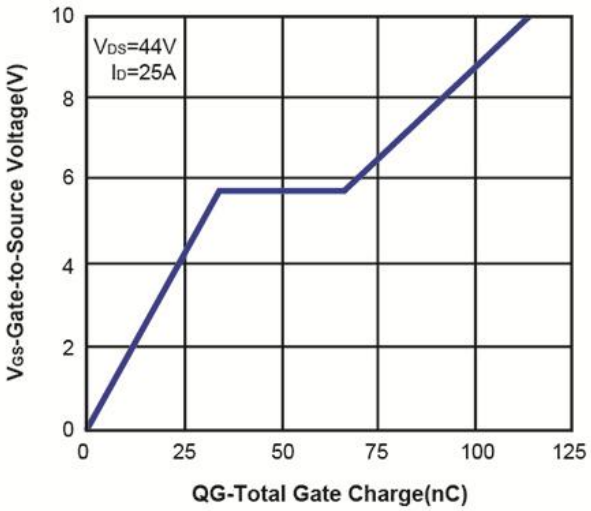
On-Region Characteristics



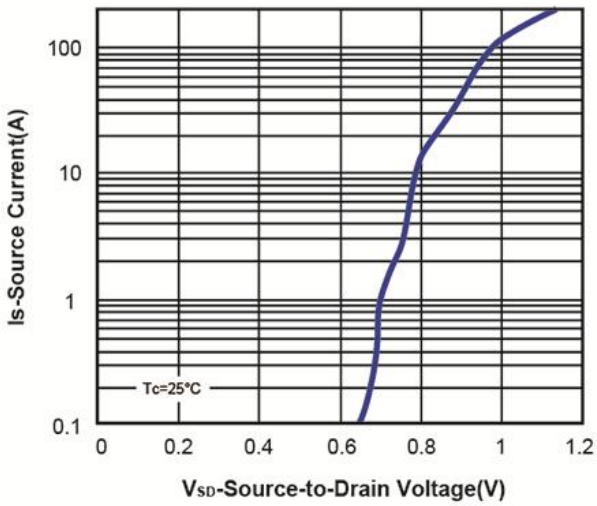
N-Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

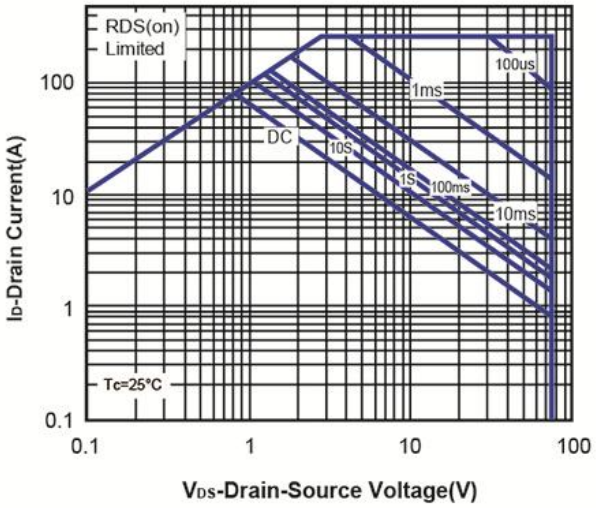
Gate Charge



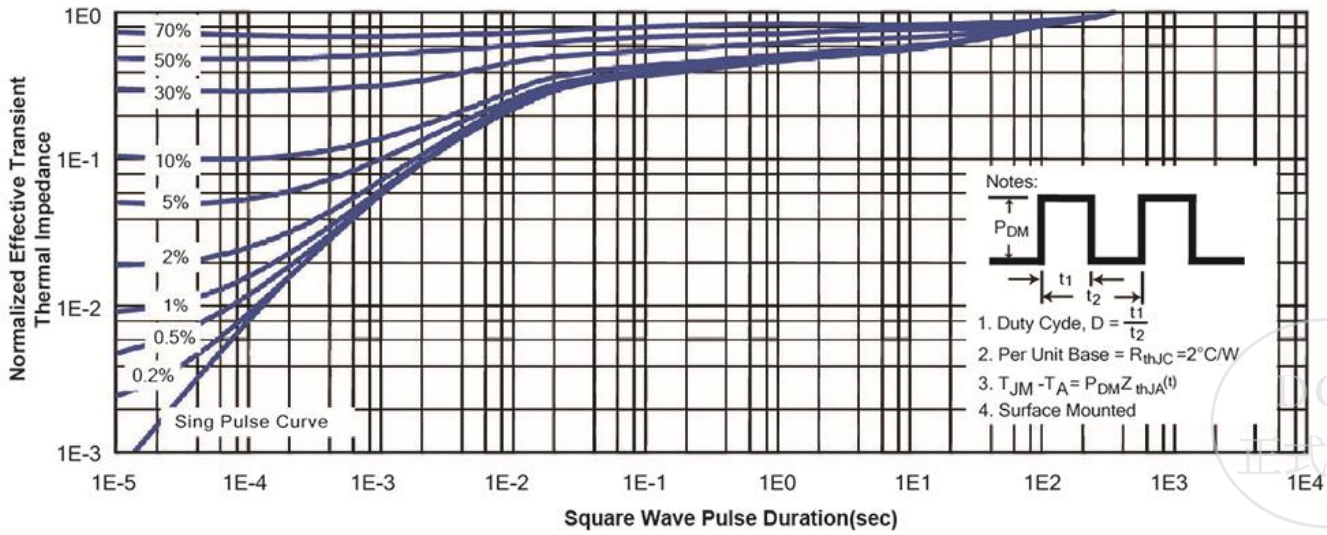
Body-diode characteristics



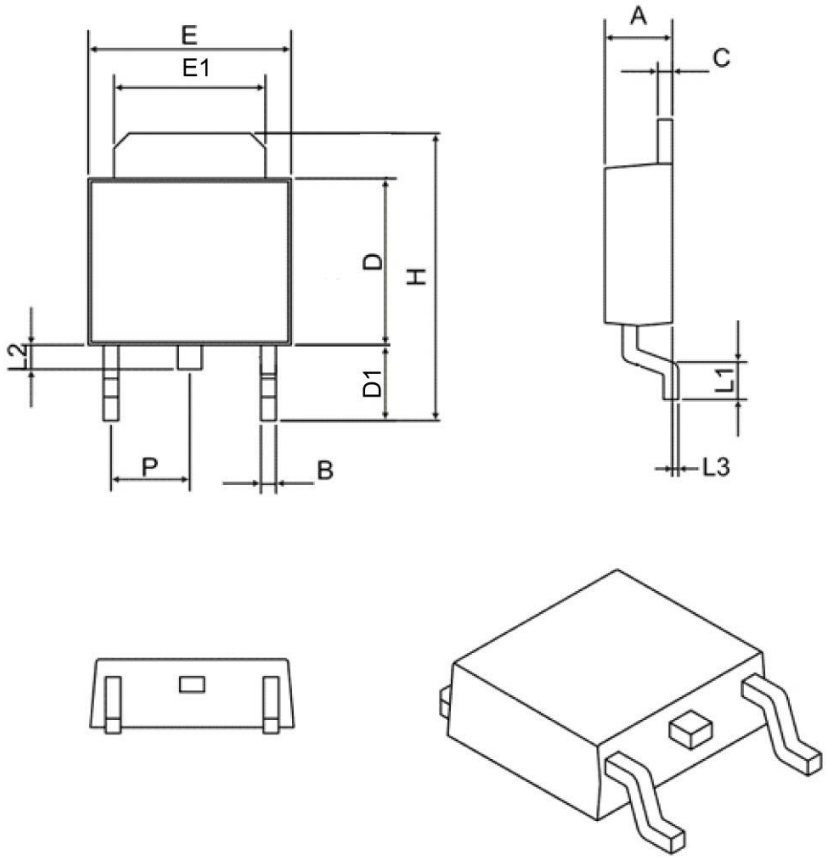
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	