

N-Channel 150-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME10N15 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

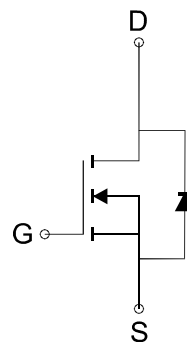
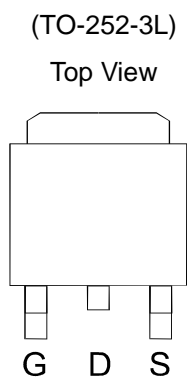
FEATURES

- $R_{DS(ON)} \leq 345m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 365m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME10N15 (Pb-free)

ME10N15-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	Tc=25°C	7.6
		Tc=70°C	6.1
Pulsed Drain Current	I_{DM}	30	A
Maximum Power Dissipation	P_D	Tc=25°C	32.1
		Tc=70°C	20.5
Operating Junction and Storage Temperature Range	TJ, Tstg	-55 to 150	°C
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	3.9	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_c =25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	150			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =120V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 7A		285	345	mΩ
		V _{GS} =4.5V, I _D = 6A		290	365	
V _{SD}	Diode Forward Voltage	I _S =1.8A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =75V, V _{GS} =10V, I _D =10A		17.5		nC
Q _{gs}	Gate-Source Charge			4.5		
Q _{gd}	Gate-Drain Charge			4.7		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		538		pF
C _{oss}	Output Capacitance			55		
C _{rss}	Reverse Transfer Capacitance			21		
t _{d(on)}	Turn-On Delay Time	V _{DS} =75V, R _L =10.68Ω, V _{GEN} =10V, R _G =6Ω		11.6		ns
t _r	Turn-On Rise Time			9.3		
t _{d(off)}	Turn-Off Delay Time			29.3		
t _f	Turn-Off Fall Time			3.7		

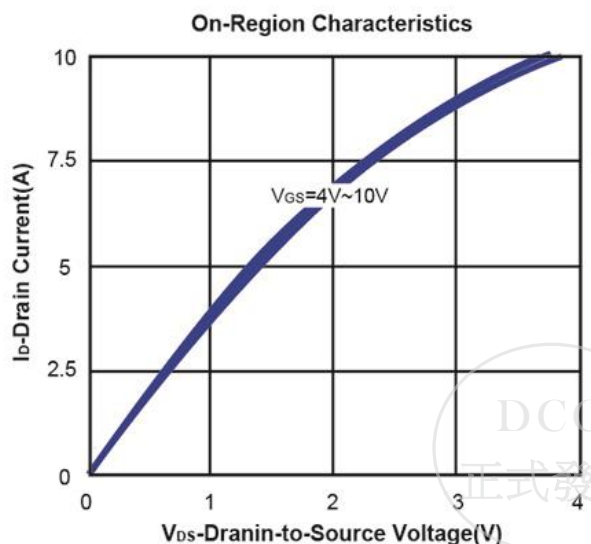
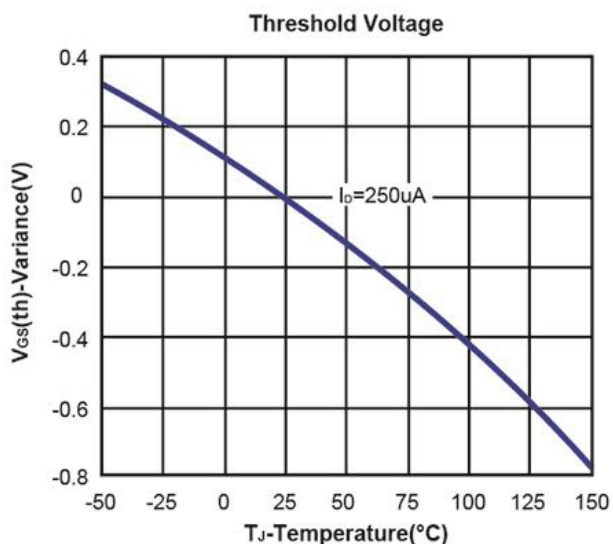
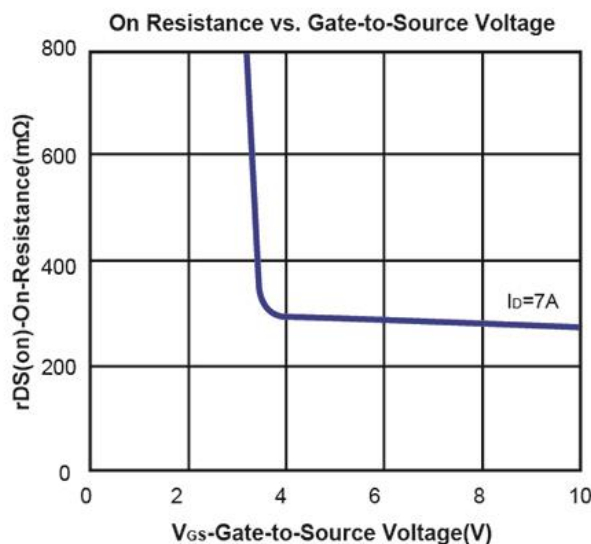
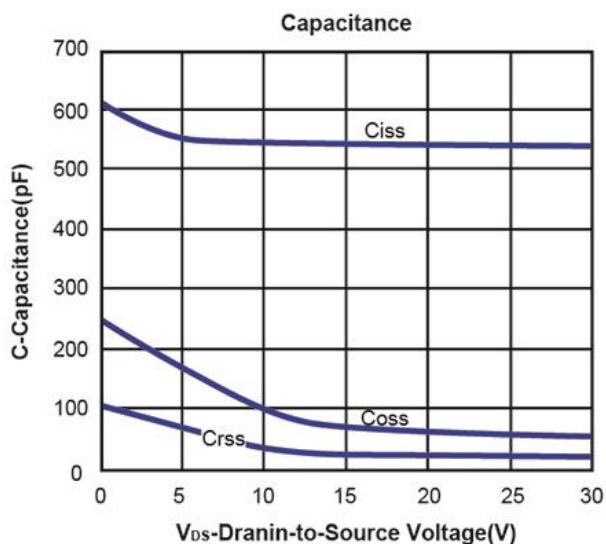
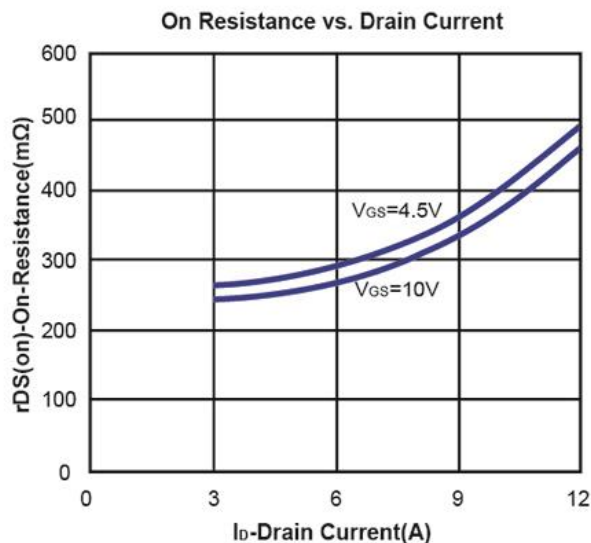
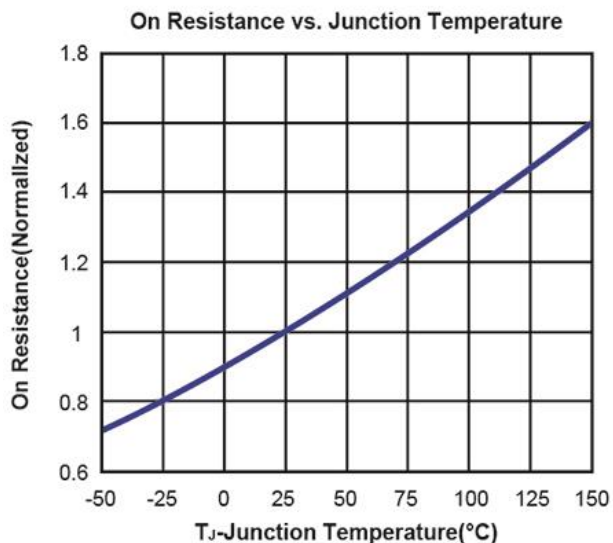
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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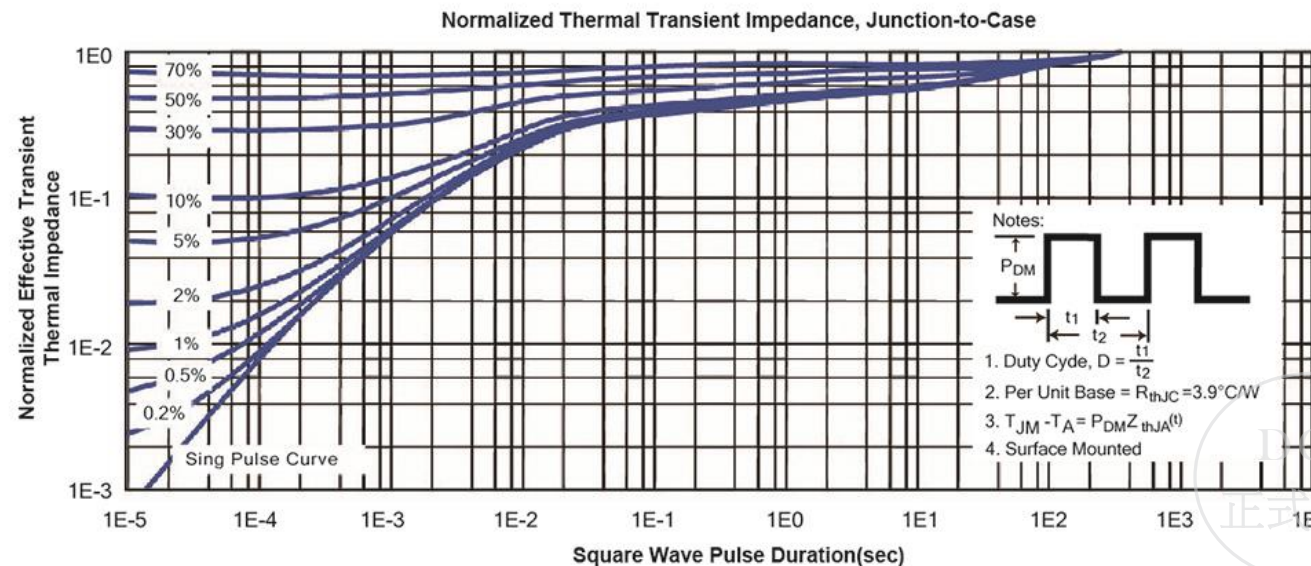
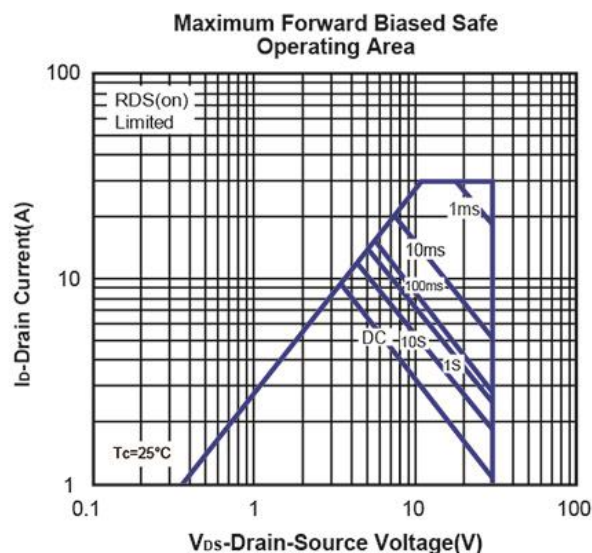
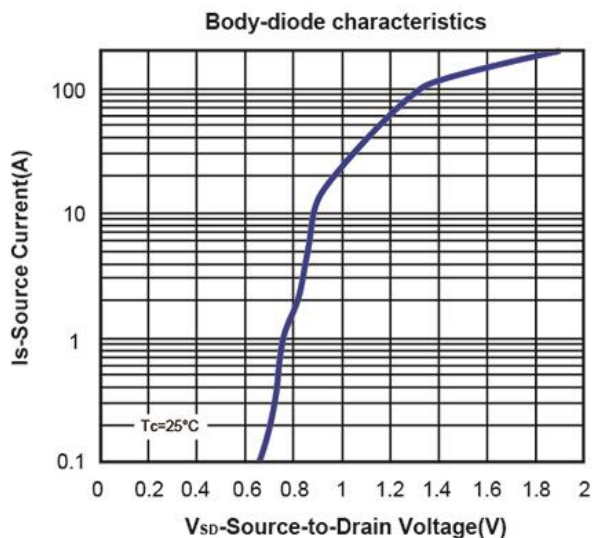
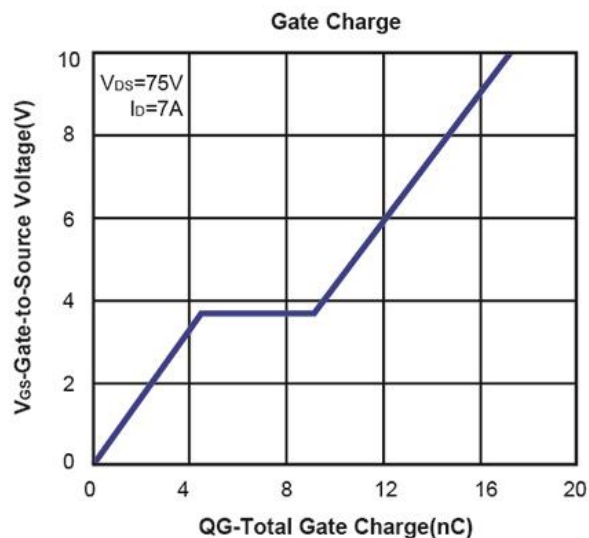
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Typical Characteristics (T_J =25°C Noted)

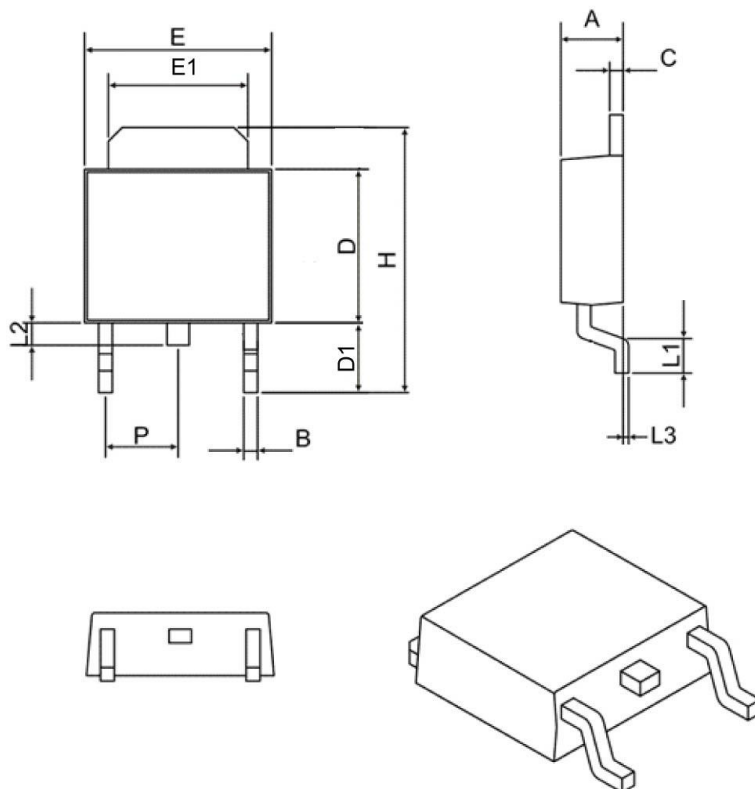


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TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

