ME4565A/ ME4565A-G

N- and P-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4565A is the N and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦26.5mΩ@V_{GS}=10V (N-Ch)
- $R_{DS(ON)}$ ≦45mΩ@V_{GS}=4.5V (N-Ch)
- $R_{DS(ON)}$ ≦44mΩ@V_{GS}=-10V (P-Ch)
- $R_{DS(ON)}$ ≦60mΩ@V_{GS}=-4.5V(P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

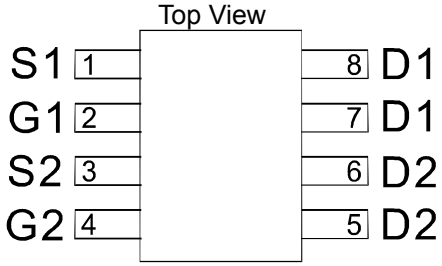
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

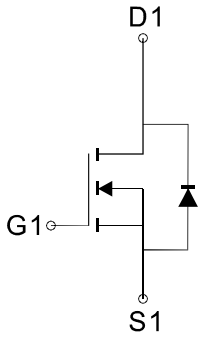
(SOP-8)

Top View

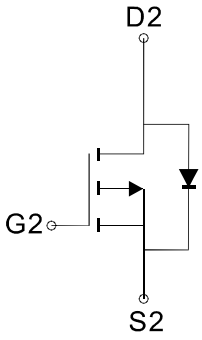


Ordering Information: ME4565A (Pb-free)

ME4565A-G (Green product-Halogen free)



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current(Tj=150℃)*	T_A=25℃	I_D	6.9	-5.3	A
	T_A=70℃		5.5	-4.3	
Pulsed Drain Current		I_{DM}	27	-21	A
Maximum Power Dissipation	T_A=25℃	P_D	2	2	W
	T_A=70℃		1.3	1.3	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5	62.5	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=5.2A		22	26.5	mΩ
		V_{GS}=4.5V, I_D=4.9A		35	45	
V_{SD}	Diode Forward Voltage	I_S=6A, V_{GS}=0V		0.86	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_D=6A		15		nC
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_D=6A		7		
Qgs	Gate-Source Charge			4.1		
Qgd	Gate-Drain Charge			3.4		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, F=1MHz		565		pF
Coss	Output Capacitance			76		
Crss	Reverse Transfer Capacitance			24		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω, I_D=1A, V_{GEN}=10V, R_G=6Ω		13		ns
t_r	Turn-On Rise Time			14		
$t_{d(off)}$	Turn-Off Delay Time			36		
t_f	Turn-On Fall Time			4		

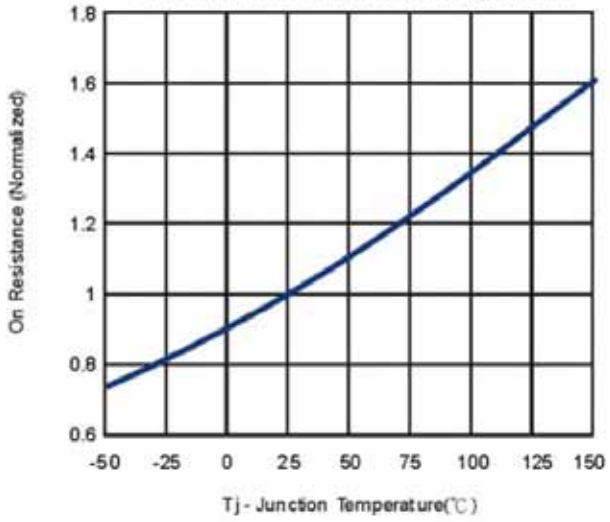
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

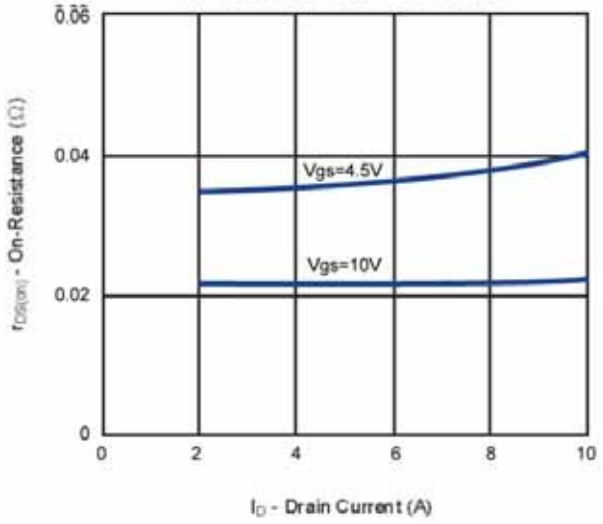
N Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

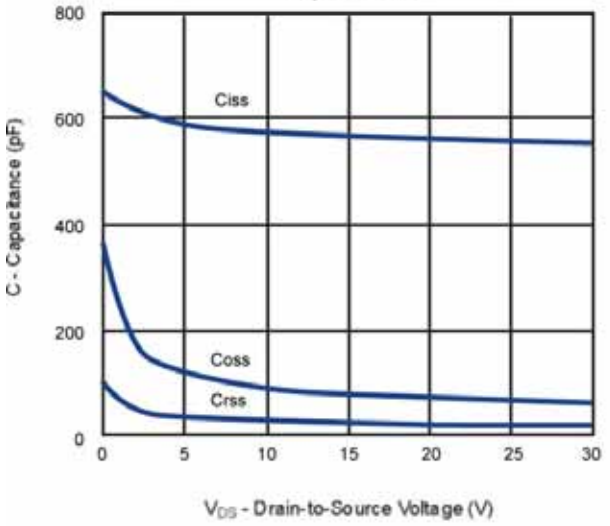
On Resistance vs. Junction Temperature



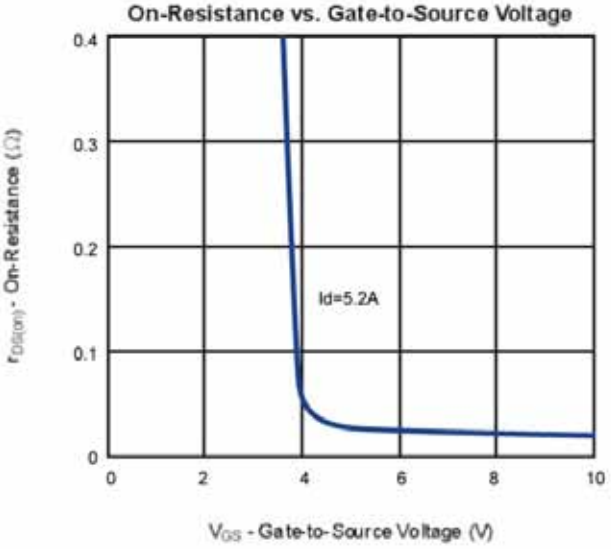
On-Resistance vs. Drain Current



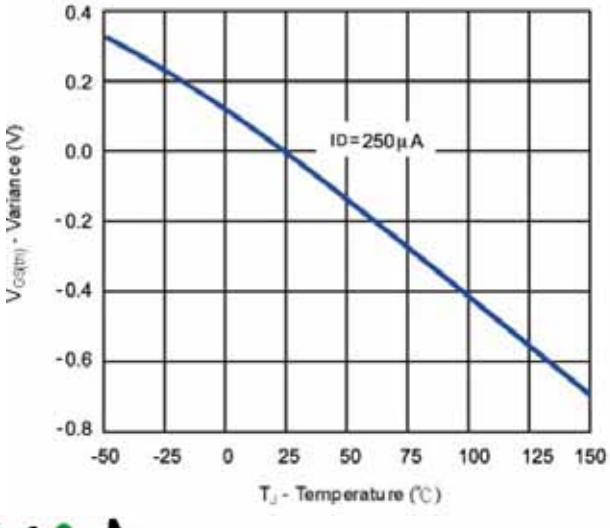
Capacitance



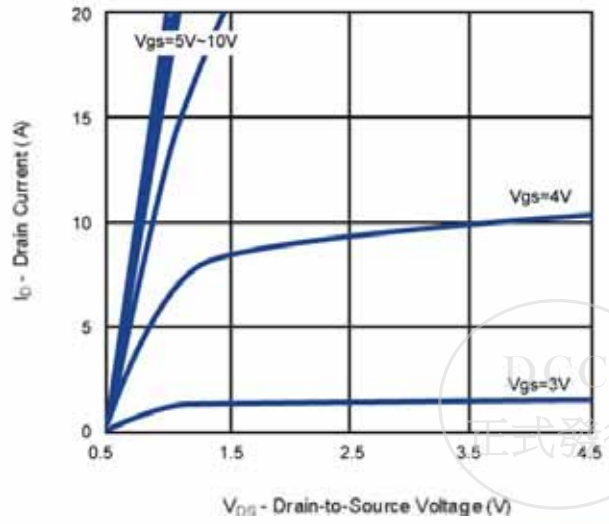
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



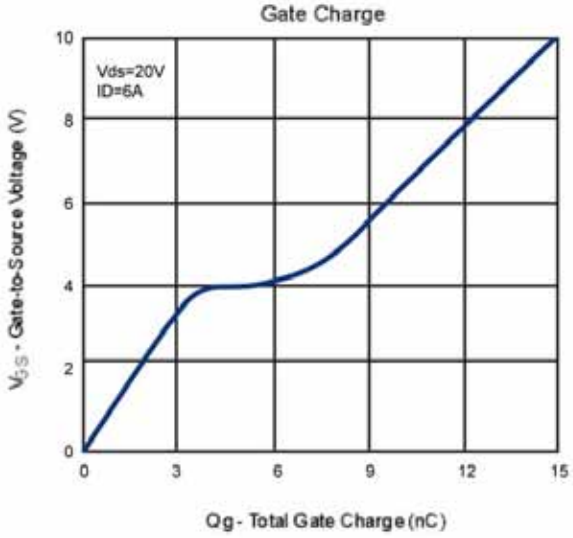
On-Region Characteristics



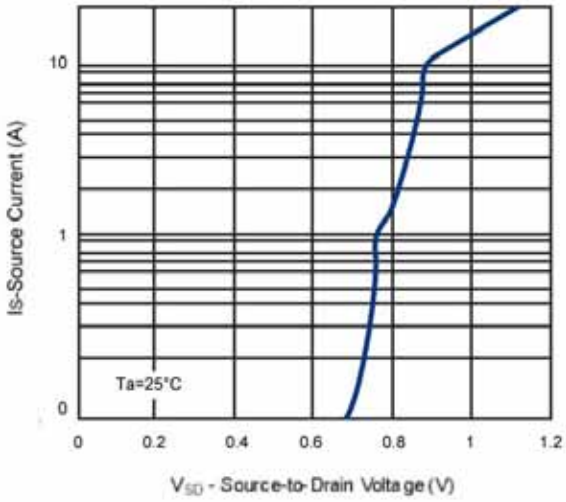
N Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

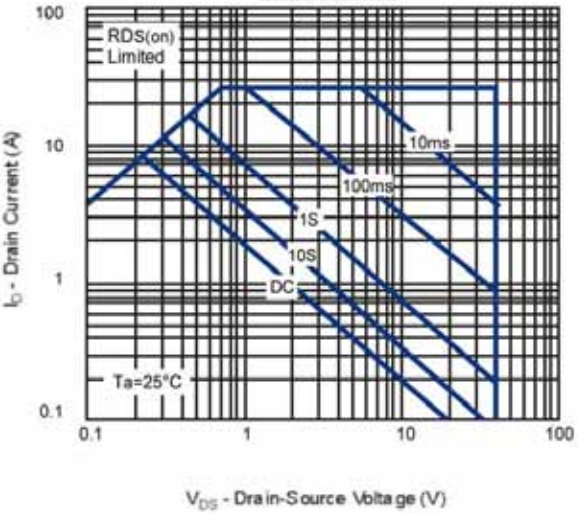
Gate Charge



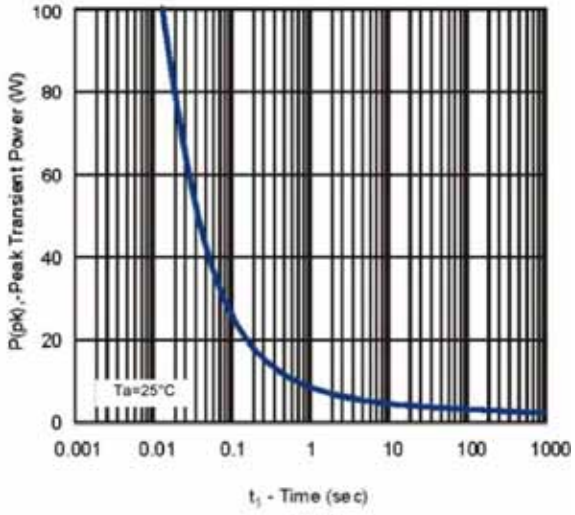
Body-diode characteristics



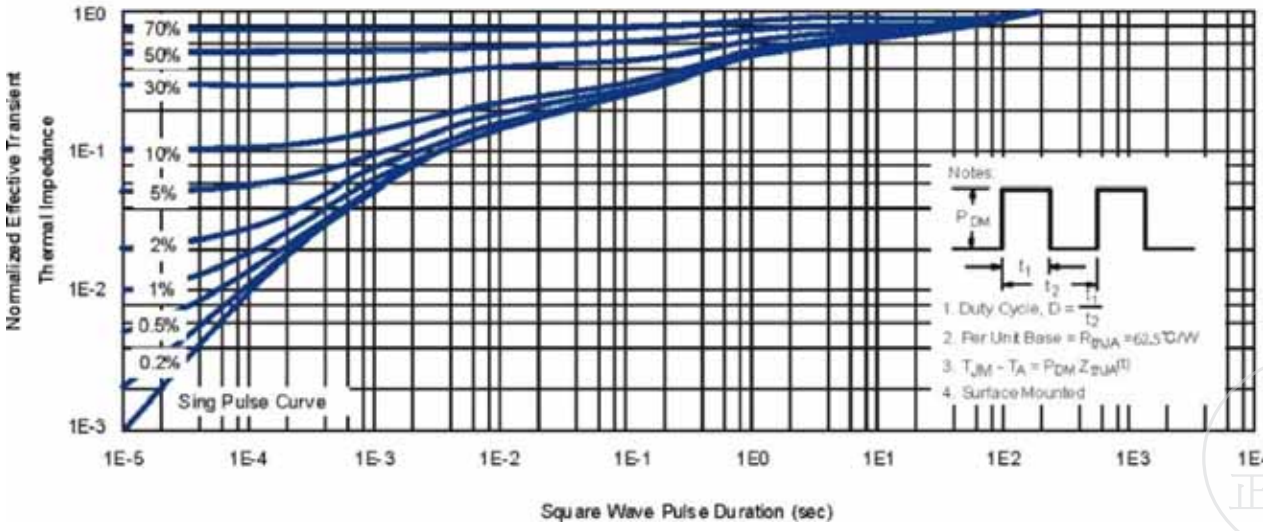
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



P Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-40V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -5A		36	44	mΩ
		V_{GS}=-4.5V, I_D= -2A		47	60	
V_{SD}	Diode Forward Voltage	I_S=-5 A, V_{GS}=0V		-0.86	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-20V, V_{GS}=-10V, I_D=-5A		20		nC
Qg	Total Gate Charge	V_{DS}=-20V, V_{GS}=-4.5V, I_D=-5A		10		
Qgs	Gate-Source Charge			4.1		
Qgd	Gate-Drain Charge			4.9		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, F=1MHz		859		pF
Coss	Output Capacitance			126		
Crss	Reverse Transfer Capacitance			41		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω		39		ns
t_r	Turn-On Rise Time			19		
$t_{d(off)}$	Turn-Off Delay Time			59		
t_f	Turn-On Fall Time			9		

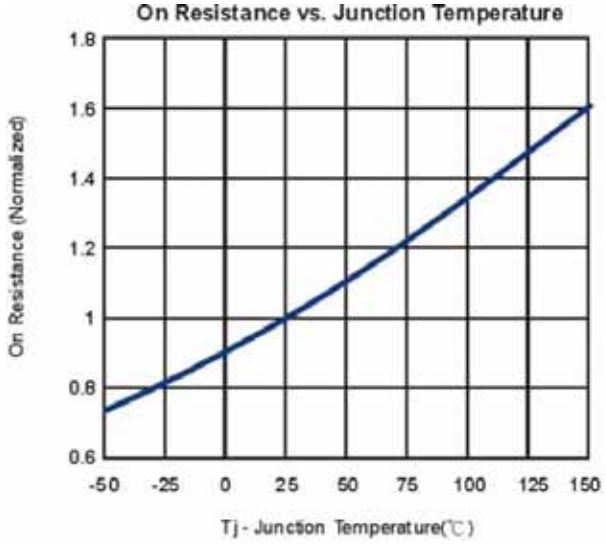
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

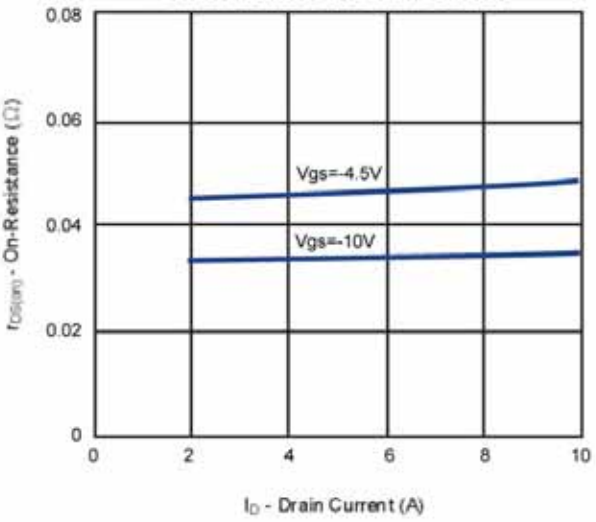
P Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

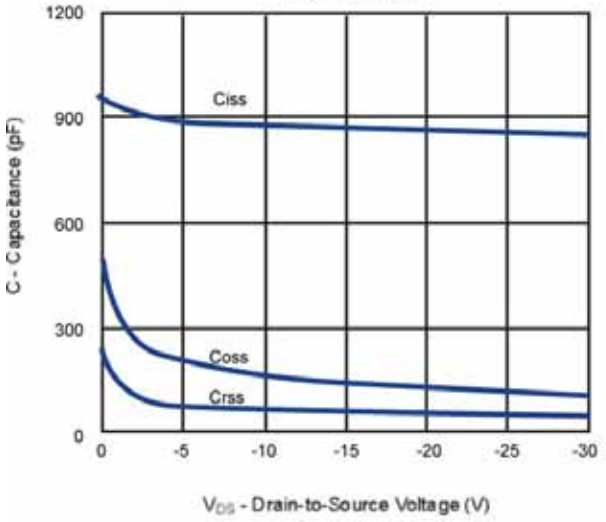
On Resistance vs. Junction Temperature



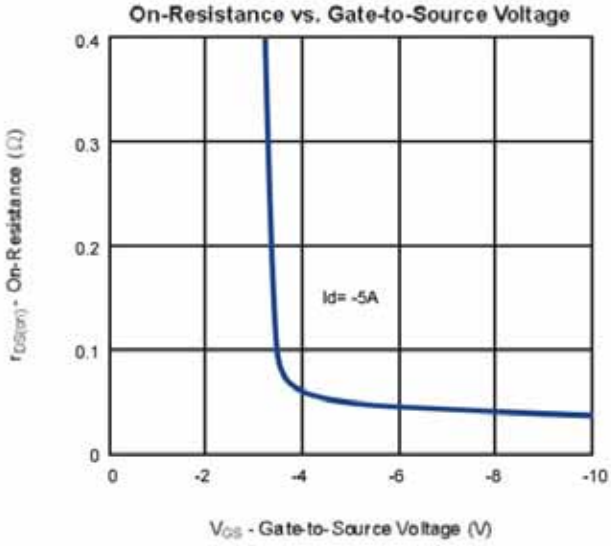
On-Resistance vs. Drain Current



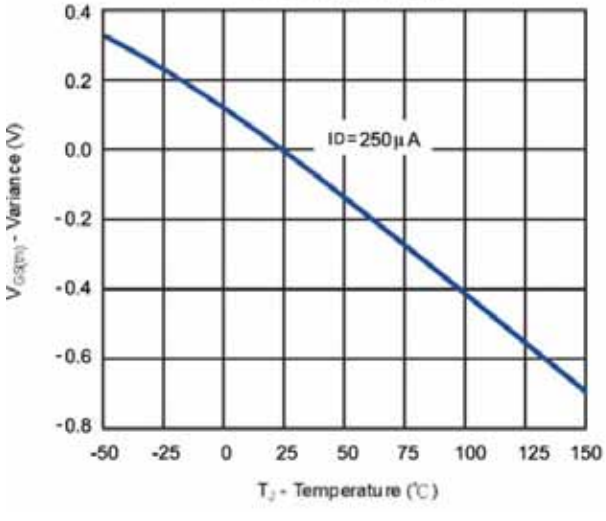
Capacitance



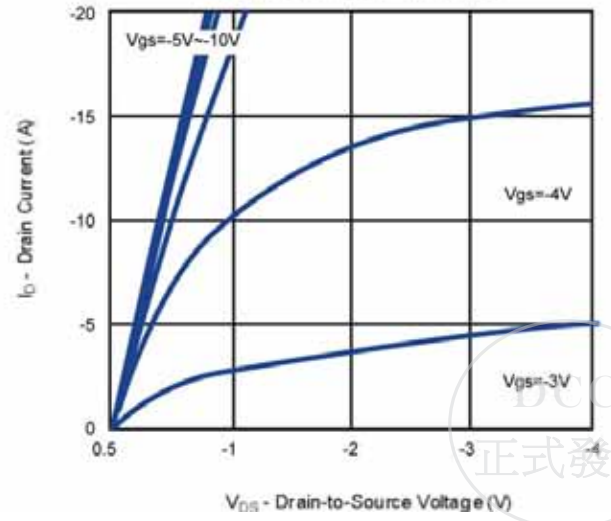
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



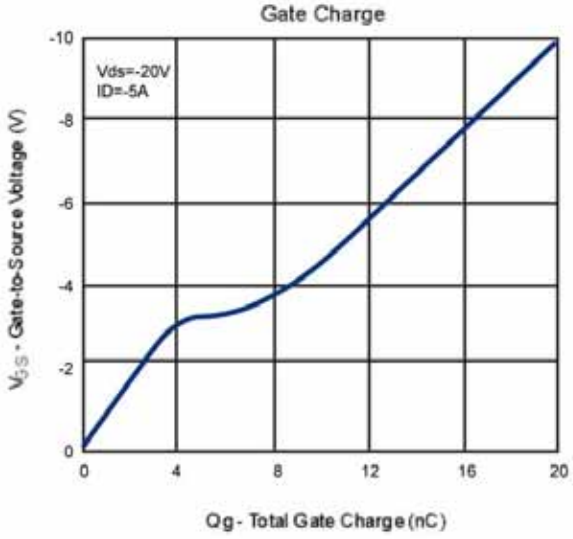
On-Region Characteristics



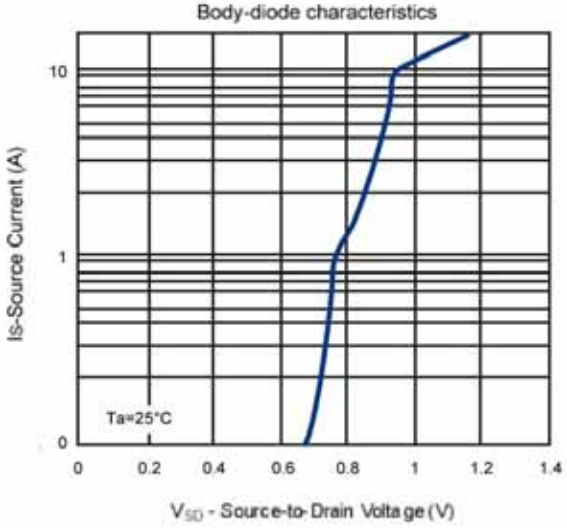
P Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

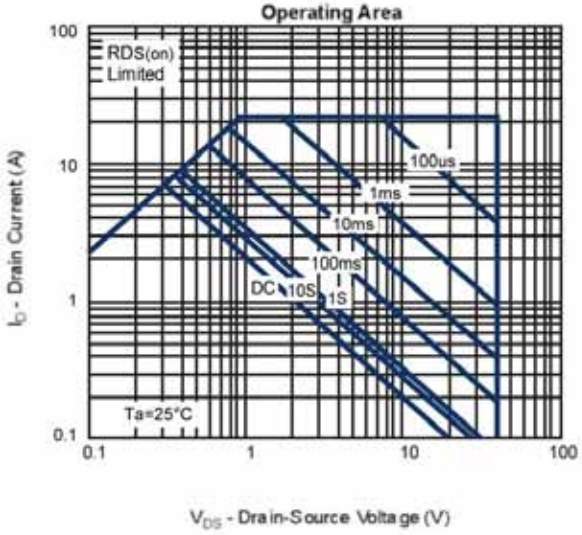
Gate Charge



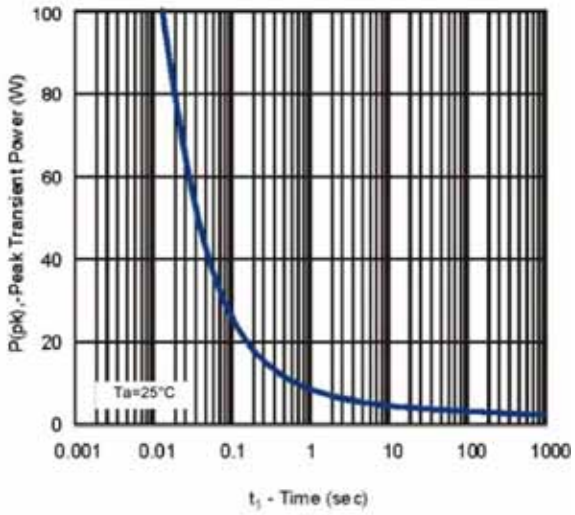
Body-diode characteristics



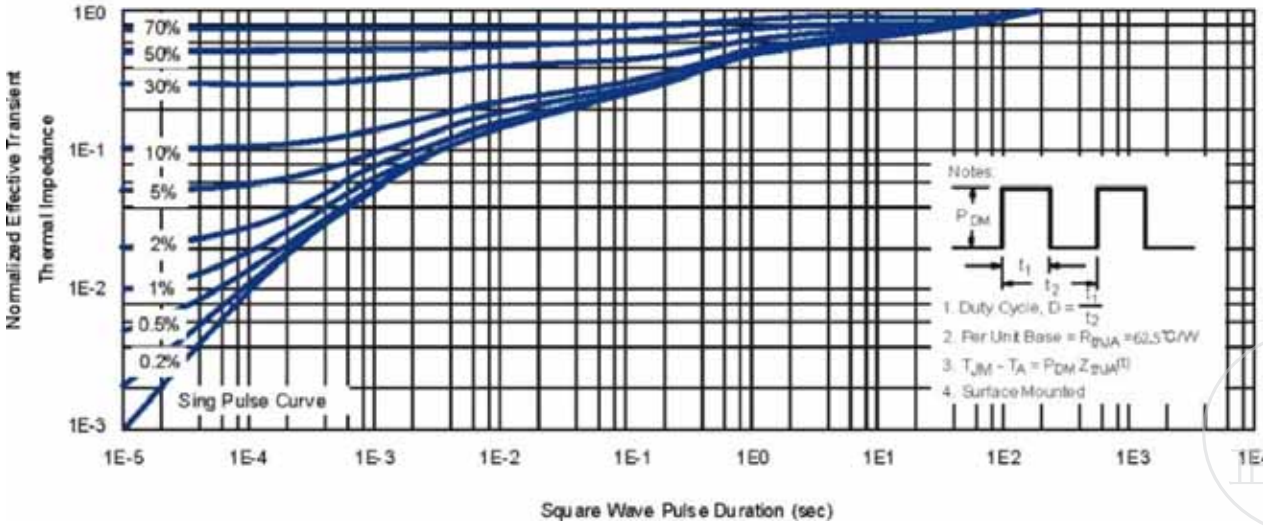
Maximum Forward Biased Safe Operating Area



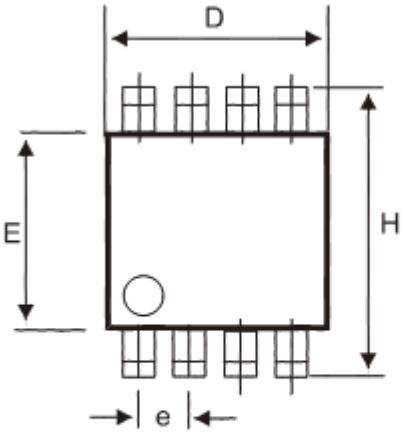
Single Pulse Maximum Power Dissipation

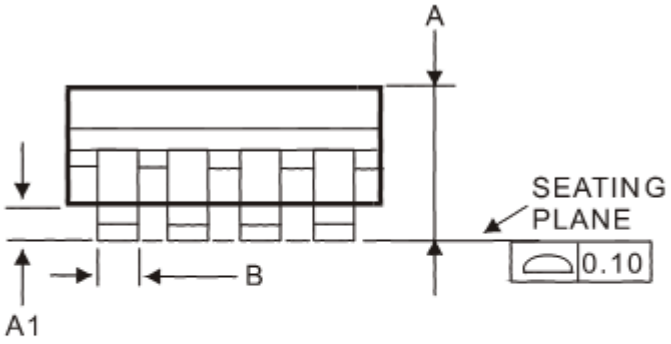


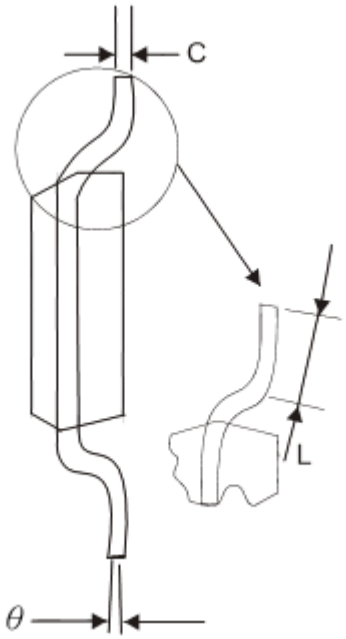
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°