

N- Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The ME35N10 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

FEATURES

- $R_{DS(ON)} \leq 22m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 26m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

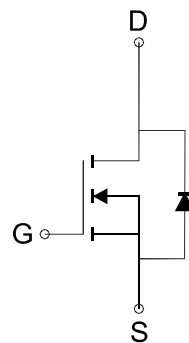
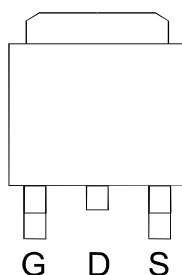
APPLICATIONS

- DC/DC Converter
- Load Switch
- LCD/ LED Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View



N-Channel MOSFET

Ordering Information: ME35N10 (Pb-free)

ME35N10-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

| Parameter | Symbol | Maximum Ratings | Unit |
|--------------------------------------|-----------------|------------------|------|
| Drain-Source Voltage | V_{DS} | 100 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current* | I_D | $T_c=25^\circ C$ | 28.1 |
| | | $T_c=70^\circ C$ | 22.5 |
| Pulsed Drain Current | I_{DM} | 112 | A |
| Maximum Power Dissipation* | P_D | $T_c=25^\circ C$ | 27.8 |
| | | $T_c=70^\circ C$ | 17.8 |
| Operating Junction Temperature | T_J | -55 to 150 | °C |
| Thermal Resistance-Junction to Case* | $R_{\theta JC}$ | 4.5 | °C/W |

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_c = 25°C Unless Otherwise Specified)

| Symbol | Parameter | Limit | Min | Typ | Max | Unit |
|----------------------|---|---|-----|------|------|------|
| STATIC | | | | | | |
| V _{(BR)DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D =250 μA | 100 | | | V |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250 μA | 1 | | 3 | V |
| I _{GSS} | Gate Leakage Current | V _{DS} =0V, V _{GS} =±20V | | | ±100 | nA |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =80V, V _{GS} =0V | | | 1 | μA |
| R _{DS(ON)} | Drain-Source On-State Resistance ^a | V _{GS} =10V, I _D = 20A | | 17 | 22 | mΩ |
| | | V _{GS} =4.5V, I _D = 16A | | 20 | 26 | |
| V _{SD} | Diode Forward Voltage | I _S =12A, V _{GS} =0V | | | 1.3 | V |
| DYNAMIC | | | | | | |
| Q _g | Total Gate Charge | V _{DS} =80V, V _{GS} =10V, I _D =35A | | 94.7 | | nC |
| Q _g | Total Gate Charge | | | 54.2 | | |
| Q _{gs} | Gate-Source Charge | V _{DS} =80V, V _{GS} =5V, I _D =35A | | 16.5 | | |
| Q _{gd} | Gate-Drain Charge | | | 20.8 | | |
| C _{iss} | Input capacitance | V _{DS} =15V, V _{GS} =0V, F=1MHz | | 4400 | | pF |
| C _{oss} | Output Capacitance | | | 286 | | |
| C _{rss} | Reverse Transfer Capacitance | | | 233 | | |
| t _{d(on)} | Turn-On Delay Time | V _{DS} =50V, R _L =1.5Ω V _{GEN} =10V, R _G =4.7Ω | | 30.3 | | ns |
| t _r | Turn-On Rise Time | | | 166 | | |
| t _{d(off)} | Turn-Off Delay Time | | | 92.4 | | |
| t _f | Turn-Off Fall Time | | | 186 | | |

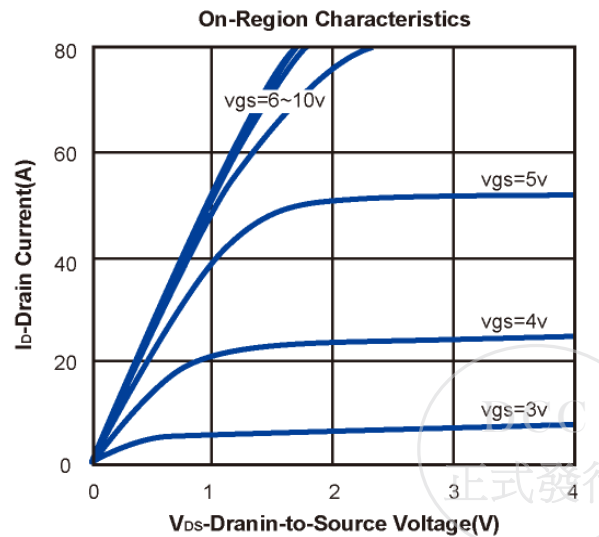
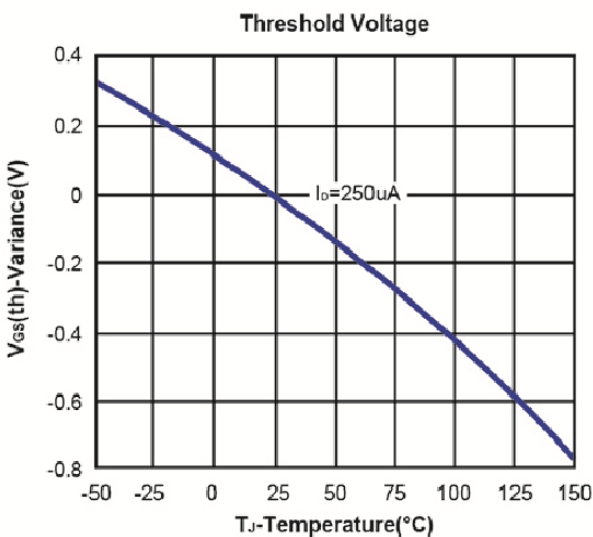
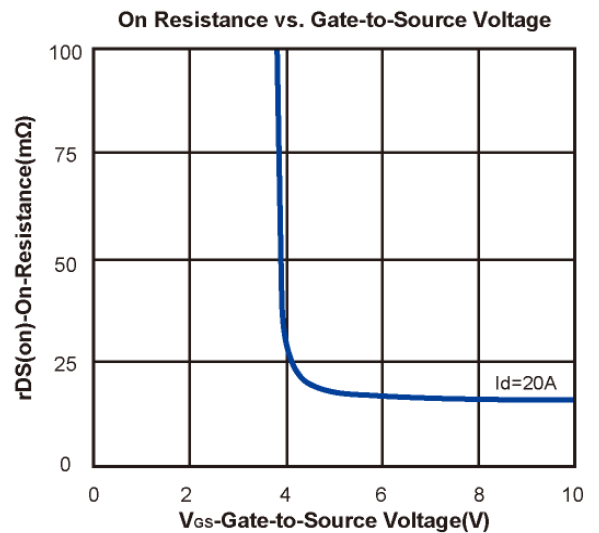
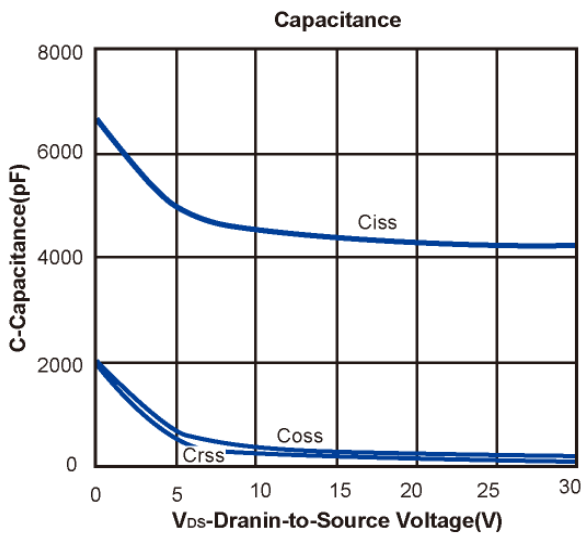
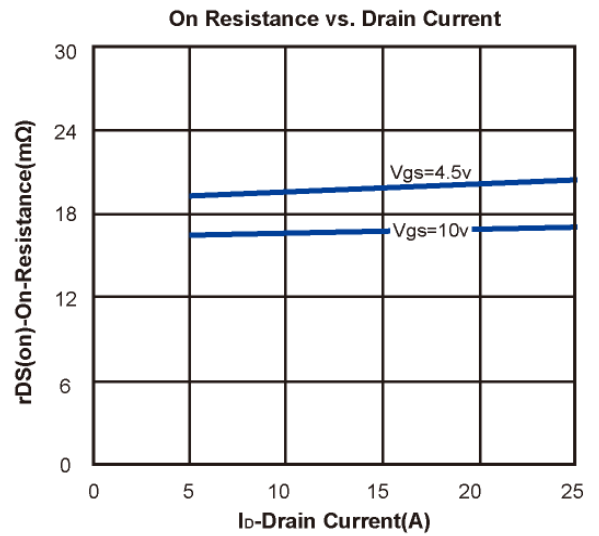
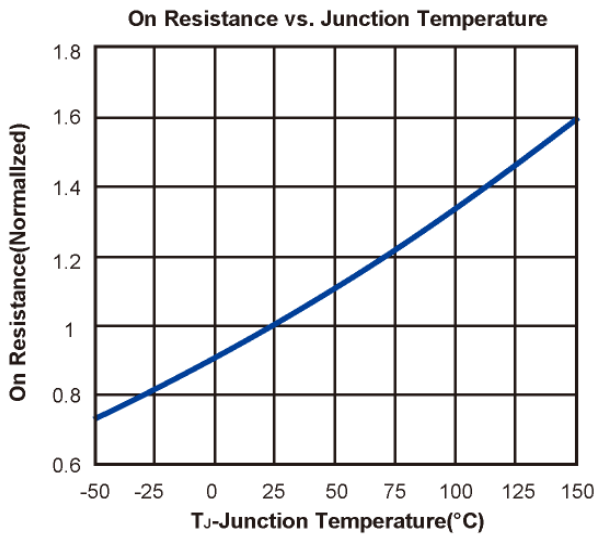
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

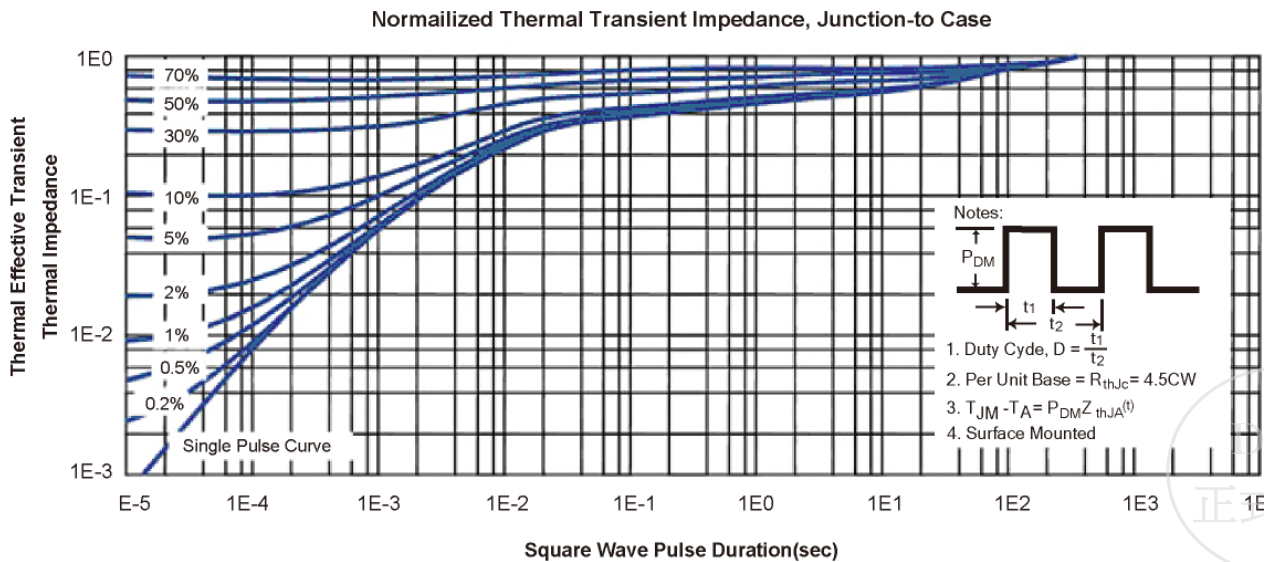
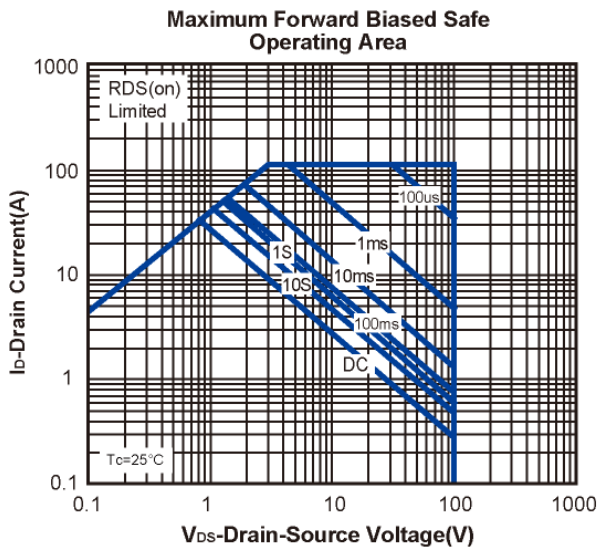
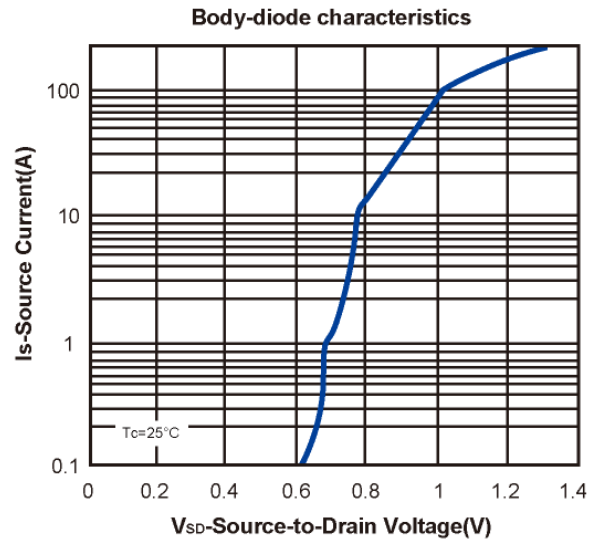
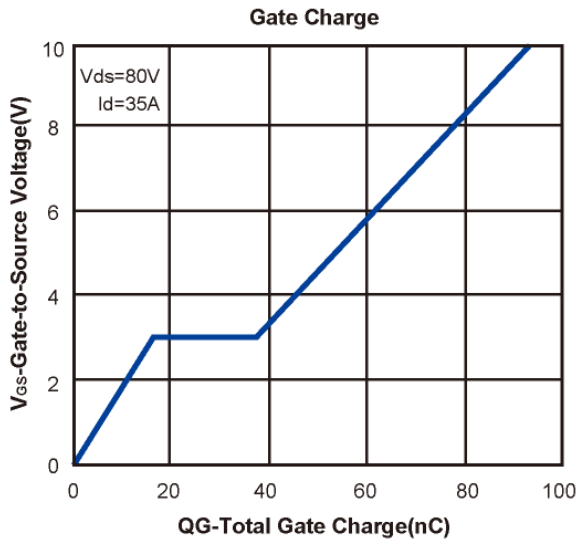
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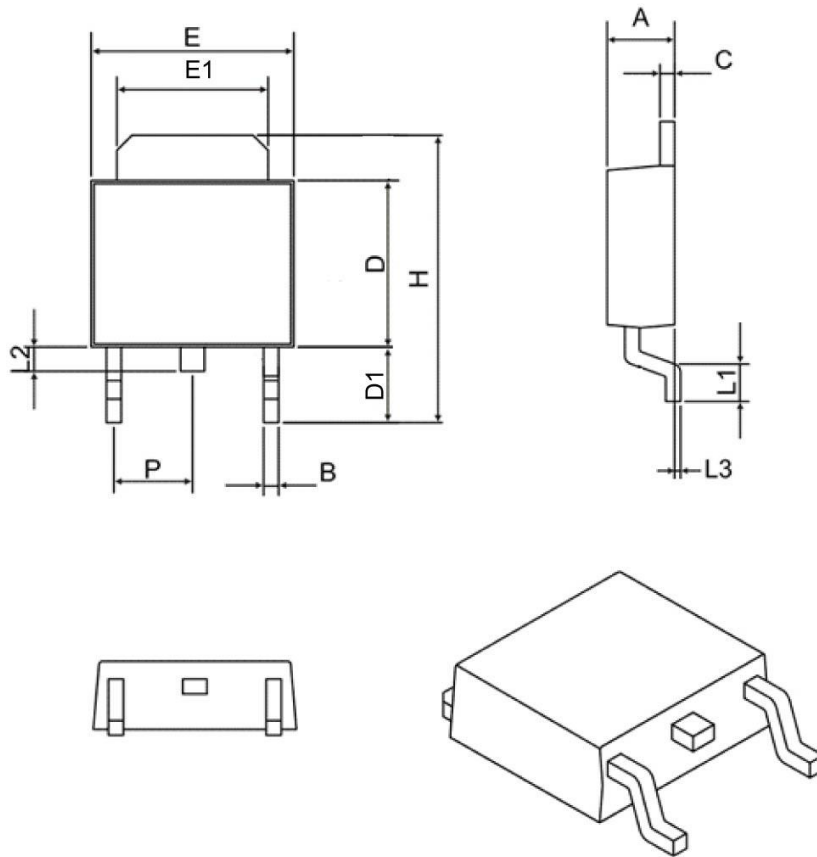
Typical Characteristics (T_J =25°C Noted)



N-Channel 100V (D-S) MOSFET
Typical Characteristics (T_J = 25°C Noted)



TO252-3L Package Outline



| SYMBOL | MIN | MAX |
|--------|----------|-------|
| A | 2.10 | 2.50 |
| B | 0.40 | 0.90 |
| C | 0.40 | 0.90 |
| D | 5.30 | 6.30 |
| D1 | 2.20 | 2.90 |
| E | 6.30 | 6.75 |
| E1 | 4.80 | 5.50 |
| L1 | 0.90 | 1.80 |
| L2 | 0.50 | 1.10 |
| L3 | 0.00 | 0.20 |
| H | 8.90 | 10.40 |
| P | 2.30 BSC | |

