

N - Channel 105-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2328 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

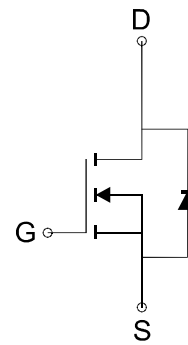
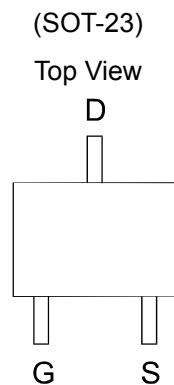
FEATURES

- $R_{DS(ON)} \leq 270m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 340m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET

Ordering Information: ME2328(Pb-free)

ME2328-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	105	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current (Tj=150°C)	$T_A=25^\circ C$	I_D	1.5	A
	$T_A=70^\circ C$		1.2	
Pulsed Drain Current		I_{DM}	6	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	1.3	W
	$T_A=70^\circ C$		0.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	105	110		V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1	2	3	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =105V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =1.5A		230	270	mΩ
		V _{GS} =4.5V, I _D =1.0A		275	340	
V _{SD}	Diode Forward Voltage *	I _{SD} =1.0A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =1.5A		12		nC
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =4.5V, I _D =1.5A		6.6		
Q _{gs}	Gate-Source Charge			2.6		
Q _{gd}	Gate-Drain Charge			3.3		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.8		Ω
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		326		pF
C _{oss}	Output Capacitance			38		
C _{rss}	Reverse Transfer Capacitance			11		
t _{d(on)}	Turn-On Delay Time	V _{DD} =50V, R _L =33Ω I _D =0.2A, V _{GEN} =10V, R _G =6Ω		10		ns
t _r	Turn-On Rise Time			6		
t _{d(off)}	Turn-Off Delay Time			30		
t _f	Turn-Off Fall Time			4		

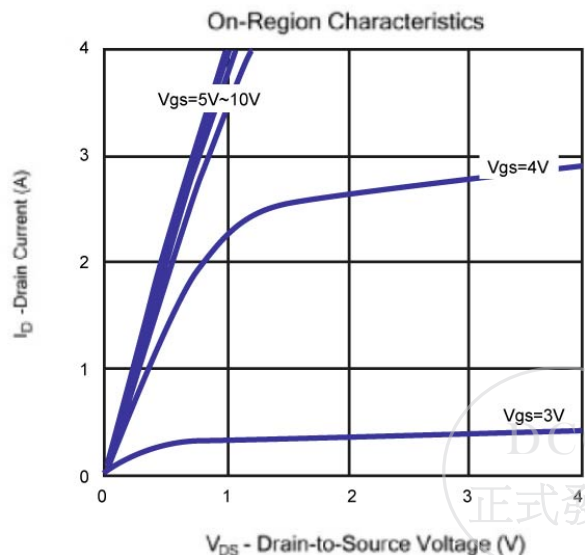
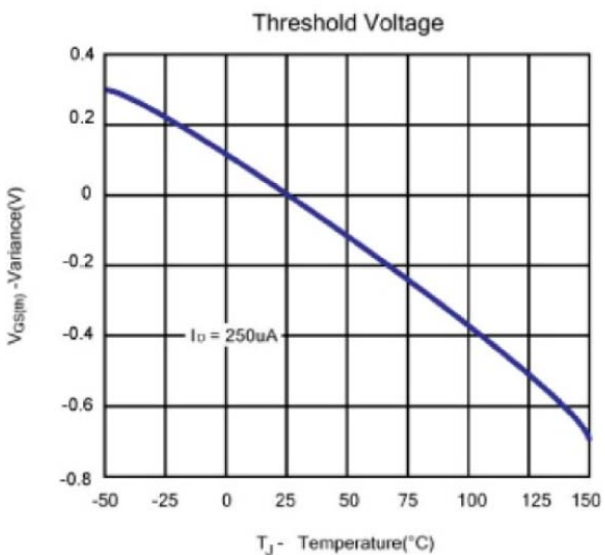
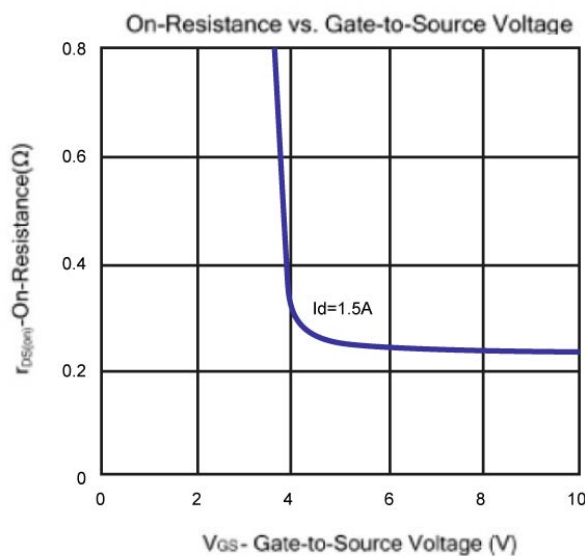
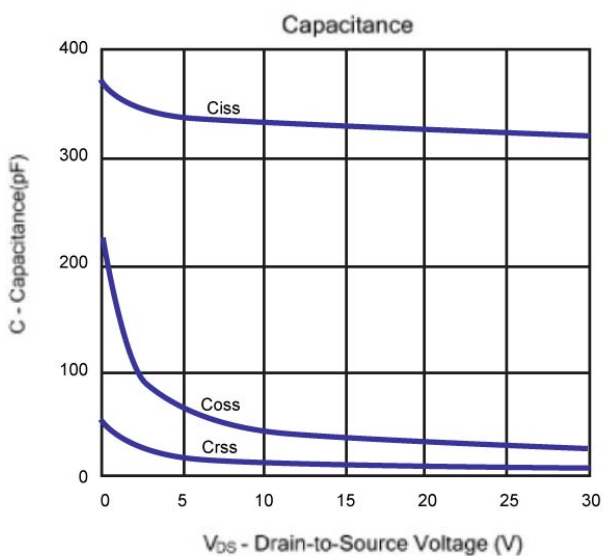
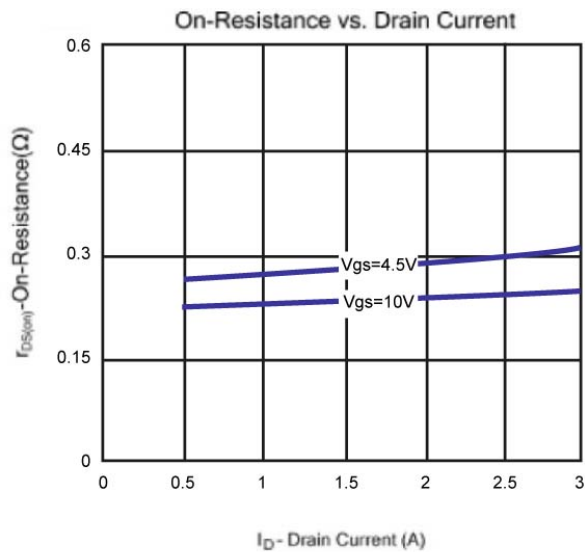
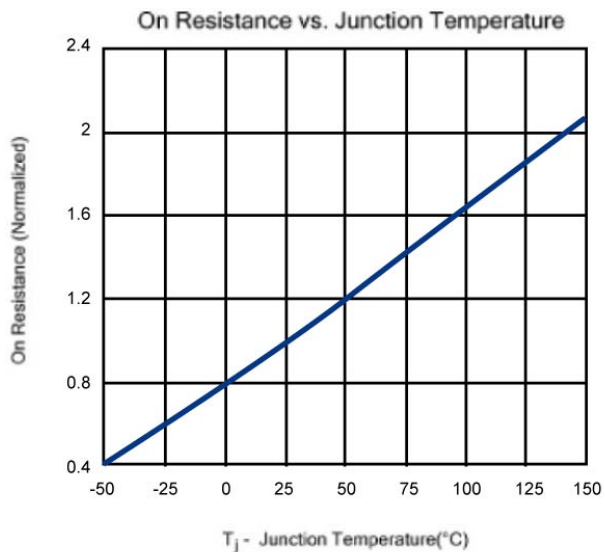
Notes: a, pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.



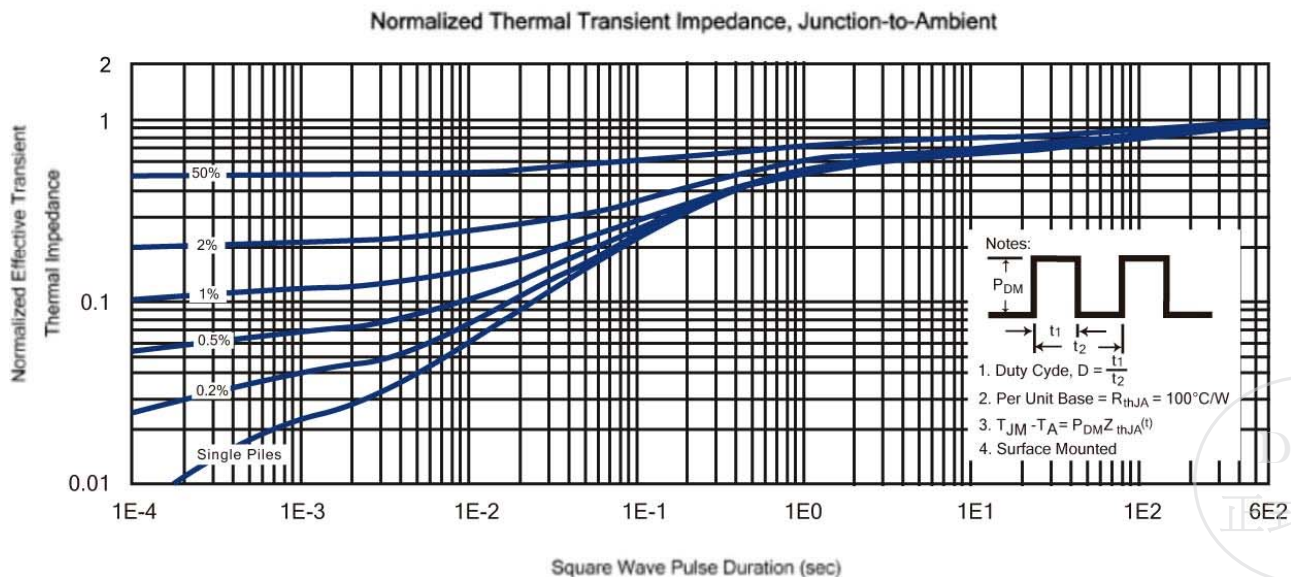
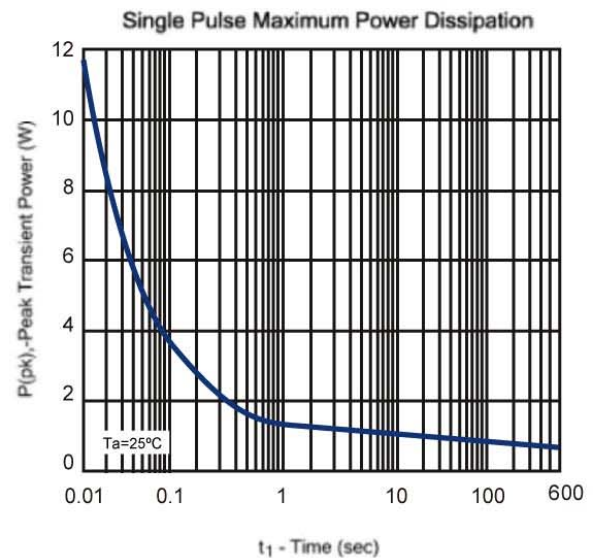
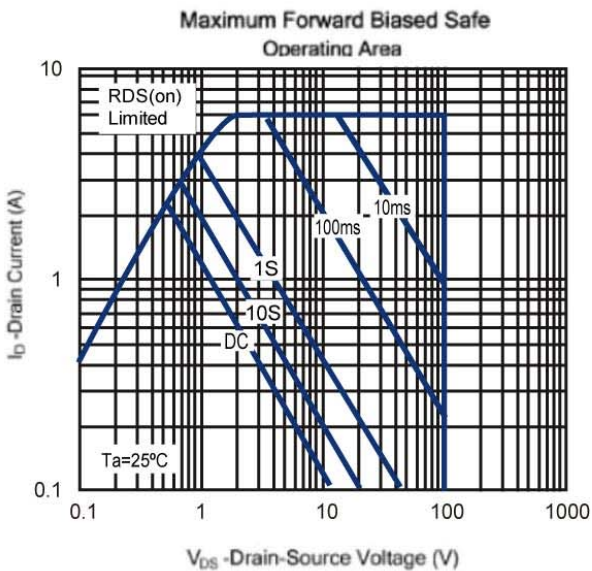
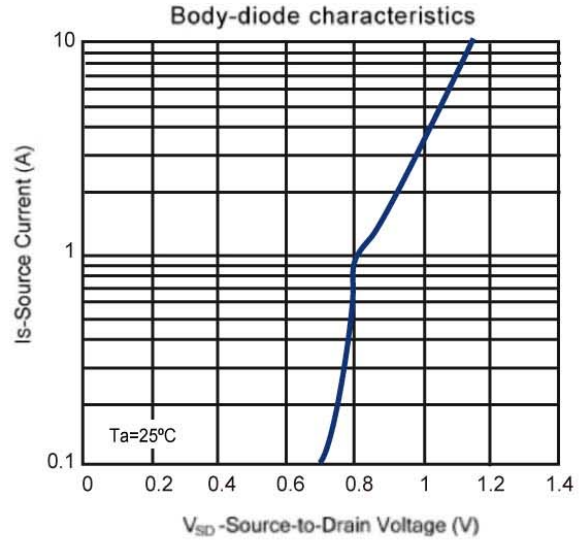
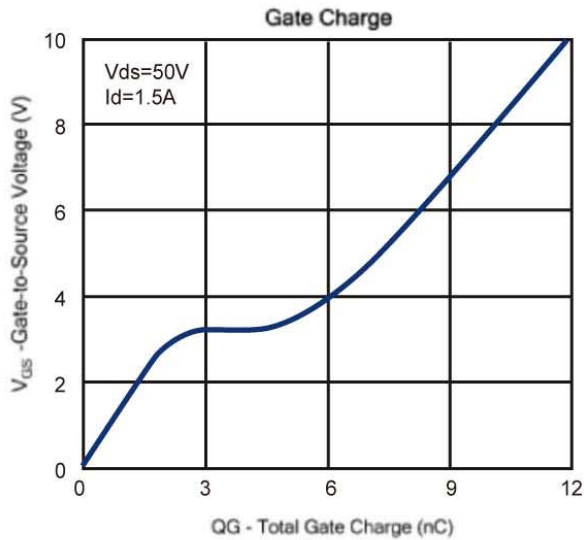
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Typical Characteristics (T_J = 25°C Noted)

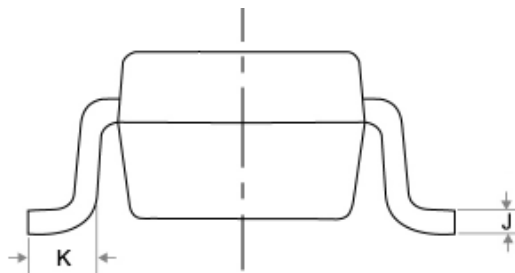
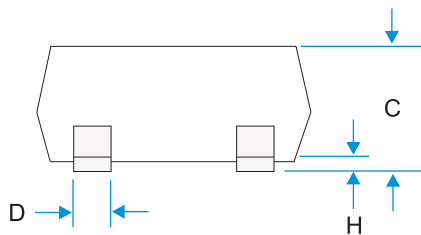
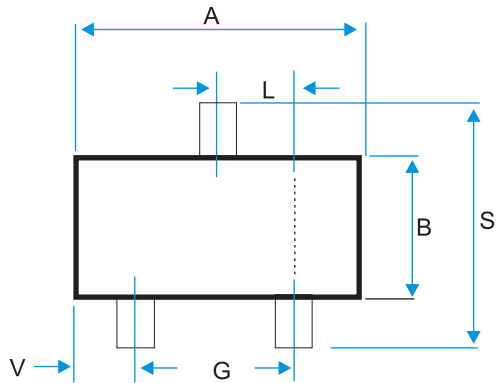


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SOT-23 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

