N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

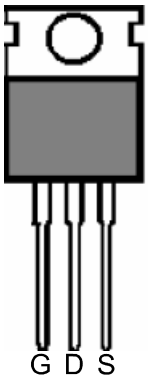
The ME110N10T and ME110N10F is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

FEATURES

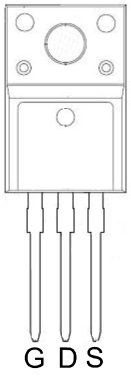
- $R_{DS(ON)} \leqq 6.2m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

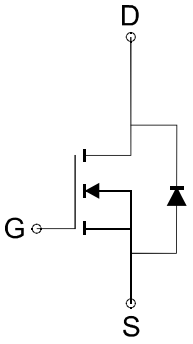
PIN CONFIGURATION

(TO-220AB)
Top View



(TO-220F)
Top View





N-Channel MOSFET

Ordering Information : ME110N10T(TO-220AB)
ME110N10F(TO-220F)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±25	V
Continuous Drain Current*	T_C=25℃	I_D	140	A
	T_C=100℃		105	
Pulsed Drain Current		I_{DM}	550	A
Maximum Power Dissipation	T_C=25℃	P_D	217	W
	T_C=100℃		108	
Operating Junction Temperature		T_J	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.69	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 140A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

N-Channel 100-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2	3	4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$ (TO-220AB)	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 70A		6.2	7.5	mΩ
$R_{DS(ON)}$ (TO-220F)	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 70A		7.0	8.0	mΩ
V_{SD}	Diode Forward Voltage	I_S=70A, V_{GS}=0V		0.8	1.0	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=70A		130		nC
Qgs	Gate-Source Charge			25		
Qgd	Gate-Drain Charge			32		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		6140		pF
Coss	Output Capacitance			943		
Crss	Reverse Transfer Capacitance			490		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.7		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=50V, R_G=6Ω, V_{GS}=10V, I_{DS}=70A		23		ns
tr	Turn-On Rise Time			39		
$t_{d(off)}$	Turn-Off Delay Time			86		
tf	Turn-Off Fall Time			46		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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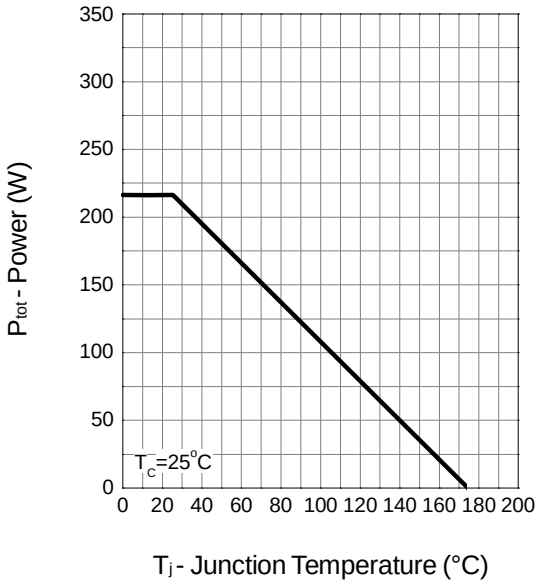
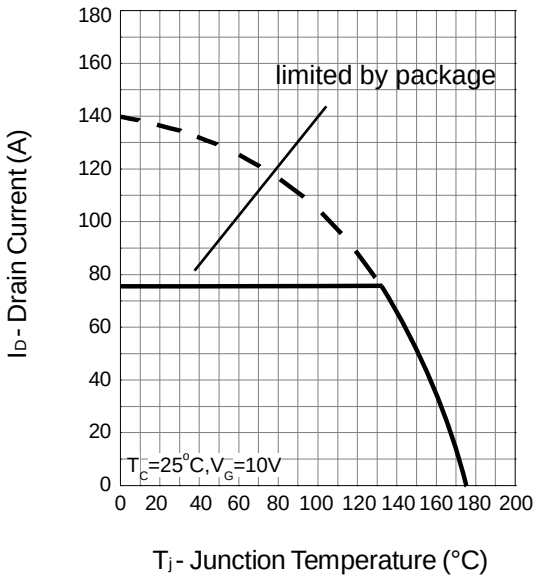
Typical Characteristics (T_J =25℃ Noted)

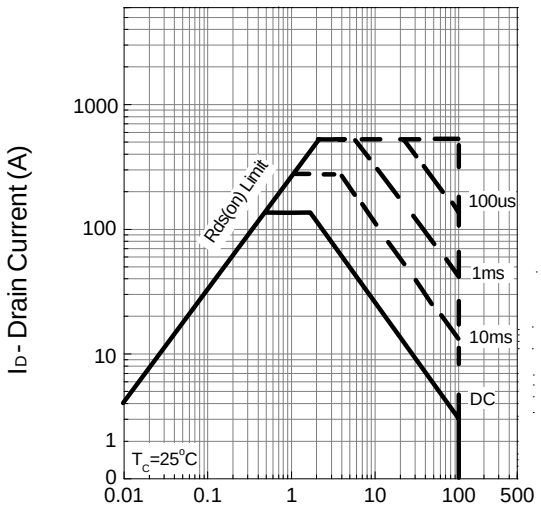
Power Dissipation



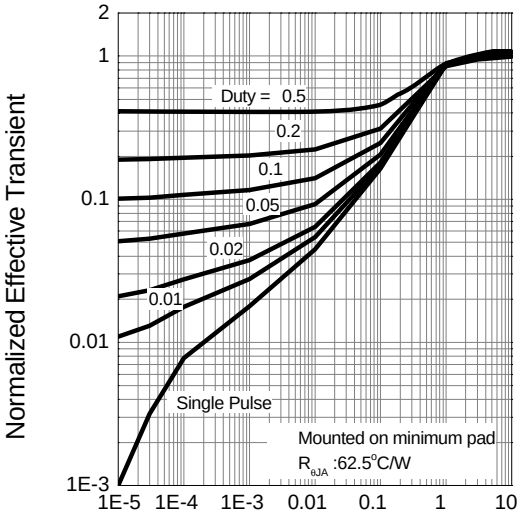
Drain Current



Safe Operation Area



Thermal Transient Impedance



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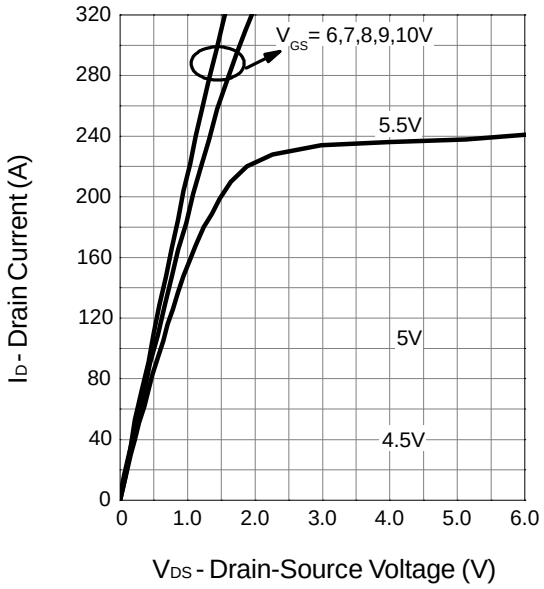
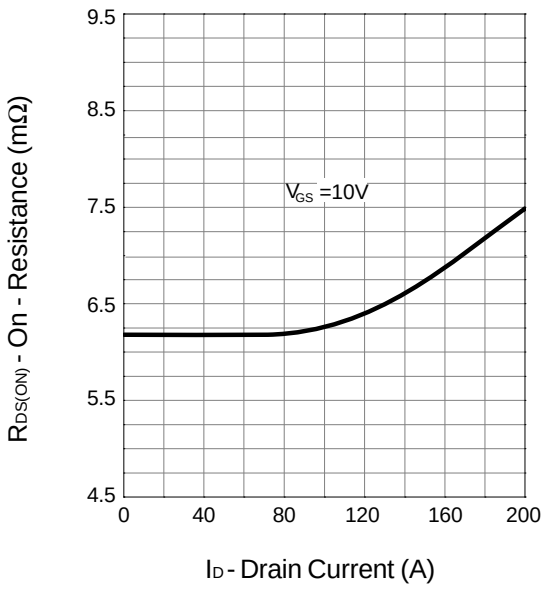
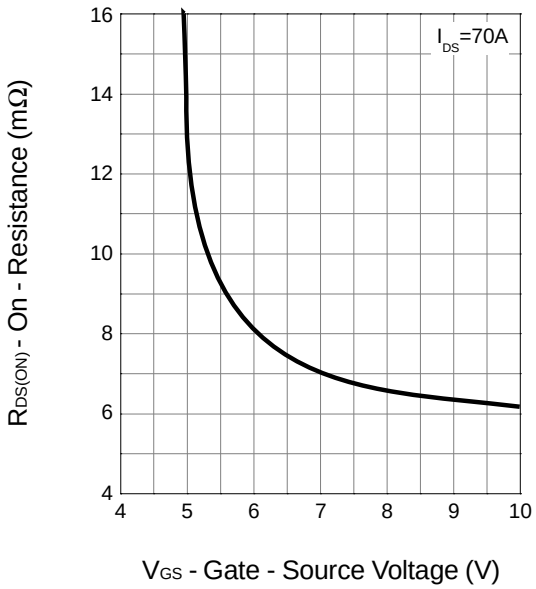
Output Characteristics



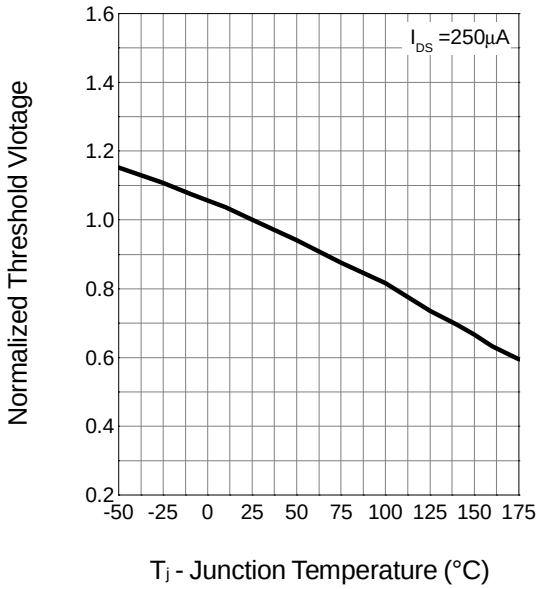
Drain-Source On Resistance



Drain-Source On Resistance



Gate Threshold Voltage



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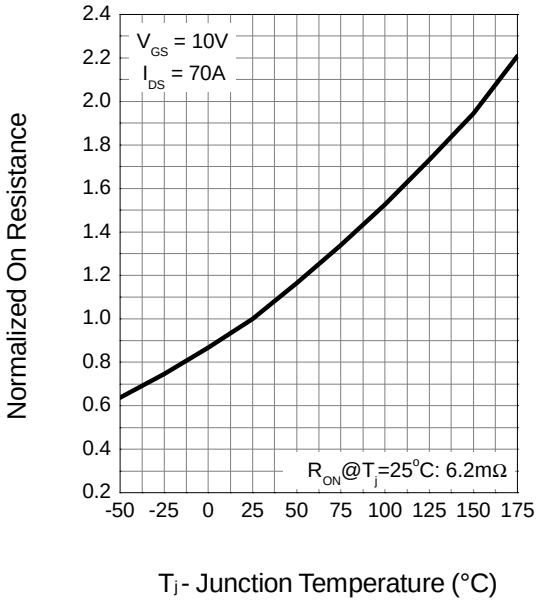
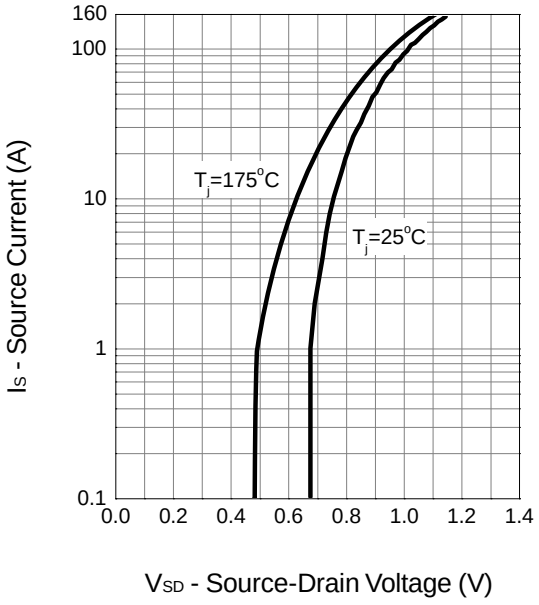
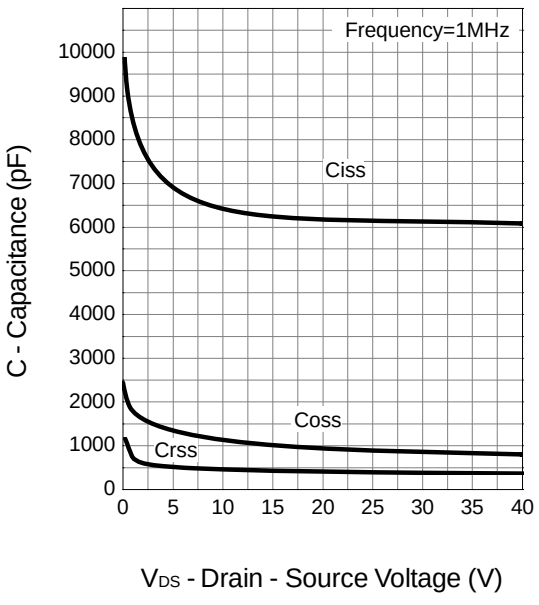
Drain-Source On Resistance



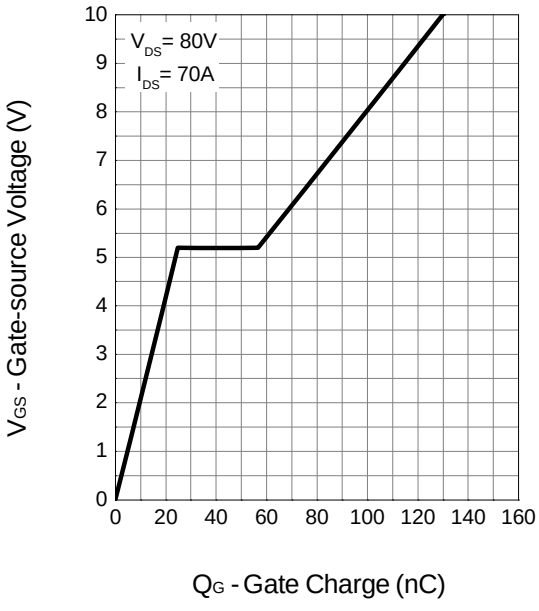
Source-Drain Diode Forward



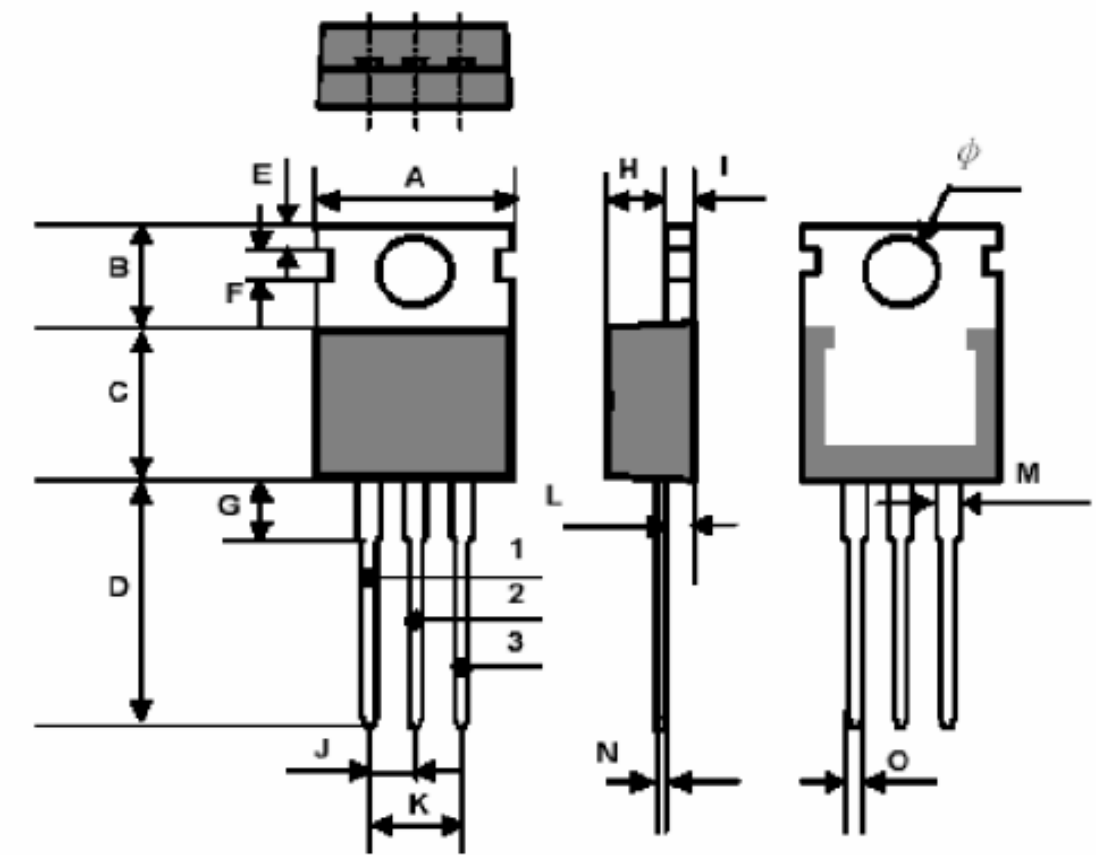
Capacitance



Gate Charge

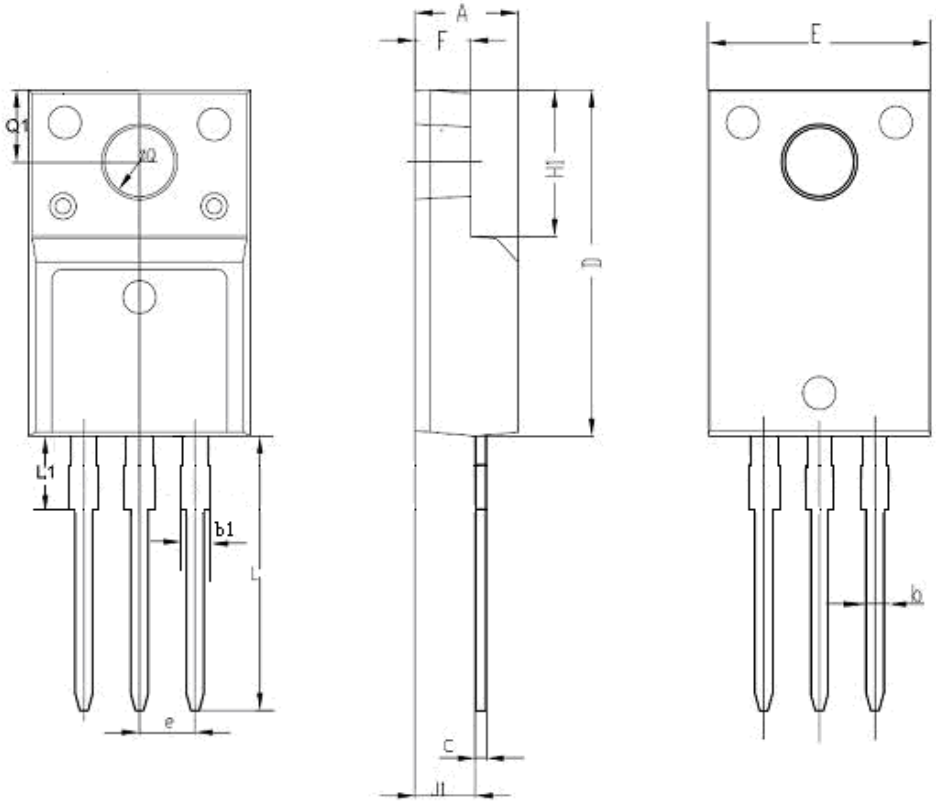


TO-220AB Package Outline



Symbol	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	9.7	10.1	0.382	0.398
B	6.3	6.7	0.248	0.264
C	9	9.47	0.354	0.373
D	12.8	13.3	0.504	0.524
E	1.2	1.4	0.047	0.055
F	1.7TYP		0.067TYP	
G	2.65TYP		0.104TYP	
H	3	3.4	0.118	0.134
I	1.25	1.4	0.049	0.055
J	2.4	2.7	0.094	0.106
K	5	5.15	0.197	0.203
L	2.2	2.6	0.087	0.102
M	1.25	1.45	0.049	0.057
N	0.45	0.6	0.018	0.024
O	0.7	0.9	0.027	0.035
ϕ	3.6		0.142	

TO-220F Package Outline



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.178	0.194	4.53	4.93	
b	0.028	0.036	0.71	0.91	
C	0.018	0.024	0.45	0.60	
D	0.617	0.633	15.67	16.07	
E	0.392	0.408	9.96	10.36	
e	0.100 TYP.		2.54TYP.		
H1	0.256	0.272	6.50	6.90	
J1	0.101	0.117	2.56	2.96	
L	0.503	0.519	12.78	13.18	
φQ	0.117	0.133	2.98	3.38	
b1	0.045	0.055	1.15	1.39	
L1	0.114	0.130	2.9	3.3	
Q1	0.122	0.138	3.10	3.50	
F	0.092	0.108	2.34	2.74	