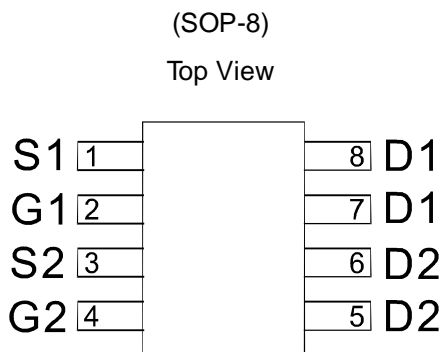


Dual N- Channel 100V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4954 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

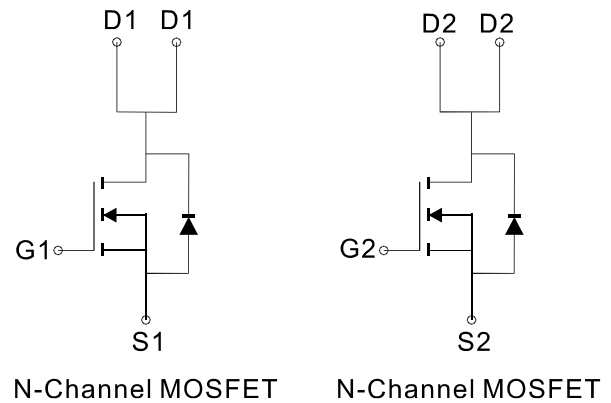


FEATURES

- $R_{DS(ON)} \leq 80m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 98m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



Ordering Information: ME4954 (Pb-free)

ME4954-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current*	I_D	$T_A=25^\circ C$	4
		$T_A=70^\circ C$	3.2
Pulsed Drain Current	I_{DM}	16	A
Maximum Power Dissipation*	P_D	$T_A=25^\circ C$	2
		$T_A=70^\circ C$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	62.5	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



Dual N- Channel 100V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

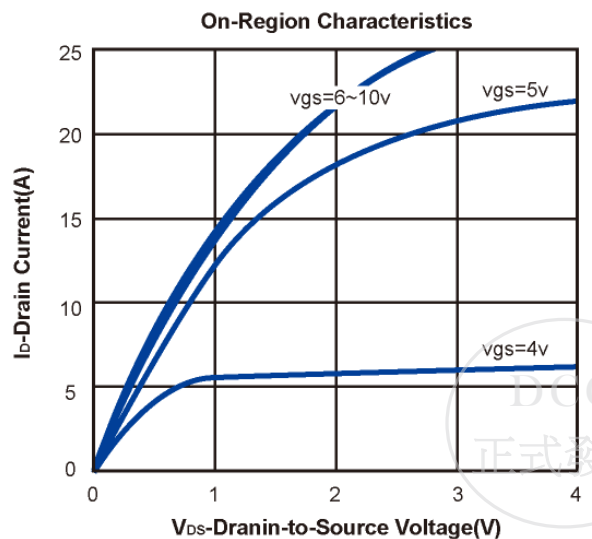
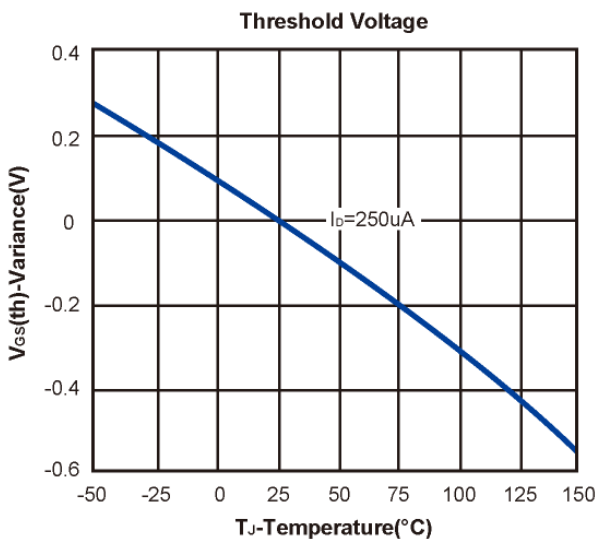
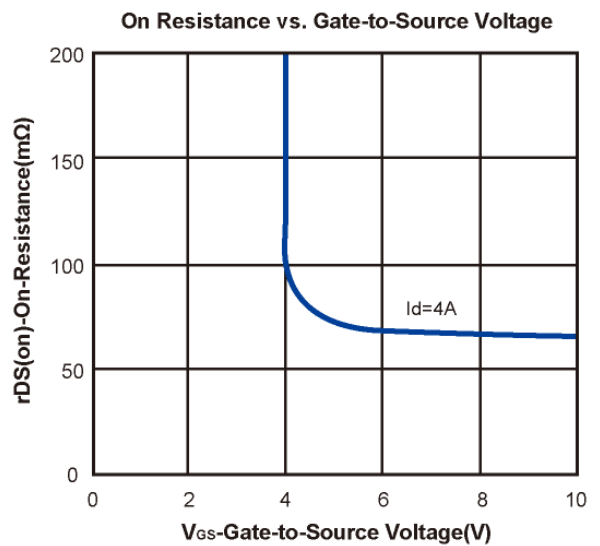
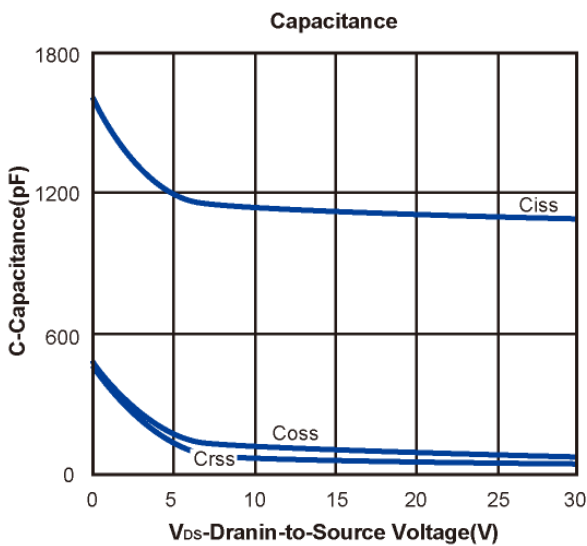
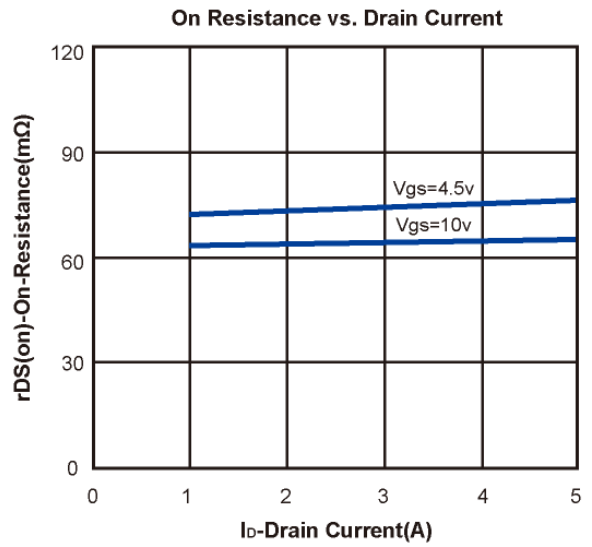
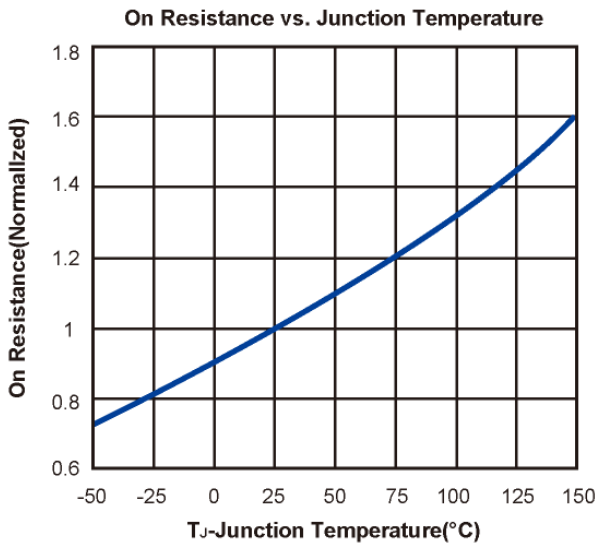
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250 μA	100			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250 μA	1		2.5	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=80V, VGS=0V			1	μA
RDS(ON)	Drain-Source On-State Resistance ^a	VGS=10V, ID= 4A		65	80	mΩ
		VGS=4.5V, ID= 3.2A		75	98	
VSD	Diode Forward Voltage	IS=12A, VGS=0V			1.3	V
DYNAMIC						
Qg	Total Gate Charge	VDS=80V, VGS=10V, ID=4A		28.8		nC
Qg	Total Gate Charge	VDS=80V, VGS=5V, ID=4A		17.4		
Qgs	Gate-Source Charge			9.9		
Qgd	Gate-Drain Charge			5.6		
Ciss	Input capacitance	VDS=20V, VGS=0V, F=1MHz		1106		pF
Coss	Output Capacitance			73		
Crss	Reverse Transfer Capacitance			46		
Rg	Gate Resistance	VDS=0V, VGS=0V, f=1MHz		2		Ω
td(on)	Turn-On Delay Time	VDS=50V, RL =12.5Ω VGEN=5V, RG=4.7Ω ID=4A		27.3		ns
tr	Turn-On Rise Time			89.9		
td(off)	Turn-Off Delay Time			36.8		
tf	Turn-Off Fall Time			11		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

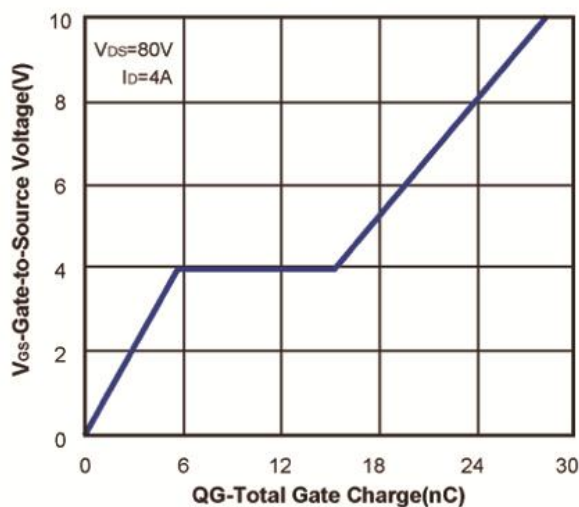
DCC
正式發行

Dual N- Channel 100V (D-S) MOSFET
Typical Characteristics (T_J = 25°C Noted)

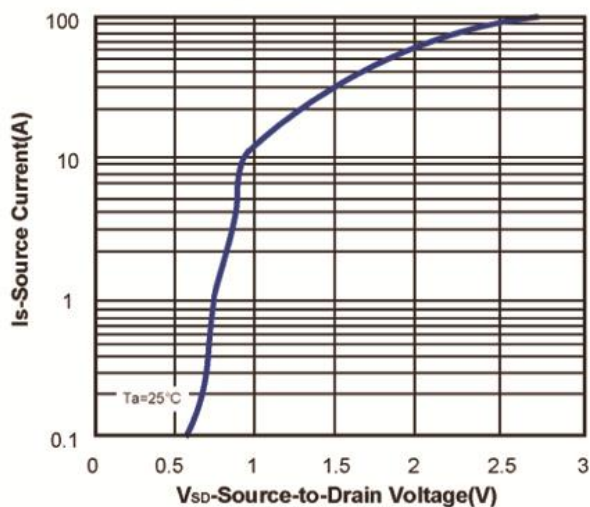


Dual N- Channel 100V (D-S) MOSFET
Typical Characteristics (T_J = 25°C Noted)

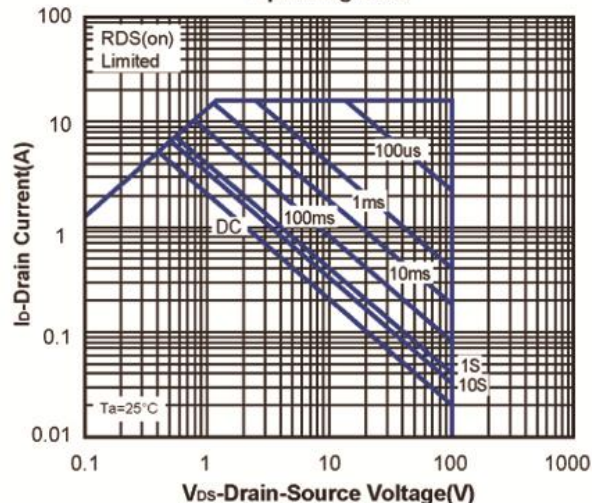
Gate Charge



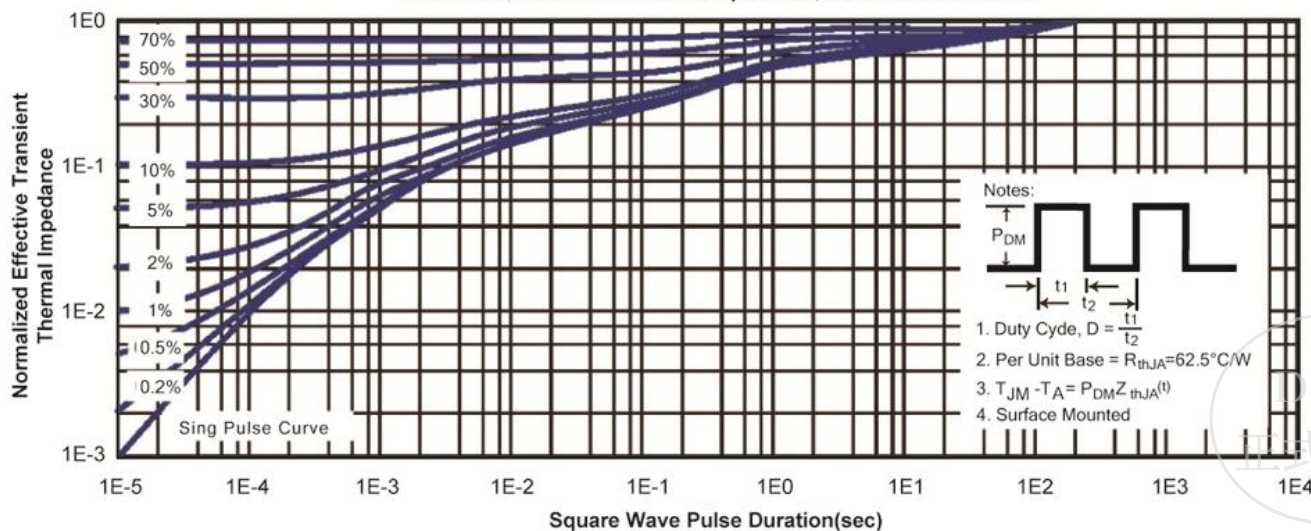
Body-diode characteristics



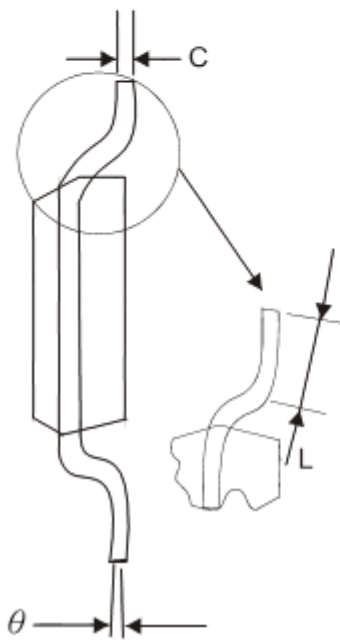
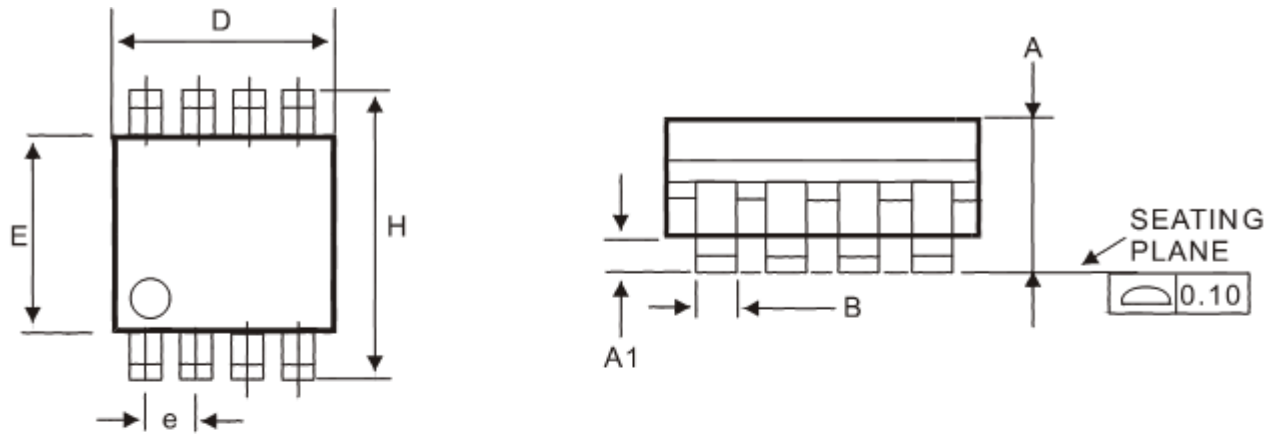
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

