ME120N10T/ME120N10T-G

N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME120N10T is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

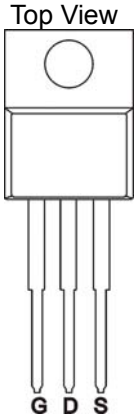
FEATURES

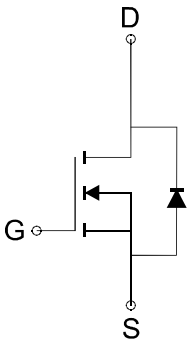
- $R_{DS(ON)} \leqq 5.0m\Omega$ @V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION

(TO-220)

Top View





N-Channel MOSFET

Ordering Information: ME120N10T(Pb-free)
ME120N10T-G(Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±25	V
Continuous Drain Current*	T_C=25℃	I_D	180	A
	T_C=100℃		132	
Pulsed Drain Current		I_{DM}	640	A
Maximum Power Dissipation	T_C=25℃	P_D	250	W
	T_C=100℃		125	
Operating Junction Temperature		T_J	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.6	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 180A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

N-Channel 100-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2	3	4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 90A		5.0	6.5	mΩ
V_{SD}	Diode Forward Voltage	I_S=90A, V_{GS}=0V		0.8	1.0	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=80V, V_{GS}=10V, I_D=90A		180		nC
Qgs	Gate-Source Charge			34		
Qgd	Gate-Drain Charge			60		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		7889		pF
Coss	Output Capacitance			1013		
Crss	Reverse Transfer Capacitance			631		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		2.3		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=50V, R_G=6Ω, V_{GS}=10V, I_{DS}=90A		28		ns
tr	Turn-On Rise Time			45		
$t_{d(off)}$	Turn-Off Delay Time			85		
tf	Turn-Off Fall Time			50		

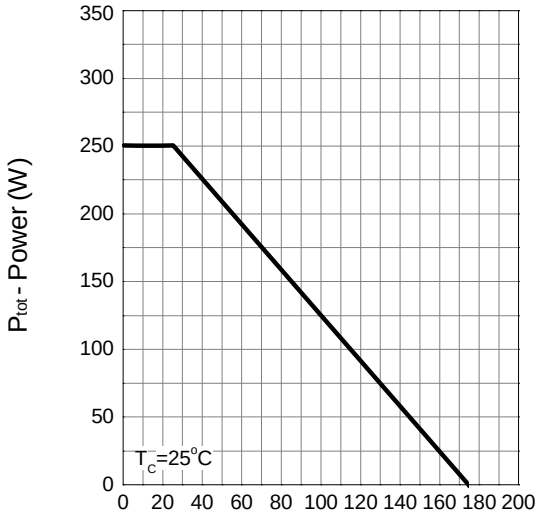
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

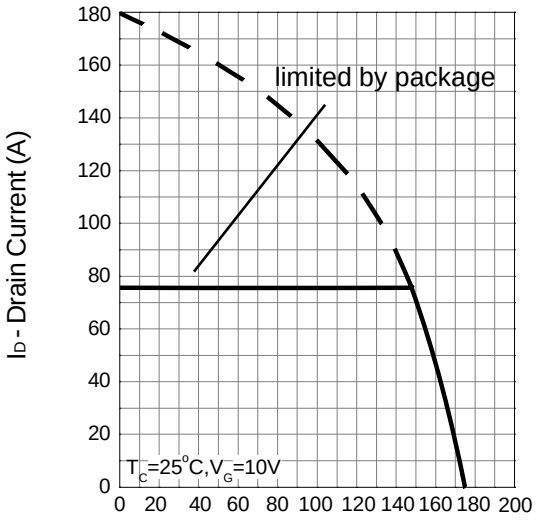
N-Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

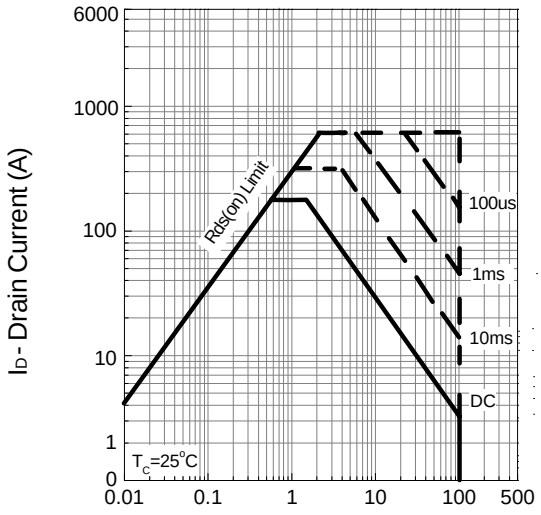
Power Dissipation



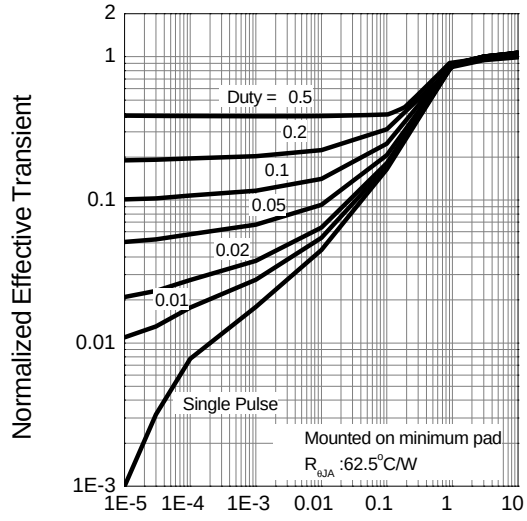
Drain Current



Safe Operation Area



Thermal Transient Impedance



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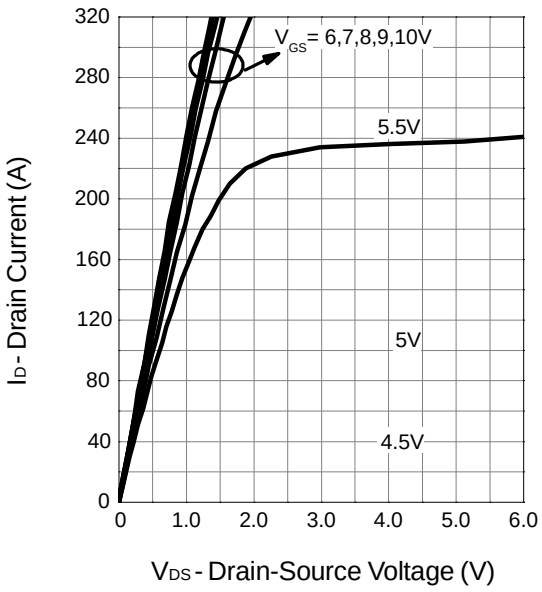
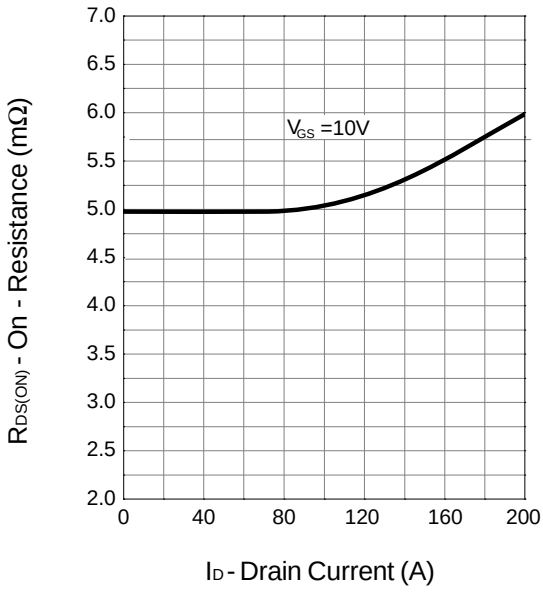
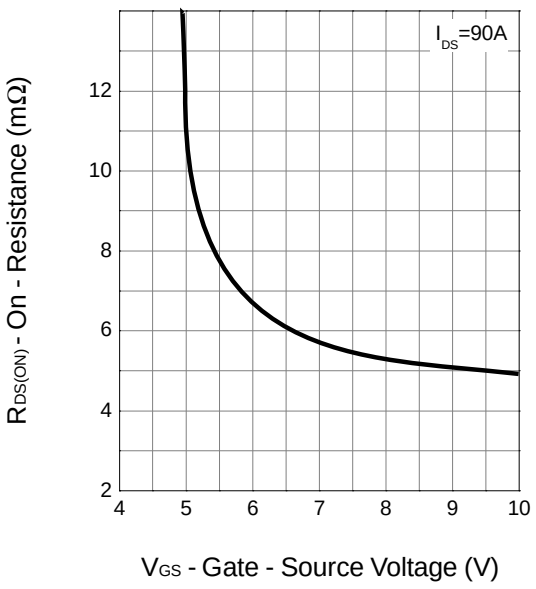
Output Characteristics



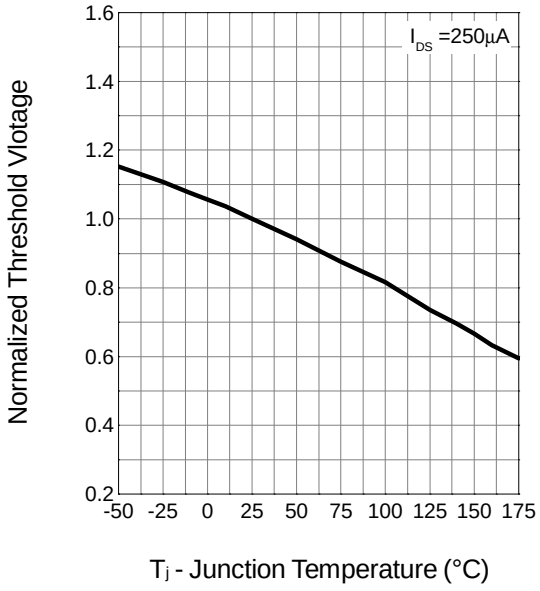
Drain-Source On Resistance



Drain-Source On Resistance



Gate Threshold Voltage



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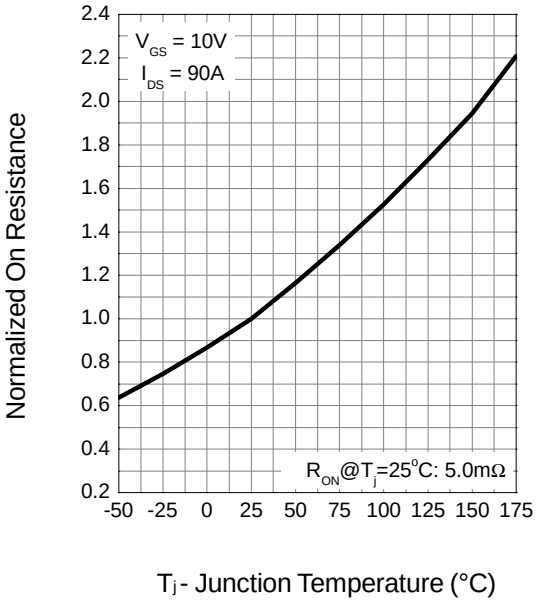
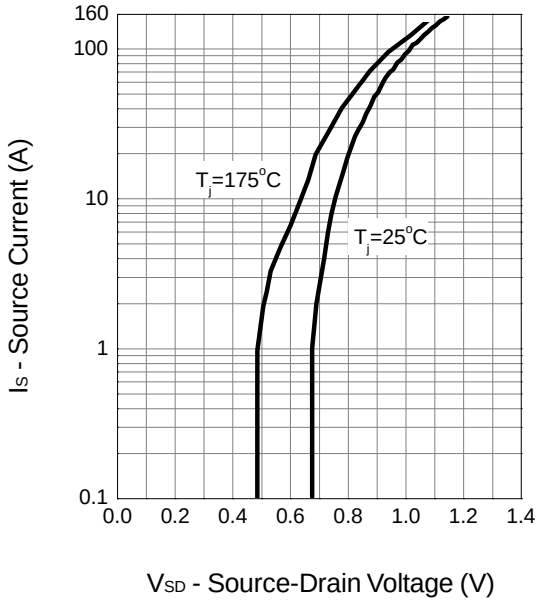
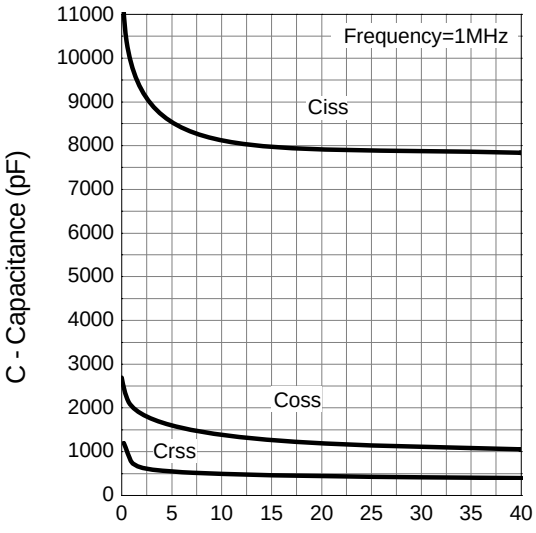
Drain-Source On Resistance



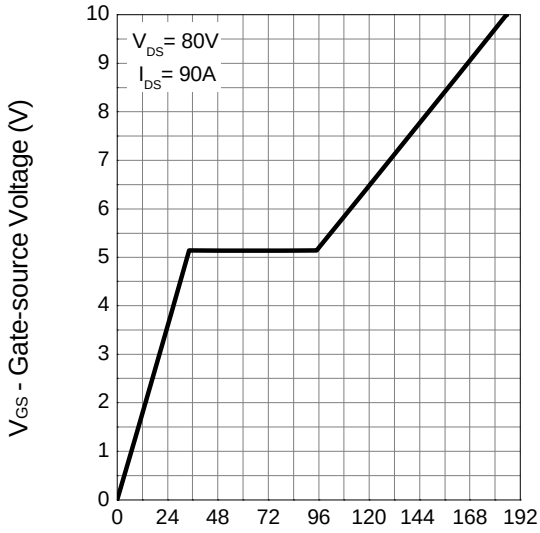
Source-Drain Diode Forward



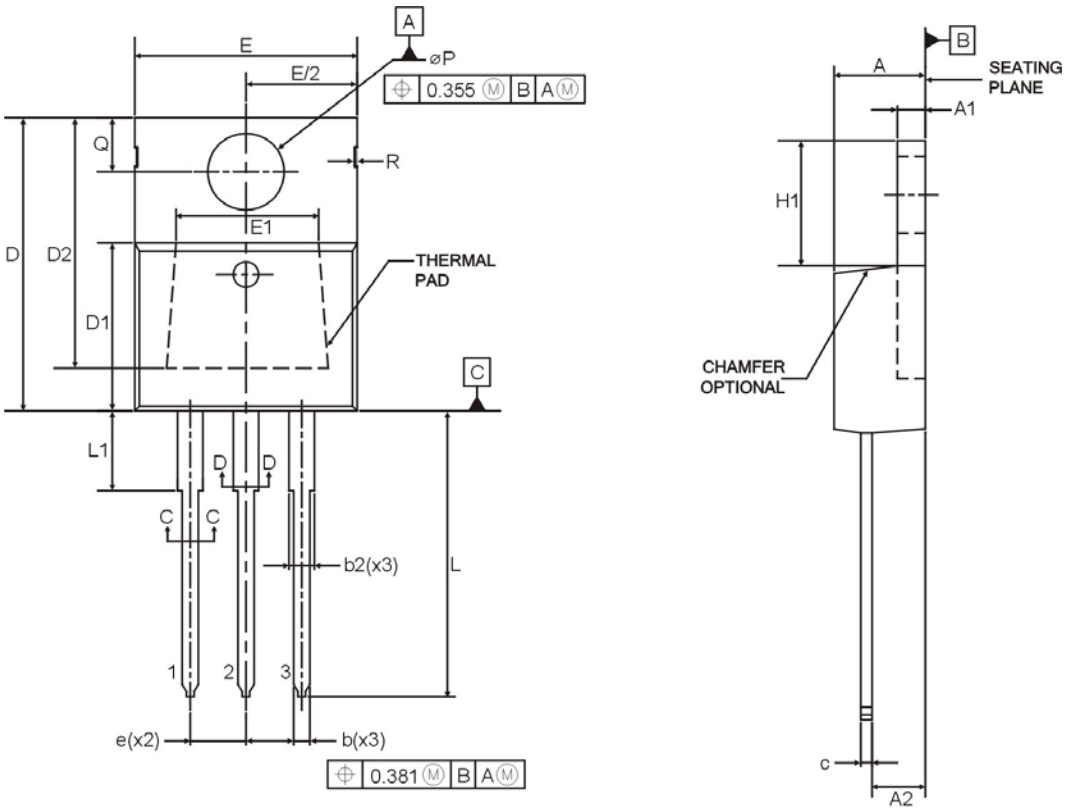
Capacitance

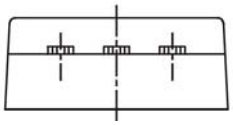


Gate Charge



TO-220 Package Outline





SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	3.500	4.90
A1	1.000	1.40
A2	2.000	3.00
b	0.500	1.00
c	0.350	0.65
D	14.00	16.50
D1	8.382	9.017
D2	12.00	13.00
E	9.600	10.70
E1	6.858	8.890
e	2.540 BSC	
H1	5.500	7.50
L	12.50	15.00
ØP	3.810	3.860
Q	2.540	3.048
b2	1.100	1.80
L1	-	7.00