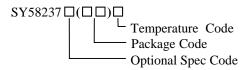
General Description

SY58237 is a single stage Flyback regulator targeting at LED lighting applications.

SY58237 integrates a 650V MOSFET to decrease physical volume. It adopts the proprietary control architecture to achieve an accurate regulation of LED current, Quasi-Resonant valley turn-on for high efficiency operation. Proprietary self-bias technique saves the bias supply and reduces the start up time.

SY58237 integrates open/short LED protection and eliminates the need for opto-coupler or auxiliary winding (in floating switch application), thus minimizing the component count and board size.

Ordering Information



| Ordering Number | Package type | Note |
|-----------------|--------------|------|
| SY58237AGC | DIP8 | |

Features

- Integrated 650V MOSFET
- Quasi-Resonant (QR) Mode to Achieve Low Switching Losses
- No Opto-coupler or Auxiliary Winding for Feedback in the Proprietary Floating Switch Configuration.
- Reliable Short LED and Open LED Protection
- Thermal Foldback Function
- Compact Package: DIP8

Applications

• LED Lighting

Typical Applications

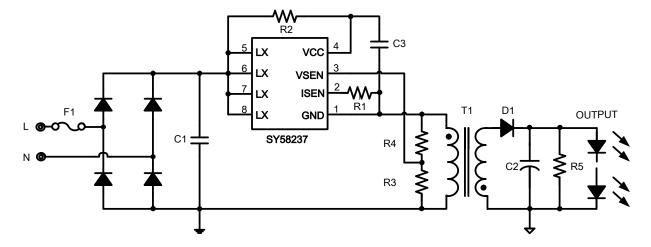
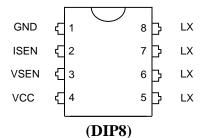


Fig.1 Schematic Diagram



Pinout (top view)



Top Mark: BXUxyz (device code: BXU, x=year code, y=week code, z= lot number code)

| Pin Name | Pin number | Pin Description | | | |
|----------|------------|--|--|--|--|
| GND | 1 | Ground Pin. | | | |
| ISEN | 2 | Current set pin. Connect a resistor to program the reference output current. $I_O = \frac{V_{REF} \times N_{PS}}{2 \times R_{ISEN}}$ | | | |
| VSEN | 3 | Voltage sense pin. Connect to a resistor divider of inductor or auxiliary winding to sense output voltage. | | | |
| VCC | 4 | Power supply pin. | | | |
| LX | 5-8 | Internal HV MOSFET drain pin. | | | |

Block Diagram

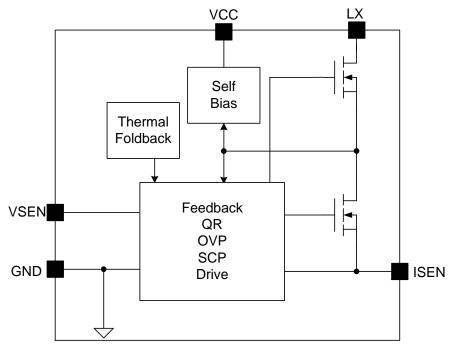


Fig.2 Simplified block diagram





Absolute Maximum Ratings (Note 1)

| 1100014te 114211114111 1tatings (1tote 1) | |
|---|--------|
| ISEN | |
| VSEN | |
| VCC | |
| LX | 650V |
| Power Dissipation, @ TA = 25°C DIP8 | 0.6W |
| Package Thermal Resistance (Note 2) | |
| DIP8, θ_{JA} | 68°C/W |
| DIP8, θ_{JC} | 55°C/W |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | |



Electrical Characteristics

 $(V_{VCC} = 12V \text{ (Note 3)}, T_A = 25^{\circ}\text{C unless otherwise specified)}$

| Parameter | Symbol | Test Conditions | Min | Тур | Max | Unit |
|---------------------------------|----------------------|-----------------------------|-----|-----|-----|------|
| Power Supply Section | | | | | | |
| VCC Turn-on Threshold | V_{VCC_ON} | | | 14 | | V |
| VCC Turn-off Threshold | V_{VCC_OFF} | | | 7 | | V |
| Start up Current | I_{ST} | VCC=13V | | 32 | | μA |
| Quiescent Current | I_Q | VCC=15V | | 125 | | μA |
| Shunt Current | I_{Shunt} | VCC=V _{VCC_ON} +4V | | 17 | | mA |
| VSEN Pin Section | | | | | | |
| VSEN Pin Reference Voltage | V_{VSEN_OVP} | | | 1.5 | | V |
| Driver Section | | | | | | |
| Min ON Time | T _{ON_MIN} | | | 450 | | ns |
| Max ON Time | T _{ON_MAX} | | | 13 | | μs |
| Min OFF Time | T _{OFF_MIN} | | | 1.7 | | μs |
| Max OFF Time | T_{OFF_MAX} | | | 420 | | μs |
| Max Switching Frequency | F_{MAX} | | | 150 | | kHz |
| ISEN Pin Section | | | | | | |
| Current Limit Threshold Voltage | V_{ISEN_OCP} | | | 485 | | mV |
| Current Reference | $V_{\rm ISEN}$ | | 294 | 300 | 306 | mV |
| Integrated MOSFET Section | | | | | | |
| BV of HV MOSFET | V_{BV} | | 650 | | | V |
| Rdson of HV MOSFET | R_{DSON} | | | | 3.4 | Ω |
| Thermal Section | | | | | | |
| Thermal Foldback Temperature | T_{FB} | | | 155 | | °C |

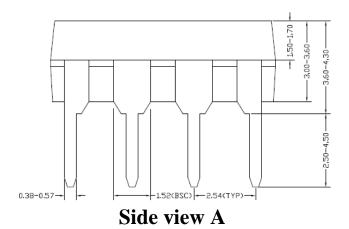
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

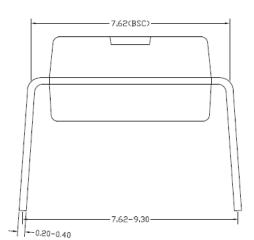
Note 2: θ_{JA} is measured in the natural convection at $T_A = 25$ °C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then turn down to 12V.

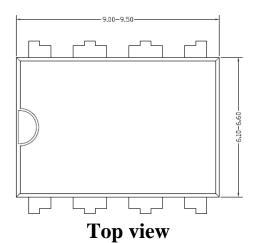


DIP8 Package Outline





Side view B



Notes: All dimension in millimeters and exclude mold flash & metal burr