

650V N-Channel Silicon Carbide Power MOSFET

FEATURES

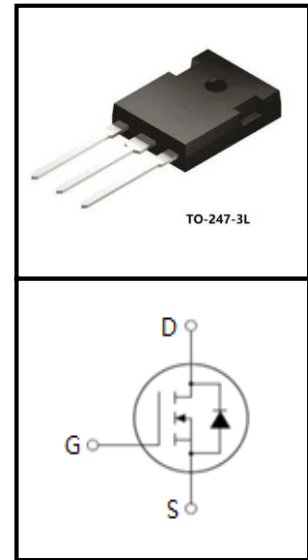
- Low On-Resistance
- Low Capacitance
- Avalanche Ruggedness
- Halogen Free, RoHS Compliant

BENEFITS

- Higher System Efficiency
- Parallel Device Convenience
- High Temperature Application
- High Frequency Operation

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Uninterruptible Power Supply (UPS)
- EV Charging station & Motor Drives
- Solar/ Wind Renewable Energy
- Power Inverters & DC/DC Converters



Device Marking and Package Information		
Device	Package	Marking
C2M065W030	TO-247-3L	C2M065W030

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted				
Parameter	Symbol	Test Conditions	Value	Unit
Drain-Source Voltage	V_{DSS}	$V_{GS}=0V, I_{DS}=100\mu A$	650	V
Continuous Drain Current	I_D	$V_{GS}=20V, T_C=25^\circ C$	100	A
Pulsed Drain Current	I_{DM}	t_{PW} limitation per Fig.17	400	
Power Dissipation	P_D	$T_C=25^\circ C$	338	W
Recommend Gate Source Voltage	$V_{GS, op}$	Static	-5/+20	V
Maximum Gate Source Voltage	$V_{GS, max}$	AC ($f > 1\text{Hz}$)	-10/+25	
Soldering Temperature	T_L		260	$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}		-55/+150	

Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	0.37	K/W

Specifications $T_J = 25^{\circ}\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 100\mu A$	650	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V, T_J = 25^{\circ}\text{C}$	--	<1	100	μA
		$V_{DS} = 650V, V_{GS} = 0V, T_J = 150^{\circ}\text{C}$	--	10	500	
Gate-Source Leakage	I_{GSS}	$V_{GS} = 20V, V_{DS} = 0V$	--	--	200	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = 10V, I_D = 5mA$	2	--	3.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 20V, I_D = 30A$	--	30	36	m Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 1.0MHz$ $V_{AC} = 25mV$	--	2333	--	μF
Output Capacitance	C_{oss}		--	264	--	
Reverse Transfer Capacitance	C_{rss}		--	46	--	
Effective Output Capacitance, Energy Related	$C_{o(er)}$		$V_{GS} = 0V$ $V_{DS} = 0$ to 450V		187	
Effective Output Capacitance, Time Related	$C_{o(tr)}$	$I_D = \text{const.}, V_{GS} = 0V$ $V_{DS} = 0$ to 450V		253		
Total Gate Charge	Q_g	$V_{DS} = 300V,$ $V_{GS} = 0/+15V,$ $I_D = 50A$	--	140	--	nC
Gate-Source Charge	Q_{gs}		--	26	--	
Gate-Drain Charge	Q_{gd}		--	69	--	
Gate plateau voltage	V_{pl}		--	10	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 300V$ $V_{GS} = 0/15V$ $I_D = 50A$ $R_{G(ext)} = 2.5\Omega$	--	45	--	ns
Turn-on Rise Time	t_r		--	107	--	
Turn-off Delay Time	$t_{d(off)}$		--	67	--	
Turn-off Fall Time	t_f		--	16	--	
Coss Stored Energy	E_{oss}	$V_{GS} = 0V, V_{DS} = 650V$ $f = 1MHz, V_{AC} = 25mV$	--	119	--	μJ
Turn-on Switching Energy	E_{on}	$V_{DS} = 650V,$ $V_{GS} = 0/15V, I_D = 20A,$ $R_{G(ext)} = 2.5\Omega$	--	194*	--	
Turn-off Switching Energy	E_{off}		--	326*	--	
Internal Gate Resistance	$R_{G(int.)}$	$f = 1MHz, V_{AC} = 25mV$	--	3	--	Ω

*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on} .

Built-in SiC Diode Characteristics						
Continuous Diode Forward Current	I_S	$V_{GS} = 0V$	--	100	--	A
Inverse Diode Forward Voltage	V_{SD}	$I_{SD} = 30A, V_{GS} = -5V$	--	--	6	V
Reverse Recovery Time	t_{rr}	$I_F = 25A, V_{DS}=150V, di_F/dt = 500A/\mu s$	--	72	--	ns
Reverse Recovery Charge	Q_{rr}		--	181	--	nC
Peak Reverse Recovery Current	IRM		--	4.6	--	A

Typical Device Performance

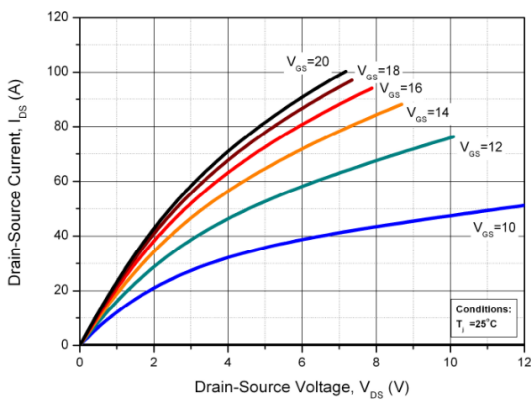


Fig. 1 Forward Output Characteristics at $T_j = 25^\circ C$

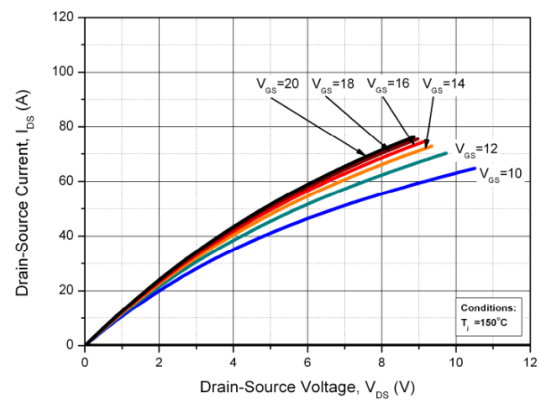


Fig. 2 Forward Output Characteristics at $T_j = 150^\circ C$

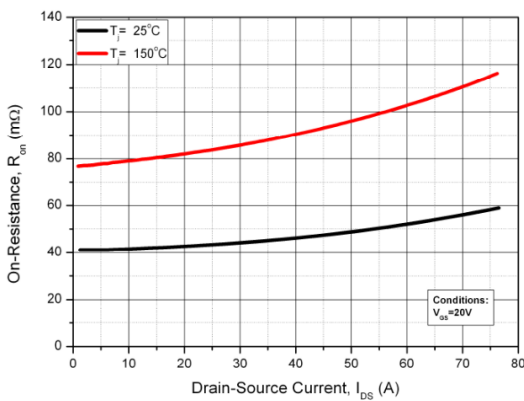


Fig. 3 On-Resistance vs. Drain Current for Various T_j

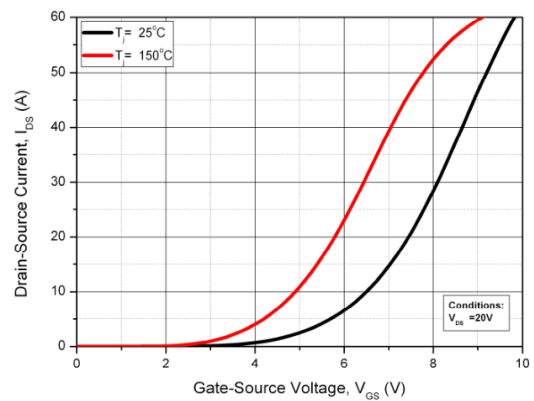


Fig. 4 Transfer Characteristics for Various T_j

Typical Device Performance

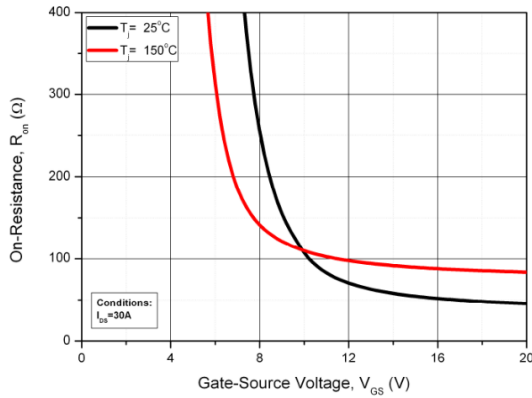


Fig. 5 On-Resistance vs. Gate Voltage for Various T_j

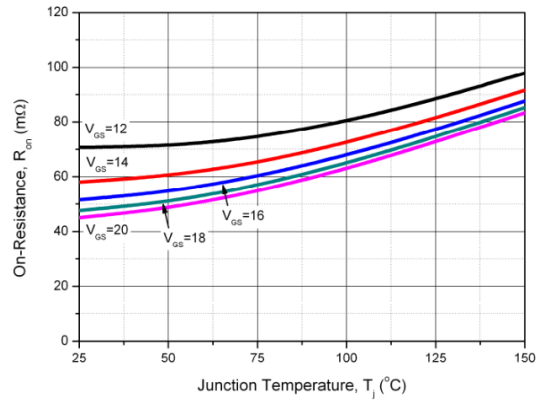


Fig. 6 On-Resistance vs. Temperature for Various Gate Voltage

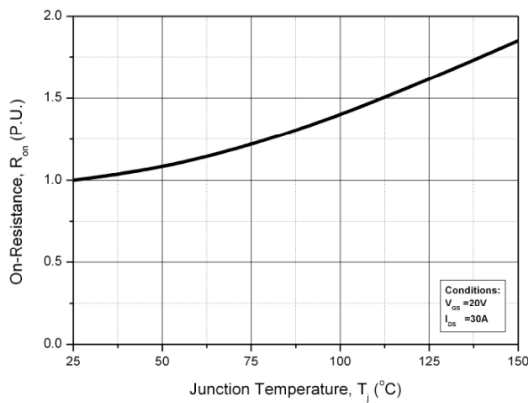


Fig. 7 Normalized On-Resistance vs. Temperature

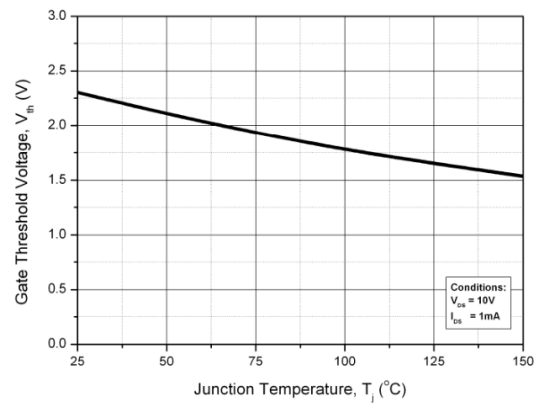


Fig. 8 Threshold Voltage vs. Temperature

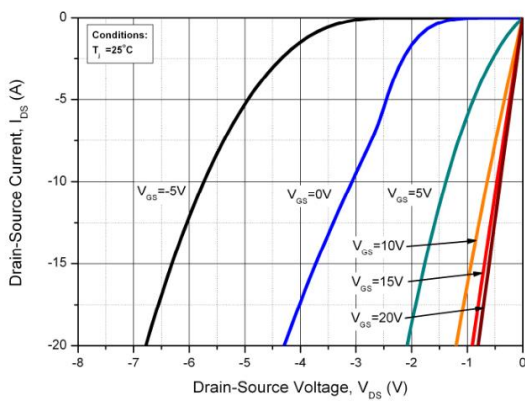


Fig. 9 Reverse Output Characteristics at $T_j = 25^\circ\text{C}$

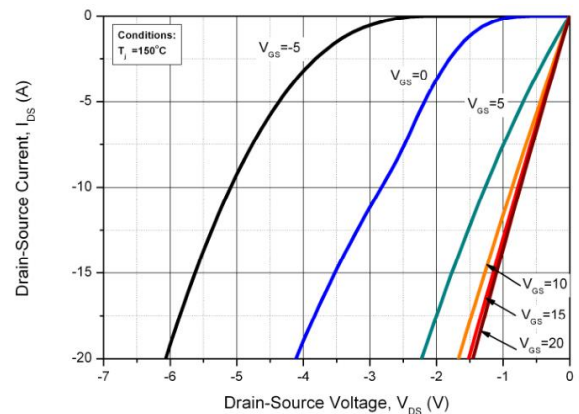


Fig. 10 Reverse Output Characteristics at $T_j = 150^\circ\text{C}$

Typical Device Performance

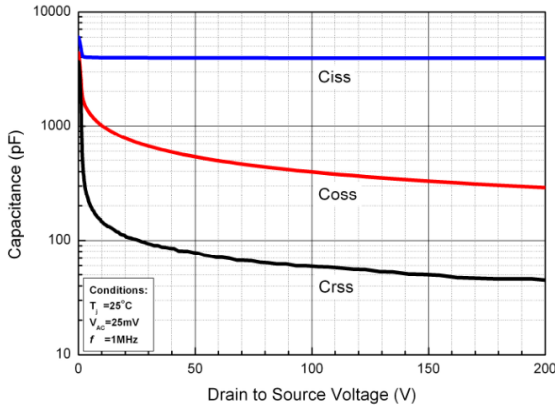


Fig. 11 Capacitances vs. Drain to Source Voltage (0 - 200V)

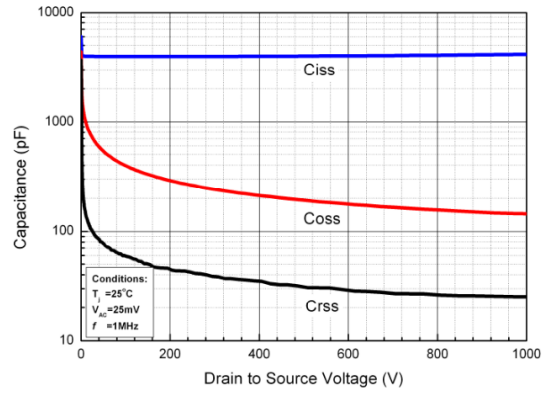


Fig. 12 Capacitances vs. Drain to Source Voltage (0 - 1000V)

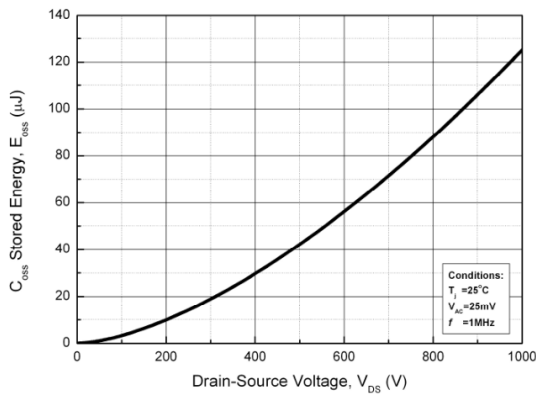


Fig. 13 Output Capacitor Stored Energy

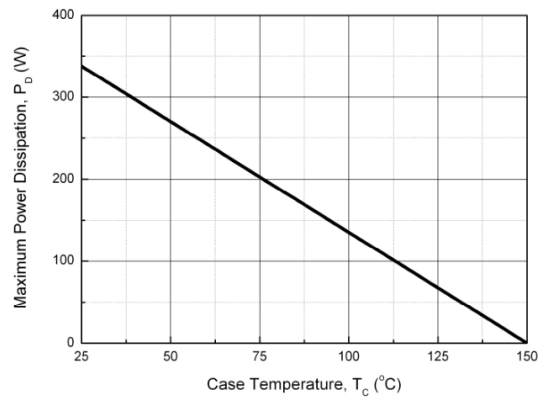


Fig. 14 Maximum Power Dissipation Derating vs. Case Temperature

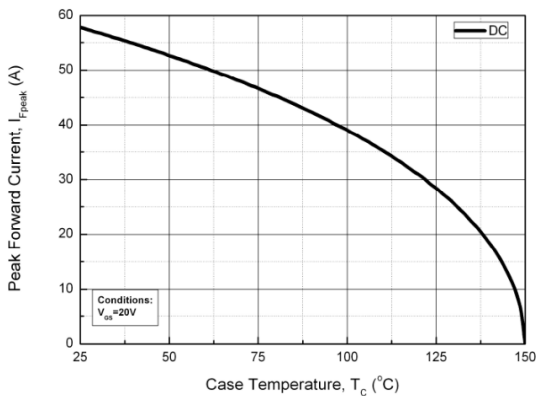


Fig. 15 Drain Current Derating vs. Case Temperature

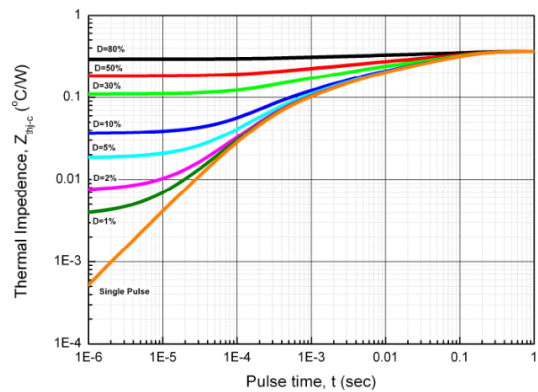
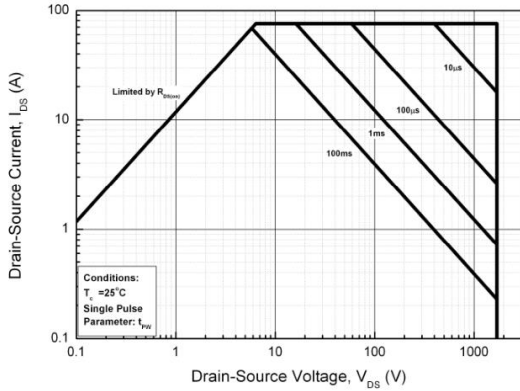
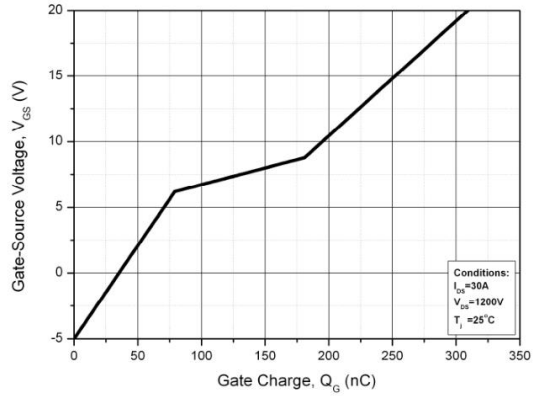
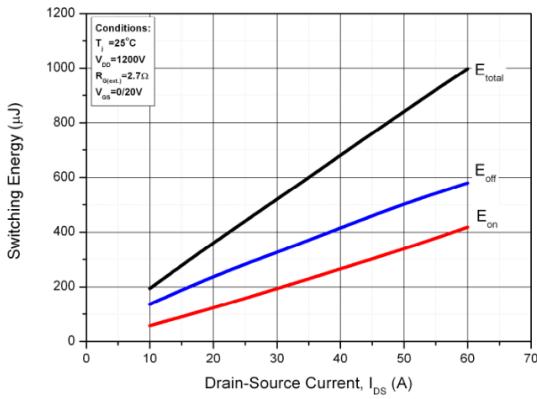
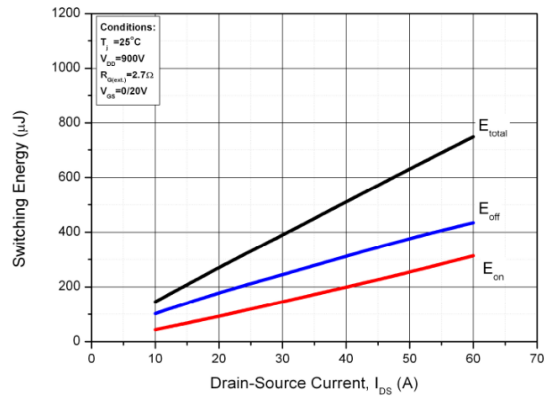
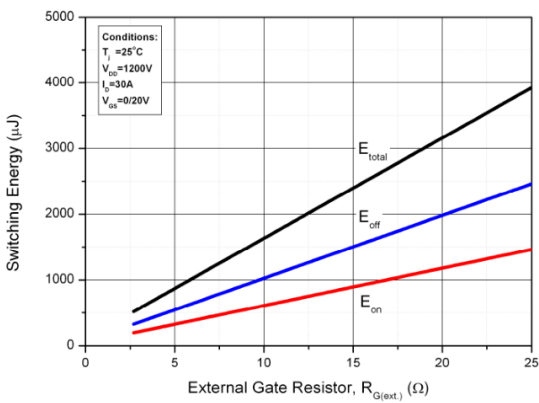
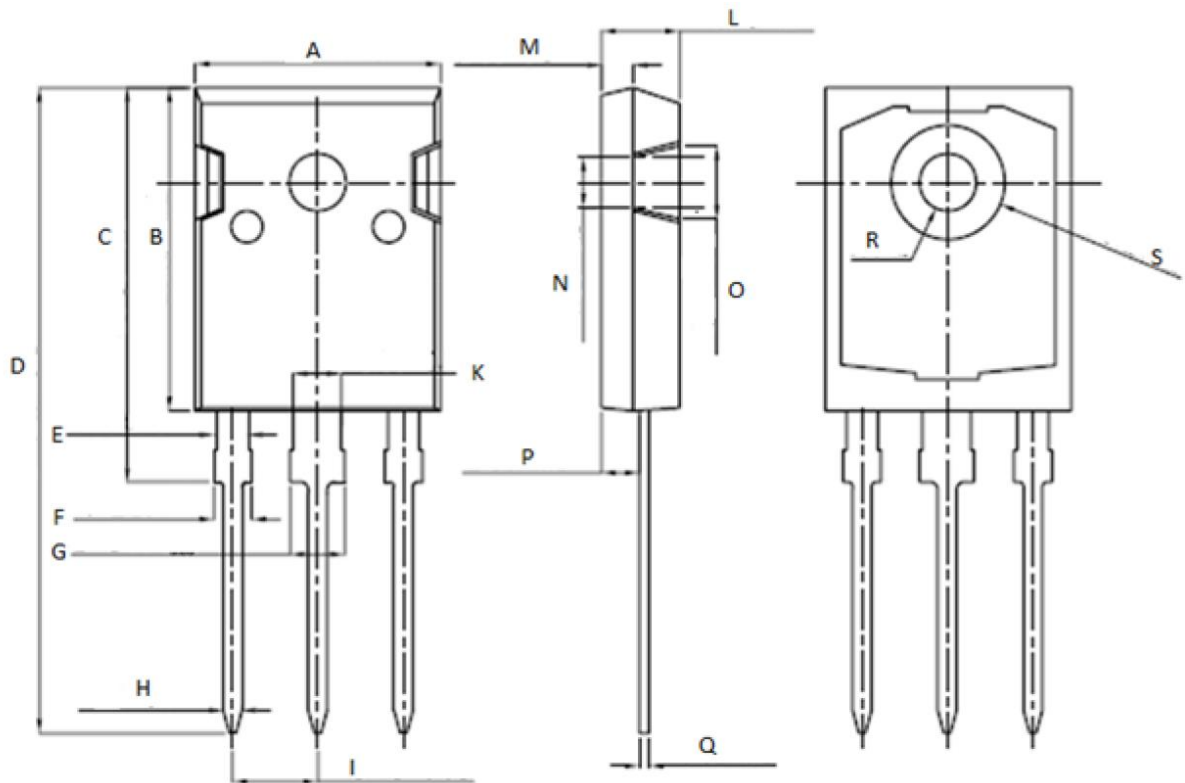


Fig. 16 Transient Junction to Case Thermal Impedance

Typical Device Performance

Fig. 17 Safe Operating Area

Fig. 18 Gate Charge Characteristics

Fig. 19 Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 1200\text{V}$)*

Fig. 20 Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 900\text{V}$)*

Fig. 21 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)*

*Base on the results of calculation, note that the energy loss caused by the reverse recovery of FWD is not included in E_{on} .

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Unit: mm		
Symbol	Min.	Max.
A	15.95	16.25
B	20.85	21.25
C	20.95	21.35
D	40.5	40.9
E	1.9	2.1
F	2.1	2.25
G	3.1	3.25
H	1.1	1.3
I	5.40	5.50

Unit: mm		
Symbol	Min.	Max.
K	2.90	3.10
L	4.90	5.30
M	1.90	2.10
N	4.50	4.70
O	5.40	5.60
P	2.29	2.49
Q	0.51	0.71
R	φ 3.5	φ 3.7
S	φ 7.1	φ 7.3

*The information provided herein is subject to change without notice.

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